Overview

Feature

- Integrated dual photodiode architecture and VCSEL IR emitter in one package
- Tiny 2mm x 1mm x 0.5mm module
- Crosstalk and ambient light cancellation
- Integrate factory calibrated 940 nm IR VCSEL
- Wide configuration range
- V_{DD} wide operation range 1.7~2.0v
- 1.8V Power Supply with 1.8~3.3V I^2C bus

Application

- Wearable product for power control
- User detection application

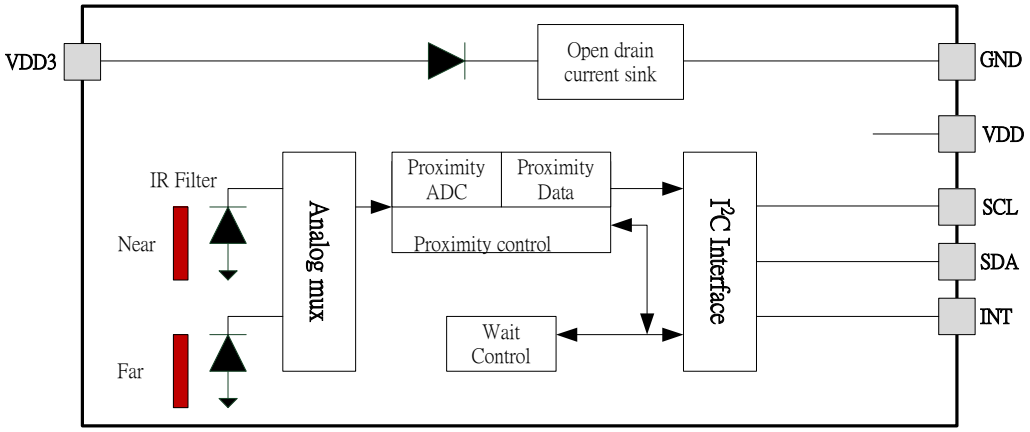
Description

The ELP2600 features proximity measurement (PS) with the extremely tiny 2mm x 1mm x 0.5mm module. This Device incorporates 940nm IR VCSEL and is factory calibrated for IR proximity response. The Device provides object detection by photodiode detection of the reflected IR light from integrated VCSEL emitter.

The ELP2600 incorporates Photodiode, timing control, ADC and VCSEL emitter into one chip. The Device provides excellent proximity detection. The proximity engine features a wide range offset adjustment to compensate for unwanted IR energy reflection at the sensor.

The ELP2600 has provided temperature calibration features and also has lower power design, including standby mode and wait mode support. The ELP2600 provide dual photodiode architecture allows applications to accurately detect proximity which enables devices to provide excellent power control management.

Block Diagram



Pin Description

Description

Name	Pin No.	IO	Description
INT	1	IO	Interrupt pin (open drain)
VDD	2	P	Power supply:1.7v~2.0v
GND	3	G	Ground
VDD3	4	P	Supply Voltage for IR emitter (2.8v~3.6v)
SCL	5	I	IIC clock
SDA	6	IO	IIC data (open drain)

Electrical Specification

■ Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
VDD	Supply Voltage to GND	-0.3	2.0	V	
VDD3	IR emitter Voltage to GND	-0.3	3.6	V	
V_{IO}	Digital I/O Terminal Voltage	-0.3	3.6	V	
I_{IO}	Digital Output Terminal Current	-1	20	mA	
Electrostatic Discharge					
I_{SCR}	Input Current (latch-up immunity)	± 100		mA	Class II JEDEC JESD78E
ESD_{HBM}	HBM Electrostatic Discharge	± 2000		V	JEDEC/ESDA JS-001-2017
ESD_{CDM}	CDM Electrostatic Discharge	± 500		V	JEDEC JS-002-2014
Temperature Ranges and Storage Conditions					
T_{STRG}	Storage Temperature Range	-40	85	°C	
T_{BODY}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020 The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices."
RH_{NC}	Relative Humidity (non-condensing)		85	%	
P_{DISS}	Power Dissipation		50	mW	Average power dissipation over a 1 second period

Recommended Operation condition

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Supply Voltage to Sensor	1.7	1.8	2.0	V
VDD3	Supply Voltage to IR emitter	2.8	3.3	3.6	V
f_{I2C}	Clock frequency of I^2C	-	-	400	kHz
T_A	Operating Ambient Temperature	-30		85	˚C

Electrical and Proximity sensor characteristics

Electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Active State (PON=1) (1)		315		μA
		Active State (PON=1) (2)		10		
		Idle State(PON=1)		24		
		Sleep State (PON = 0) (3)		0.5		
V_{OL}	INT, SDA output low voltage	6mA sink current			0.6	V
I_{LEAK}	Leakage current, SDA, SCL, INT		-5		5	μA
V_{IH}	SCL, SDA input high voltage(3)		1.26			V
V_{IL}	SCL, SDA input low voltage				0.54	V
T_{Active}	Time from power-on to ready to receive I^2C commands			1.5		ms

Note(s):

1. Active state occurs when PON =1 and the device is actively integrating. For the PS operation, 16 pulse with a pulse width of 16us and a VCSEL current of 10mA are used during a measurement time of 2.78ms.
2. Active state occurs when PON =1 and the device is actively integrating. For the PS operation, 4 pulse with a pulse width of 6us and a VCSEL current of 5mA are used during a measurement time of 100ms.
3. Sleep state occurs when PON = 0 and I^2C bus is idle. If sleep state has been entered as the result of operational flow, SAI = 1, PON will remain high.
4. Digital pins: SDA, SCL, INT are tolerant to a communication voltage up to 3.6V

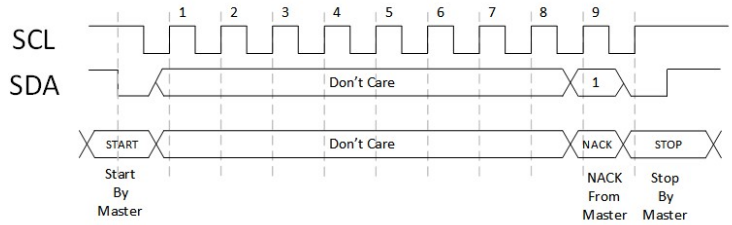
■ Proximity sensor characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Peak sensitivity wavelength for PS			940		um
PS_{FS}				4096	Counts
Detection distance	10mA, 16 us pulse width, 16pulse		3		cm
VCSEL pulse current				10	mA
VCSEL pulse width				16	us
Numbers of VCSEL pulse			16	64	pulse

I2C Timing Diagram

IIC Communication

Dummy Command:



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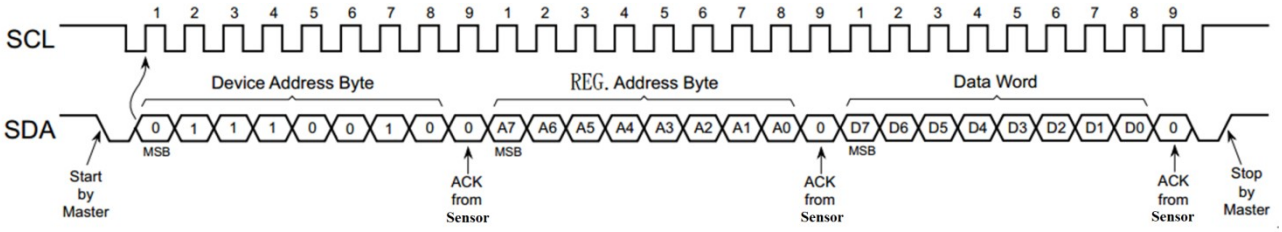
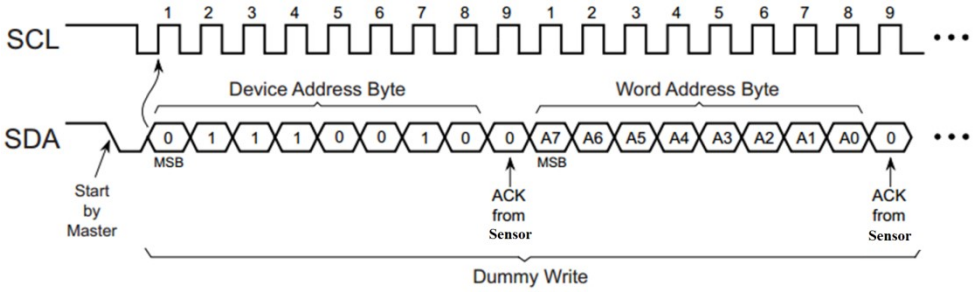
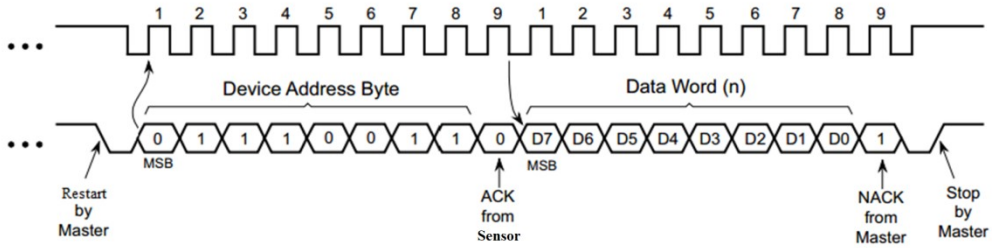
Write:



Read:





- I2C address selection

Master I²C Bus Signal		7-Bit I²C Address
Clock	Data	
SCL	SDA	0x39
SDA	SCL	0x38

Notes:

A Single dummy I2C access (read or write with valid I2C stop) to the device is required to initialize the device their respective I2C address. The device will feedback a NOT-ACKNOWLEDGE (NACK) during initial dummy access.

Register Description

■ Register table

Address	Register Name	R/W	Register Function	Reset Value
0x80	ENABLE	R/W	Enables states and interrupts	0x00
0x82	PRATE	R/W	Proximity time	0x00
0x88	PILTL	R/W	Proximity interrupt low threshold low byte	0x00
0x89	PILTH	R/W	Proximity interrupt low threshold high byte	0x00
0x8A	PIHTL	R/W	Proximity interrupt high threshold low byte	0x00
0x8B	PIHTH	R/W	Proximity interrupt high threshold high byte	0x00
0x8C	PERS	R/W	Proximity interrupt persistence filters	0x00
0x8D	CFG0	R/W	Configuration zero	0x50
0x8E	PCFG0	R/W	Proximity configuration zero	0x8F
0x8F	PCFG1	R/W	Proximity configuration one	0x60
0x90	CFG1	R/W	Configuration one	0x40
0x91	REVID	R	Revision ID	0x10
0x92	ID	R	Device ID	0x44
0x9B	STATUS	R, SC	Device status	0x00
0x9C	PDATAL	R	Proximity ADC low data	0x00
0x9D	PDATAH	R	Proximity ADC high data	0x00
0xA6	REVID2	R	Revision ID two	0x01
0xA8	SOFTRST	R/W	Soft reset	0x00
0xA9	PWTIME	R/W	Proximity wait time	0x00
0xAA	CFG8	R/W	Configuration eight	0x02
0xAB	CFG3	R/W	Configuration three	0x04
0xAE	CFG6	R/W	Configuration six	0x3F
0xB3	PFILTER	R/W	Proximity filter	0x00
0xC0	POFFSETL	R/W	Proximity offset low data	0x00
0xC1	POFFSETH	R/W	Proximity offset high data	0x00
0xD7	CALIB	R/W	Proximity offset calibration	0x00
0xD9	CALIBCFG	R/W	Proximity offset calibration control	0x50
0xDC	CALIBSTAT	R	Proximity offset calibration status	0x00

0xDD	INTENAB	R/W	Interrupt enables	0x00
0xF6	PSDA	R/W	Proximity offset Calibration	0x60

Detail of Register Description

■ *Enable register (Address 0x80)*

Addr: 0x80		Enable		
Bit	Bit Name	Default	Access	Bit Description
7:5	Reserved	000	--	Reserved
4	PWEN	0	RW	This bit activates the proximity wait feature which is set by the PWTIME register. Active high.
3	Reserved	0	--	Reserved
2	PEN	0	RW	This bit activates the proximity detection. Active high.
1	Reserved	0	--	Reserved
0	PON	0	RW	This field activates the internal oscillator and ADC channels. Active high.

■ *PRATE register (Address 0x82)*

Addr:0x82		PRATE		
Bit	Bit Name	Default	Access	Bit Description
7:0	PRATE	0x00	RW	**PS Integration Time Value** The PRATE value specifies the PS integration time in 2.78ms intervals. 0x00 indicates 2.78ms. The maximum PS count value depends on the integration time.

Note :

- **PS Integration Time depends on the "Pulse Length", "Pulse Number".**
- **PS Integration Time must be set more than 20 x 2 + 2 x (4 + Pulse_Length + 2) x (Pulse_Number + 1) + 9 + 69 (us)**

■ *PILTL Register (Address 0x88)*

Addr: 0x88		PILTL		
Bit	Bit Name	Default	Access	Bit Description
7:0	PILTL	0x00	RW	**PS Low Threshold Value** This register contains the low byte of the 12-bit proximity LOW threshold when APC is disabled. If APC is enabled, the register contains the low byte of the 16-bit proximity LOW threshold.

■ *PILTH Register (Address 0x89)*

Addr: 0x89		PILTH		
Bit	Bit Name	Default	Access	Bit Description
7:0	PILTH	0x00	RW	**PS Low Threshold Value** This register contains the upper 4-bits of the 12-bit proximity LOW threshold when APC is disabled. If APC is enabled, the register contains the high byte of the 16-bit proximity LOW threshold.

■ *PIHTL Register (Address 0x8A)*

Addr: 0x8A		PIHTL		
Bit	Bit Name	Default	Access	Bit Description
7:0	PIHTL	0x00	RW	**PS High Threshold Value** This register contains the low byte of the 12-bit proximity HIGH threshold when APC is disabled. If APC is enabled, the register contains the low byte of the 16-bit proximity HIGH threshold.

■ *PIHTH Register (Address 0x8B)*

Addr: 0x8B		PIHTH		
Bit	Bit Name	Default	Access	Bit Description
7:0	PIHTH	0x00	RW	**PS High Threshold Value** This register contains the upper4-bits of the 12-bit proximity HIGH threshold when APC is disabled. If APC is enabled, the register contains the high byte of the 16-bit proximity HIGH threshold.

■ *PERS Register (Address 0x8C)*

Addr: 0x8C		PERS			
Bit	Bit Name	Default	Access	Bit Description	
7:4	Reserved	0000	--	Reserved.	
3:0	PERS	0000	RW	This register sets the PS persistence filter.	
				0 (0000)	Every PS cycle
				1 (0001)	Any value outside PS thresholds
				2 (0010)	2 consecutive PS values out of range
				3 (0011)	3 consecutive PS values out of range
				4 (0100)	4 consecutive PS values out of range
				5 (0101)	5 consecutive PS values out of range
				6 (0110)	6 consecutive PS values out of range
				7 (0111)	7 consecutive PS values out of range
				…	…
				13 (1101)	13 consecutive PS values out of range
				14 (1110)	14 consecutive PS values out of range
				15 (1111)	15 consecutive PS values out of range

■ *CFG0 Register (Address 0x8D)*

Addr: 0x8D		CFG0		
Bit	Bit Name	Default	Access	Bit Description
7:4	Reserved	0101	--	Reserved. **Must be set to default value.**
3	PWLONG	0	RW	**PS Wait Long Flag** The PWTIME is increased by a factor of 16 when PWLONG is asserted. PWLONG = 1, PWTIME = PWTIME x 16 PWLONG = 0, PWTIME = PWTIME x 1
2:0	Reserved	000	--	Reserved. **Must be set to default value.**

■ *PCFG0 Register (Address 0x8E)*

Addr: 0x8E		PFCG0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	PGAIN1	10	RW	**PS Gain1 Value** PGAIN1 = 0, 1x gain. PGAIN1 = 1, 2x gain. PGAIN1 = 2, 4x gain. PGAIN1 = 3, 8x gain.
5:0	PPULSE	001111	RW	**PS Pulse Number Value** The PPULSE sets the maximum number of pulses in a single proximity cycle. Max. pulse number=64

■ *PCFG1 Register (Address 0x8F)*

Addr: 0x8F		PFCG1			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:5	PPULSE _LEN	011	RW	**PS Pulse Length Value** The minimum pulse length is 5μs	
				Value	Pulse Length
				(000)0	5μs
				(001)1	6μs
				(010)2	7μs
				(011)3	8μs
				(100)4	12μs
				(101)5	16μs
				(110)6	24μs
				(111)7	32μs
4	Reserved	0	--	Reserved.	
3:0	PLDRIVE	0001	RW	**PS Pulse Drive Current** The drive strength of the IR VCSEL current is set by the field	
				PLDRIVE	VCSEL Current
				0001	3mA
				0010	4mA

				0011	5mA
				0100	6mA
				0101	7mA
				0110	8mA
				0111	9mA
				1000	10mA
				others	7mA

■ *CFG1 Register (Address 0x90)*

Addr: 0x90		CFG1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	Reserved	0	--	Reserved.
6:5	PGAIN2	10	RW	**PS Gain2 Value** PGAIN2 = 0, 2.5x gain. PGAIN2 = 1, 5x gain. PGAIN2 = 3, 10x gain. Others, 1x gain
4:0	Reserved	00000	--	Reserved.

■ *REVID Register (Address 0x91)*

Addr: 0x91		REVID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	Reserved	00010	--	Reserved.
2:0	REV_ID	000	RO	Device revision number.

■ *ID Register (Address 0x92)*

Addr: 0x92		ID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2	ID	010001	RO	Device type identification.
1:0	Reserved	00	--	Reserved.

- *STATUS Register (Address 0x9B)*

Addr: 0x9B		STATUS		
Bit	Bit Name	Default	Access	Bit Description
7	PHIGH	0	R, SC	**PS Threshold High Flag** Set when PINT is set and PDATA > high threshold (after persistence). Cleared when PINT is cleared.
6	PLOW	0	R, SC	**PS Threshold Low Flag** Set when PINT is set and PDATA < low threshold (after persistence).Cleared when PINT is cleared.
5	PSAT	0	R, SC	**PS Saturation Flag** Proximity saturation flag indicates that an ambient- or reflective-saturation event occurred during a previous proximity cycle. (Note:PS_IR data = 12'h000 or PS_EM data = 12'h000 including hardware average)
4	PINT	0	R, SC	**PS Interrupt Flag** Proximity interrupt flag indicates that proximity results have exceeded thresholds and persistence settings.
3	CINT	0	R,SC	**Calibration Interrupt Flag** Calibration interrupt flag indicates that calibration has completed.
2	ZINT	0	R,SC	**PS Zero Detection Flag** Zero detection interrupt flag indicates that a zero value in PDATA has caused the proximity offset to be decremented (if AUTO_OFFSET_ADJ = 1).
1	PSAT _REFLE	0	R,SC	**PS Reflective Proximity Saturation Flag** The Reflective Proximity Saturation Interrupt flag signals that the AFE has saturated during the IR VCSEL active portion of proximity integration. (Note : one PS_IR data = 12'h000)

0	PSAT _AMBIT	0	R,SC	**PS Ambient Proximity Saturation Flag** The Ambient Proximity Saturation Interrupt flag signals that the AFE has saturated during the IR VCSEL inactive portion of proximity integration. (Note : one PS_EM data = 12'h000)

- *PDATAL Register (Address 0x9C)*

Addr: 0x9C		PDATAL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PDATAL	0x00	RO	**PS Low Byte Data (PS_L_Data)** This register contains the low byte of the 16-bit proximity ADC data.

- *PDATAH Register (Address 0x9D)*

Addr: 0x9D		PDATAH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PDATAH	0x00	RO	**PS High Byte Data (PS_H_Data)** This register contains the high byte of the 16-bit proximity ADC data.

- *REVID2 Register (Address 0xA6)*

Addr: 0xA6		REVID2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Reserved	0000	--	Reserved.
3:0	VER_ID	0001	RO	Device Version Number

- *SOFTRST Register (Address 0xA8)*

Addr: 0xA8		IRM		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:1	Reserved	0000000	--	Reserved

0	SOFTRST	0	R/W	**Software Reset Enable Flag** Writing a 1 to this bit will cause all registers to be reset to their default state. This will immediately terminate all device operation and put the device into the sleep state. SOFTRST = 1, All registers will be reset to the default state. SOFTRST = 0, Normal operation.

■ *PWTIME Register (Address 0xA9)*

Addr: 0xA9		PWTIME				
Bit	Bit Name	Default	Access	Bit Description		
7:0	PWTIME	0x00	RW	**PS Wait Time Value** The PWTIME value specifies the PS wait time in 2.78ms intervals. 0x00 indicates 2.78ms.		
				PWTIME	Wait Cycles	Wait Time
				0x00	1	2.78ms
				0x01	2	5.56ms
				0x11	18	50ms
				0x23	36	100ms
				……	……	……
				0x3F	64	178ms
				……	……	……
				0xFF	256	712ms

■ *CFG8 Register (Address 0xAA)*

Addr: 0xAA		CFG8			
Bit	Bit Name	Default	Access	Bit Description	
7:2	Reserved	000000	--	Reserved.	
1:0	PDSELECT	10	RW	Proximity PD Selection Flag	
				Value	PD Select
				0	No PD
				1	Far PD
				10	Near PD

				11	Far + Near

■ *CFG3 Register (0xAB)*

Addr: 0xAB		CFG3		
Bit	Bit Name	Default	Access	Bit Description
7	INTRD _CLEAR	0	RW	**Status Reset Flag** If set, then flag bits in the STATUS register will be reset whenever the STATUS register is read over I2C. INTRD_CLR = 1, All flag bits of the STATUS register are reset. INTRD_CLR = 0, IDLE.
6:5	Reserved	00	--	Reserved.
4	SAI	0	RW	**Sleep After Interrupt Enable Flag** The Sleep After Interrupt bit is used to place the device into a low power mode upon an interrupt pin assertion.

PON	SAI	INT	Oscillator
0	X	X	OFF
1	0	X	ON
1	1	1	ON
1	1	0	OFF

3:0	Reserved	0100	RW	Reserved. Must be set to default value.

■ *CFG6 Register (Address 0xAE)*

Addr: 0xAE		CFG6		
Bit	Bit Name	Default	Access	Bit Description
7	Reserved	0	--	Reserved.
6	APC _DISABLE	0	RW	**Proximity Automatic Pulse Control (APC) Disable Flag** APC_DISABLE = 0, APC is enabled. APC_DISABLE = 1, APC is disabled.
5:0	Reserved	111111	--	Reserved. Must be set to default value.

■ *PFILTER Register (Address 0xB3)*

Addr: 0xB3		PFILTER		
Bit	Bit Name	Default	Access	Bit Description

7:2	Reserved	--	--	Reserved.	
1:0	PMAVG	00	RW	Proximity Moving average selection Flag	
				PMAVG	MAV Select
				0	Disabled
				1	2 Values
				10	4 Values
				11	8 Values

■ *POFFSETL Register (Address 0xC0)*

Addr: 0xC0		POFFSETL		
Bit	Bit Name	Default	Access	Bit Description
7:0	POFFSETL	0x00	RW	**Proximity Crosstalk Offset Low Byte** This register contains the low byte of the signed proximity offset adjust value.

■ *POFFSETH Register (Address 0xC1)*

Addr: 0xC1		POFFSETH		
Bit	Bit Name	Default	Access	Bit Description
7:5	Reserved	000	--	Reserved.
4:0	POFFSETH	00000	RW	**Proximity Crosstalk Offset High Byte** This register contains the high byte of the signed proximity offset adjust value.

■ *CALIB Register (Address 0xD7)*

Addr: 0xD7		CALIB		
Bit	Bit Name	Default	Access	Bit Description
7	CALAVG	0	RW	**Calibration Average Enable Flag** Enables proximity hardware averaging as selected with PROX_AVG during calibration. CALAVG = 0, No hardware averaging CALAVG = 1, Hardware averaging enabled
6:5	Reserved	00	--	Reserved.

4	CALPRATE	0	RW	**Calibration PRATE Enable Flag** Enables PRATE during calibration. Useful when averaging is enabled. CALPRATE = 0, PRATE ignored CALPRATE = 1, PRATE applied between averaging samples
3:1	Reserved	000	--	Reserved.
0	START_OFFSET_CAL	0	RW	**Calibration Start Flag** Calibration sequence start. START_OFFSET_CAL = 1, Calibration start. START_OFFSET_CAL = 0, IDLE.

- *CALIBCFG Register (Address 0xD9)*

Addr: 0xD9		CALIBCFG			
Bit	Bit Name	Default	Access	Bit Description	
7:5	BINSRCH_TARGET	010	RW	**Proximity Offset Calibration Target**	
				Value	PDATA Target
				(000)0	3
				(001)1	7
				(010)2	15
				(011)3	31
				(100)4	63
				(101)5	127
				(110)6	255
				(111)7	511
4	Reserved	1	--	Reserved. **Must be set to default value.**	
3	AT_OFS_ADJ	0	RW	**Auto Offset Adjustment** If set, this bit causes the value in POFFSETL register to be decremented if PDATA ever becomes zero.	
2:0	PROX_AVG	000	RW	**PS Hardware Average Number** PROX_AVG defines the number of ADC samples collected and hardware averaged during a proximity cycle.	
				Value	Averaging Cycle
				(000)0	Disable

				(001)1	2
				(010)2	4
				(011)3	8
				(100)4	16

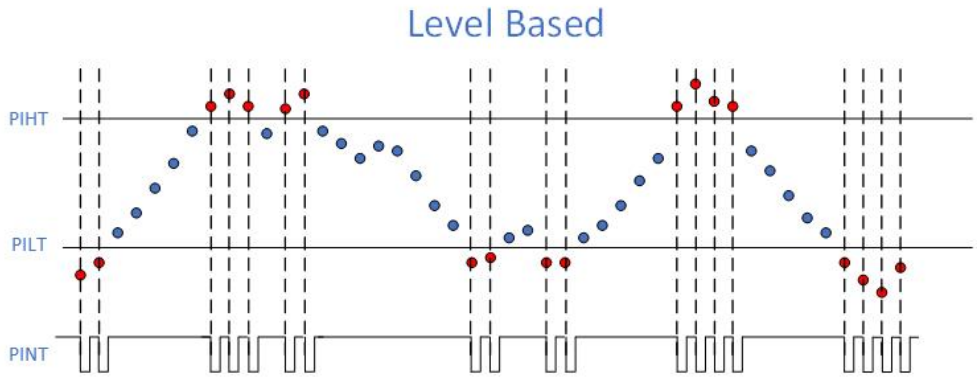
■ *CALIBSTAT Register (Address 0xDC)*

Addr: 0xDC		CALIBSTAT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	Reserved	00000	--	Reserved.
2	OFFSET _ADJUSTED	0	RW	Bit is set when the proximity offset has been automatically decremented if AUTO_OFFSET_ADJ = 1 (see CALIBCFG register). This bit can be cleared by writing 1 to it or setting AUTO_OFFSET_ADJ to 0.
1	Reserved	0	--	Reserved.
0	CALIB_ FINISHED	0	RW	This flag indicates that calibration has finished. This bit is a copy of the CINT bit in the STATUS register. It will be cleared when the CINT bit is cleared.

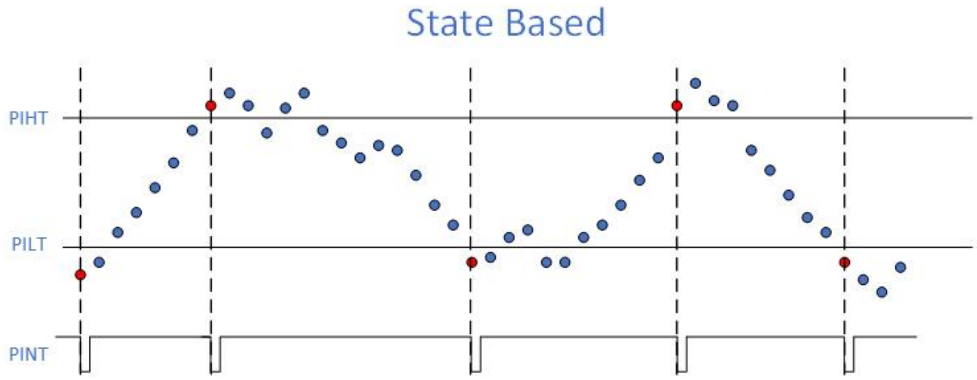
■ *INTENAB Register (Address 0xDD)*

Addr: 0xDD		INTENAB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Reserved	00	--	Reserved. **Must be set to default value.**
5	PIM	0	RW	PS interrupt mode selection PIM=0, Level based PIM=1, State based
4	PIEN	0	RW	PS Interrupt Enable Flag
3	PSIEN	0	RW	PS Saturation interrupt Enable Flag
2	CIEN	0	RW	Calibration Interrupt Enable Flag
1	ZIEN	0	RW	Zero detect Interrupt Enable Flag
0	Reserved	0	--	Reserved.

PIM = 00，Level Mode



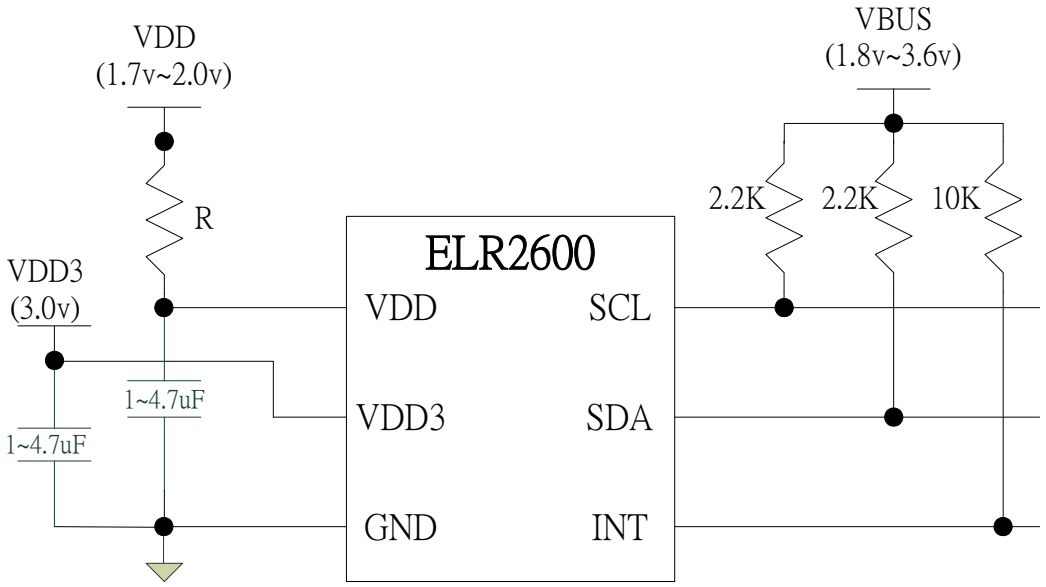
PIM=01，State Mode



■ *PSDA Register (Address 0xF6)*

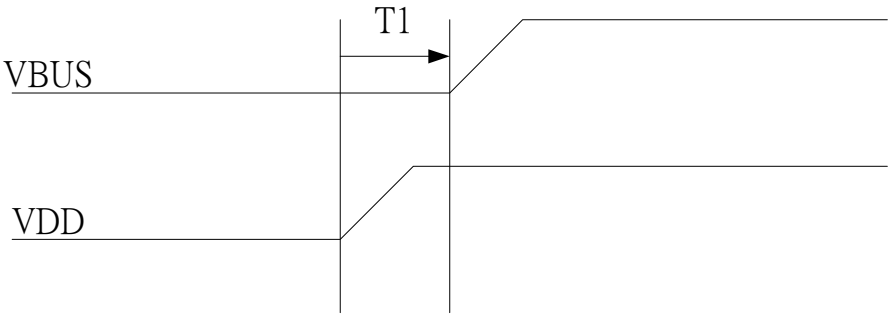
Addr: 0xF6		PSDA		
Bit	Bit Name	Default	Access	Bit Description
7:6	RS	01	RW	PS0 Offset Calibration DA Stage Flag
5:0	PSDA	100000	RW	PS Offset Calibration DA Selection Flag

Application Note



Note: The recommended R value is 22 ohm

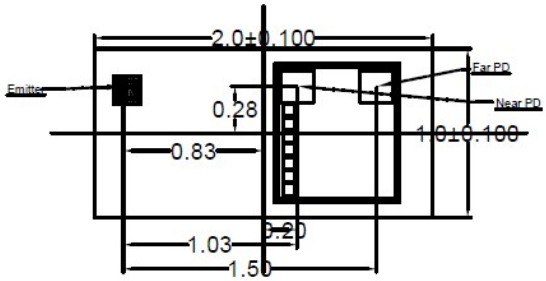
- Power on Sequence

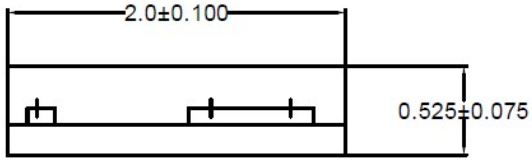


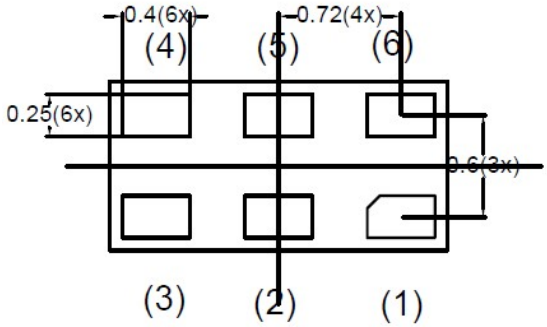
Note: The T1 time is recommended more than 30ms (VDD first is recommended)

Package

- Package Outline Drawing



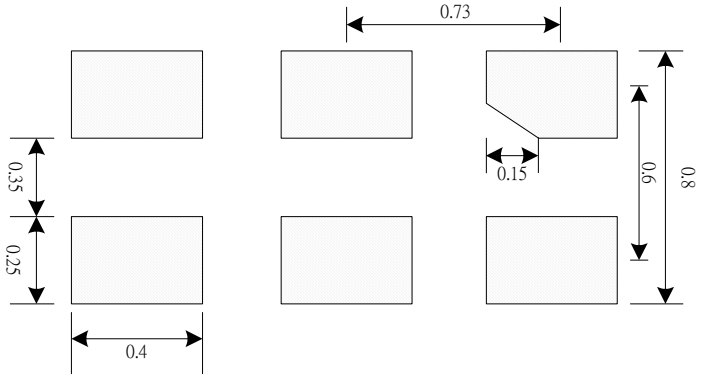




Pin-Out Assignment

1.INT	2.VDD
3.GND	4.VDD3
5.SCL	6.SDA

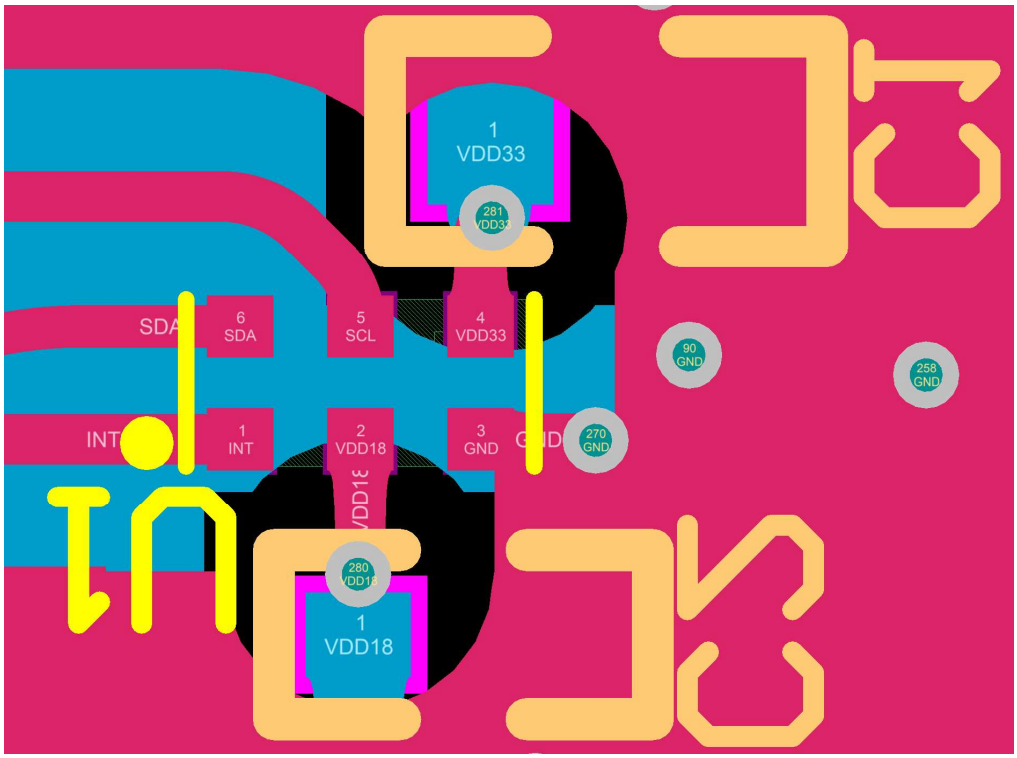
- Recommended PCB Layout



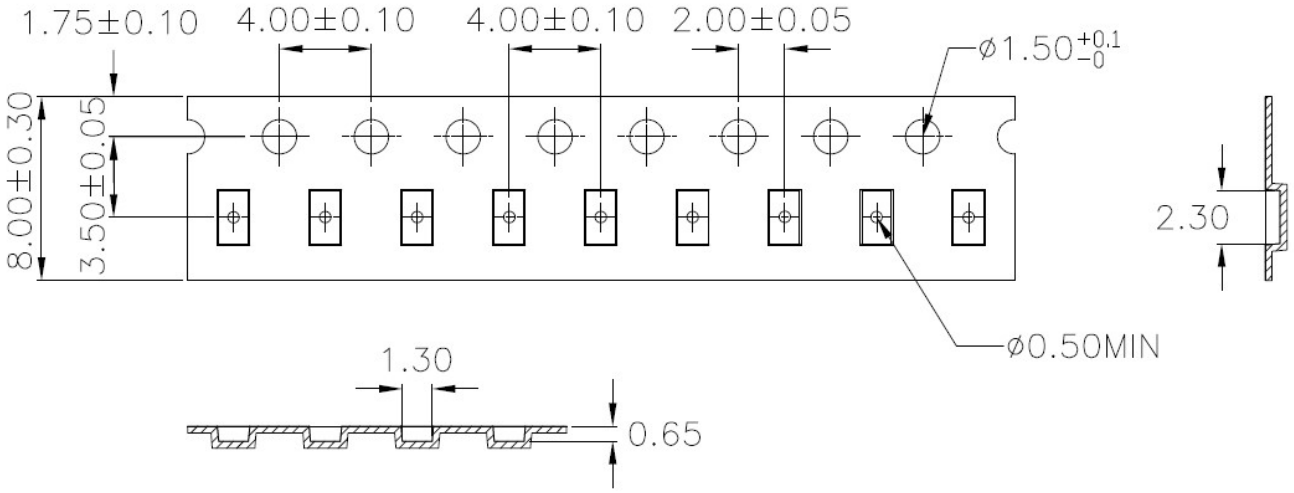
Note: all dimensions are in mm

Layout Guide Line

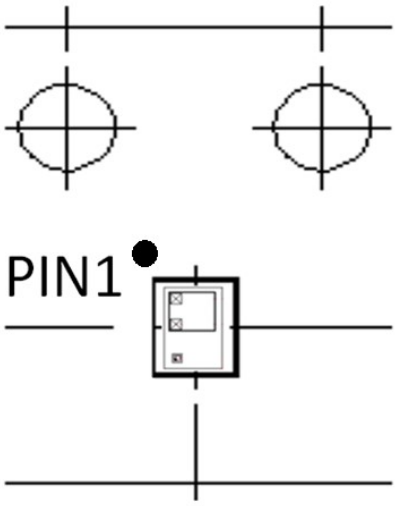
The ELP2600 provides maximum 10mA current to drive the internal VCSEL and different pulse width setting is used to adjust the VCSEL turn on time. VDD3 is not suggested to be shared with other power-hungry device, such as touch panel. The bypass capacitors C1 and C2 can placed on bottom layer of PCB and C1 and C2 should as close ELP2600 as possible.



Tape and Reel Information



Chip in Reel



Order & Packing Information

Package	Product ID	Packing
OPLGA 2.0x1.0x0.5mm	ELP2600GU06NDR	Tape & Reel 3K pcs

GU06: OPLGA 2.0x1.0x0.5mm 6PIN

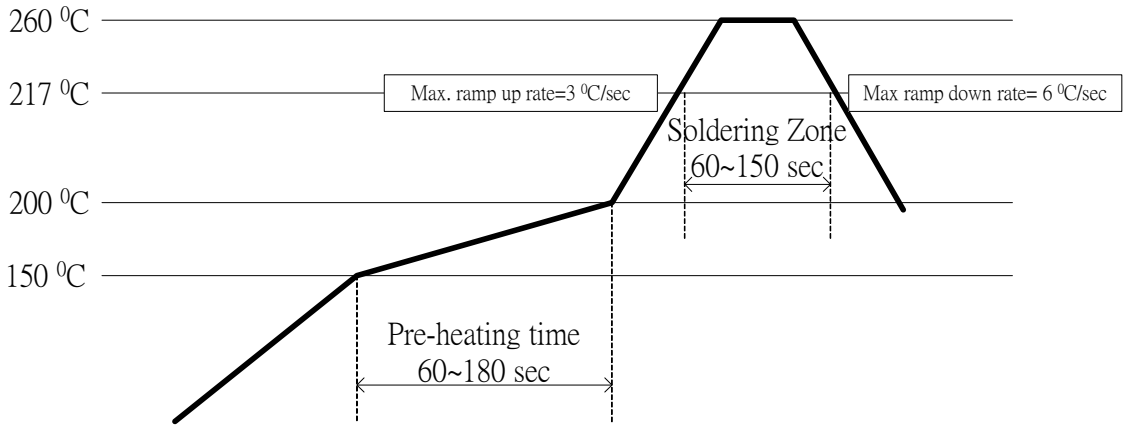
N: RoHS & Halogen free

D:-30~85℃

R:Tape & Reel

Soldering Information

■ Soldering condition



Note [1]: Reflow soldering should not be done more than three times

Note [2]: When soldering, do not stress on IC during heating

Note [3]: After soldering, do not warp the board

Recommended of storage method and ESD precaution

Dry box storage is recommended as soon as the aluminum bag has been opened. It could prevent moisture absorption.
The following conditions should be followed if dry boxes are not available

-- Storage temperature 10C to 30C
-- Storage humidity <= 60% RH max

After more than 72 hours Under the conditions moisture content will be too high for reflow soldering. In case of moisture absorption, the devices will recover to former conditions by drying under the following condition

-- 192 hours at 40C and 5% RH or
-- 96 hours at 60C and < 5% RH for device containers, or
-- 24 hours at 125C is not suitable for reel

ESD precaution
-- When the Chips are removed from Anti-static bag, please follow the handing procedure to prevent ESD damage