EHB0528 12V 1A H-Bridge Driver

General Description

The EHB0528 device provides an integrated motor driver solution for cameras, consumer products, toys, and other low-voltage or battery-powered motion control applications. The device can drive one dc motor or other devices like solenoids. The output driver block consists of N-channel power MOSFETs configured as an H-bridge to drive the motor winding. An internal charge pump is used to generate the required gate drive voltage.

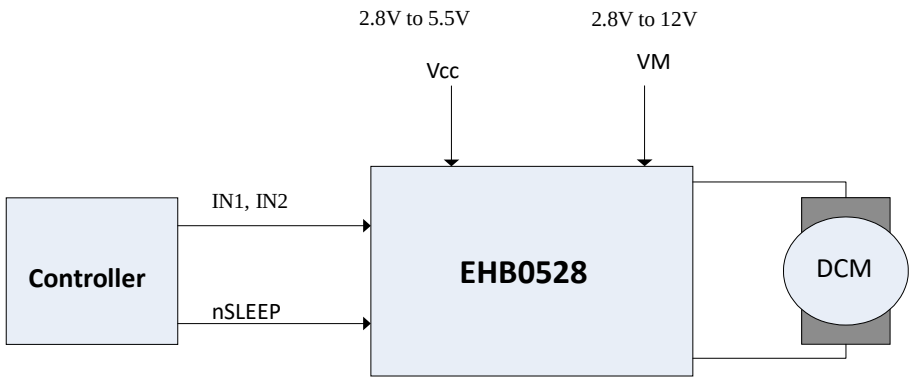
The EHB0528 device can supply up to 1A of output current. It operates on a motor power supply voltage from 2.8V to 12V, and a device power supply voltage of 2.8V to 5.5V. The EHB0528 device has a PWM (IN1/N2) input interface; the interface is compatible with industry-standard devices. Internal shutdown functions are provided for over current protection, short-circuit protection, under voltage lockout, and over temperature.

Features

- Low MOSFET On-Resistance: HS + LS 1Ω
- 1 A Maximum Drive Current
- Separate Motor and Logic Supply Pins:
  - Motor VM: 2.8V to 12V
  - Logic VCC: 2.8V to 5.5V
- Low-Power Sleep Mode
  - 120nA Maximum Sleep Current
- Small Package and Footprint
  - TDFN2x2-8 with Thermal Pad
- Protection Features
  - VCC Under Voltage Lockout (UVLO)
  - Over Current Protection (OCP)
  - Thermal Shutdown (TSD)

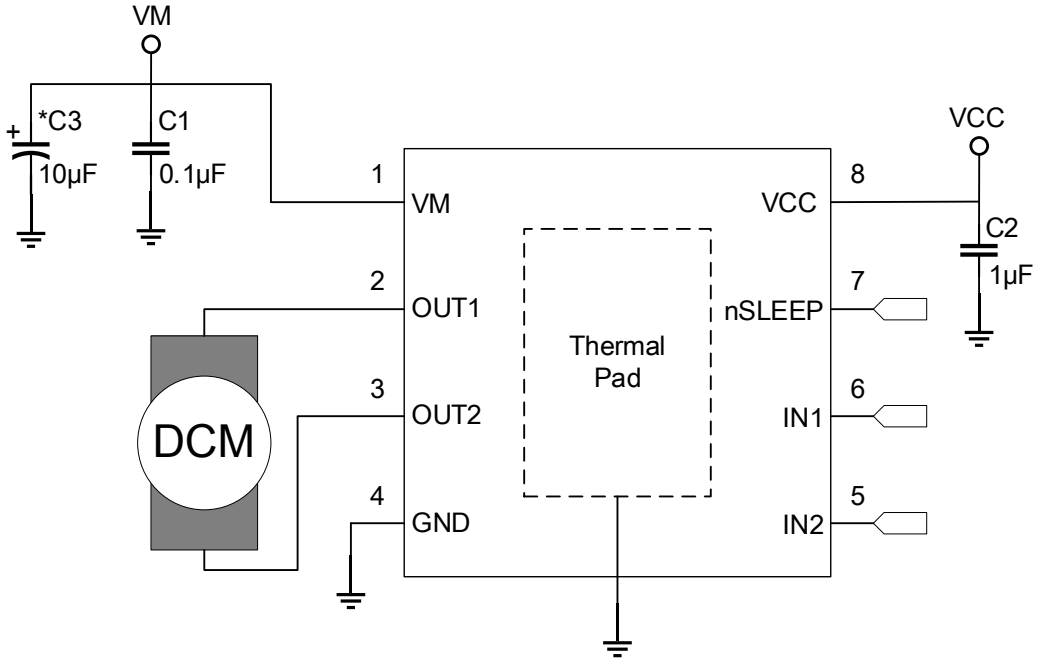
Applications

- Cameras
- DSLR Lenses
- Consumer Products
- Toys
- Robotics
- Medical Devices



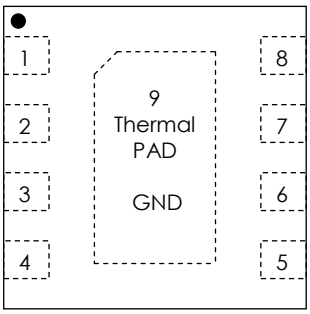
EHB0528 Simplified Diagram

Typical Application



In general, the recommended bypass capacitor value is 1μF for VCC supply and 0.1μF for VM supply respectively. The recommended value of C3 is at least 10μF. For detail, please refer to the chapter "Power Supply Recommendations".

Package Configuration

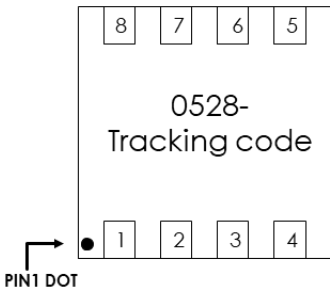


TDFN2x2-8

EHB0528

DA08	TDFN2x2-8 Package
NRR	RoHS & Halogen free package
	Commercial Grade Temperature
	Rating: -40 to 85°C
	Package in Tape & Reel

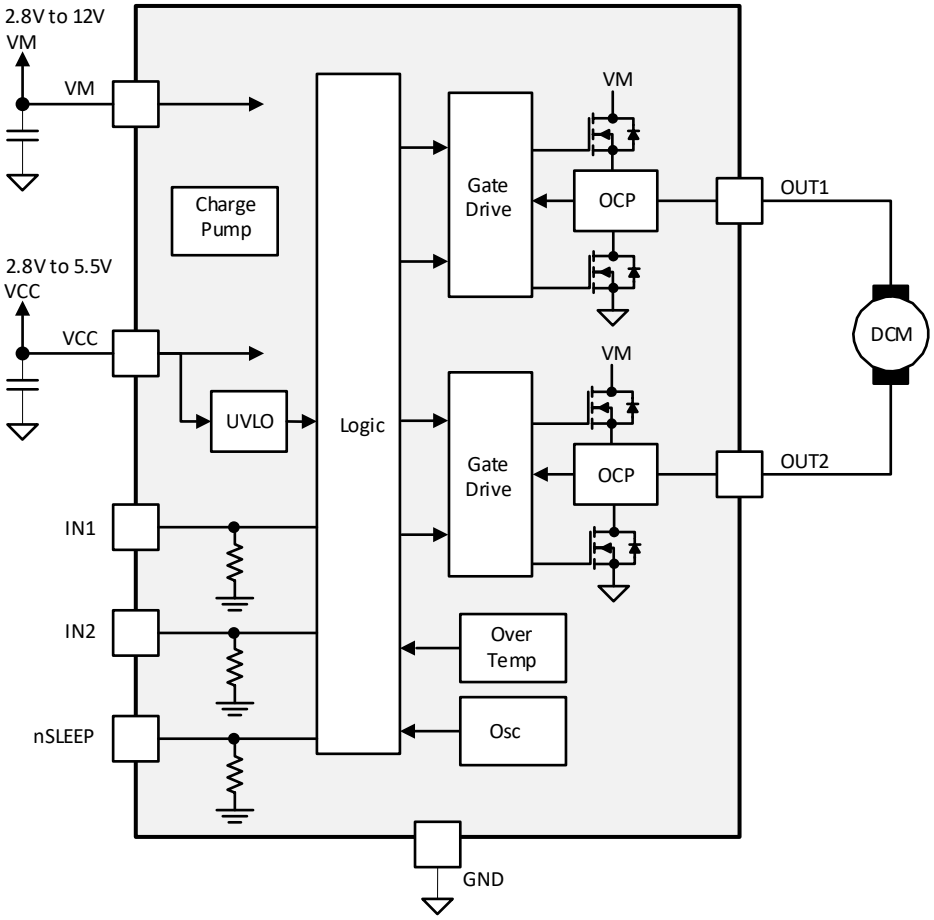
Order, Mark & Packing information

Package	Product ID.	Marking	Packing
TDFN2x2-8	EHB0528-DA08NRR		Tape & Reel 3K pcs

Pin Functions

PIN Name	TDFN2x2-8	DESCRIPTION
VM	1	**Motor power supply.** Bypass this pin to the GND pin with a 0.1μF ceramic capacitor rated for VM.
OUT1	2	**Motor output.** Connect these pins to the motor winding.
OUT2	3	
GND	4	**Ground Pin.**
IN2	5	**IN2 input.** See the Detailed Description section for more information.
IN1	6	**IN1 input.** See the Detailed Description section for more information.
nSLEEP	7	**Sleep mode input.** When this pin is in logic low, the device enters low-power sleep mode. The device operates normally when this pin is logic high. Internal pulldown
VCC	8	**Logic power supply.** Bypass this pin to the GND pin with a 1μF ceramic capacitor rated for VCC.
GND	9	**Ground Pin/Thermal Pad.** This Pin must be connected to ground. The thermal pad with large thermal land area on the PCB will helpful chip power dissipation.

Function Block Diagram



Absolute Maximum Ratings

Devices are subjected to fail if they stay above absolute maximum ratings.

		MIN	MAX	Unit
Motor power-supply voltage	VM	-0.3	14.4	V
Logic power-supply voltage	VCC	-0.3	6	V
Control pin voltage	IN1, IN2, nSLEEP	-0.5	6	V
Peak drive current	OUT1, OUT2	Internally limited		A
Operating virtual junction temperature, T_J(Note 1)		-40	150	°C
Storage temperature, T_{stg}		-60	150	°C

ESD Ratings

			VALUE	Unit
V_{ESD}	Electrostatic	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V
V_{ESD}	Electrostatic	Charged-device model (CDM), per JEDEC specification JESD22-C101	±500	V

Recommended Operating Conditions

		MIN	MAX	Unit
VM	Motor power supply voltage	2.8	12	V
VCC	Logic power supply voltage	2.8	5.5	V
I_{OUT}	Motor peak current	0	1	A
F_{PWM}	Externally applied PWM frequency	0	250	kHz
V_{LOGIC}	Logic level input voltage	0	5.5	V
T_A	Operating ambient temperature	-40	85	°C

Thermal data

Package	Thermal resistance	Parameter	Value
TDFN2x2-8	θ_{JA} (Note 2)	Junction-ambient	74.7°C/W
	θ_{JC} (Note 3)	Junction-case	24°C/W

Note 1: T_J is a function of the ambient temperature T_A and power dissipation P_D ($T_J = T_A + (P_D) * (74.7°C/W)$).

Note 2: θ_{JA} is measured in the natural convection at T_A=25℃ on a highly effective thermal conductivity test board(2 layers , 2S0P) according to the JEDEC 51-7 thermal measurement standard.

Note 3: θ_{JC} represents the heat resistance between the chip and the package top case.

Electrical Characteristic

TA=25°C, over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	Unit
POWER SUPPLIES (VM, VCC)						
I_{VM}	VM operating supply current	VM=5V;VCC=3V; No PWM		100	200	µA
		VM=5V;VCC=3V; 50 kHz PWM		0.8	1.5	mA
I_{VMQ}	VM sleep mode supply current	VM=5V;VCC=3V; nSLEEP = 0		30	95	nA
I_{VCC}	VCC operating supply current	VM=5V;VCC=3V; No PWM		300	500	µA
		VM=5V;VCC=3V; 50kHz PWM		0.7	1.5	mA
I_{VCCQ}	VCC sleep mode supply current	VM=5V;VCC=3V; nSLEEP=0		5	25	nA
CONTROL INPUTS (IN1, IN2, nSLEEP)						
V_{IL}	Input logic-low voltage falling threshold				0.25 x VCC	V
V_{IH}	Input logic-high voltage rising threshold		0.6 x VCC			V
V_{HYS}	Input logic hysteresis			0.08 x VCC		V
I_{IL}	Input logic low current	VIN=0V	-5		5	µA
I_{IH}	Input logic high current	VIN = 3.3 V			50	µA
R_{PD}	Pulldown resistance			100		kΩ
MOTOR DRIVER OUTPUTS (OUT1, OUT2)						
$R_{DS(on)}$	HS + LS FET on-resistance	VM=5V;VCC=3V; IO = 200 mA; TJ = 25°C		1000		mΩ
I_{OFF}	Off-state leakage current	VOUT=0V	–200		200	nA
PROTECTION CIRCUITS						
V_{UVLO}	VCC undervoltage lockout	VCC rising		2.5	2.75	V
		VCC falling		2.4	2.65	V
I_{OCP}	Over current protection trip level		1.2			A
t_{DEG}	Over current deglitch time			1		µs
t_{RETRY}	Over current retry time			2		ms
T_{TSD}	Thermal shutdown temperature			160		°C
T_{HY}	Thermal shutdown Hysteresis			30		°C

Timing Requirements

T_A = 25°C, VM = 5 V, VCC = 3 V, RL = 20 Ω

Time	Parameter	Min	Max	Unit
t1	Output enable time		500	ns
t2	Output disable time		300	ns
t3	Delay time, INx high to OUTx high		600	ns
t4	Delay time, INx low to OUTx low		350	ns
t5	Output rise time	20	188	ns
t6	Output fall time	20	188	ns

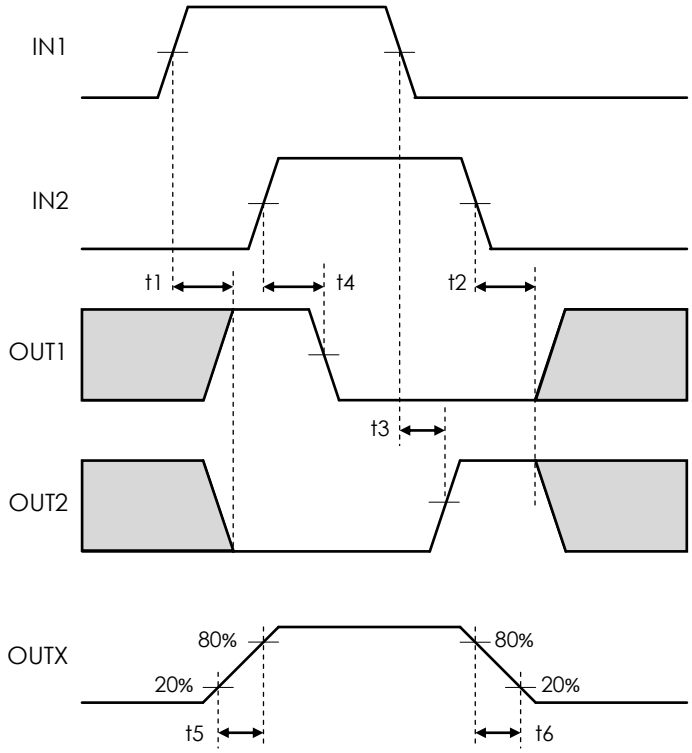


Figure 1. Input and Output Timing

Typical Characteristics

Plots generated using characterization data.

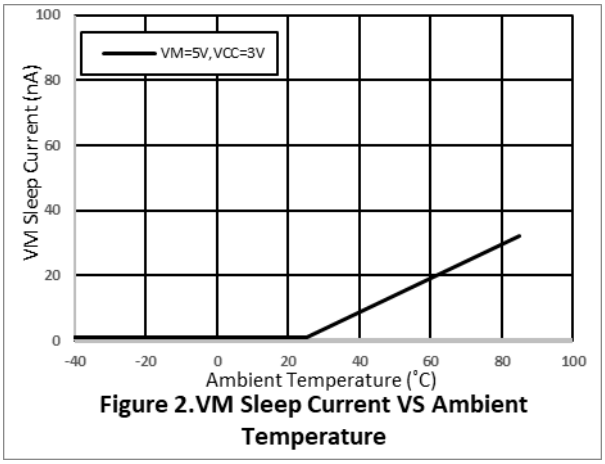


Figure 2.VM Sleep Current VS Ambient Temperature

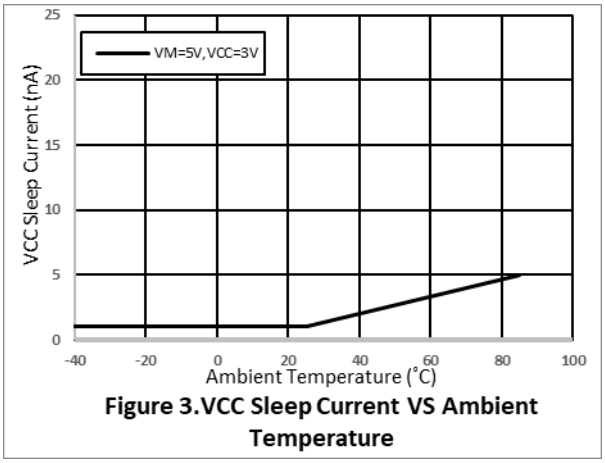


Figure 3.VCC Sleep Current VS Ambient Temperature

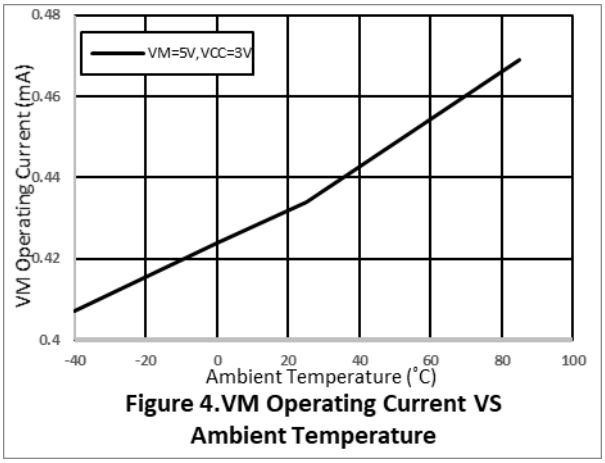


Figure 4.VM Operating Current VS Ambient Temperature

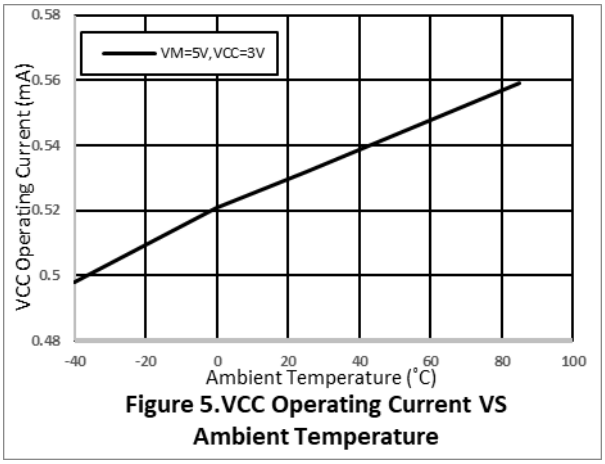


Figure 5.VCC Operating Current VS Ambient Temperature

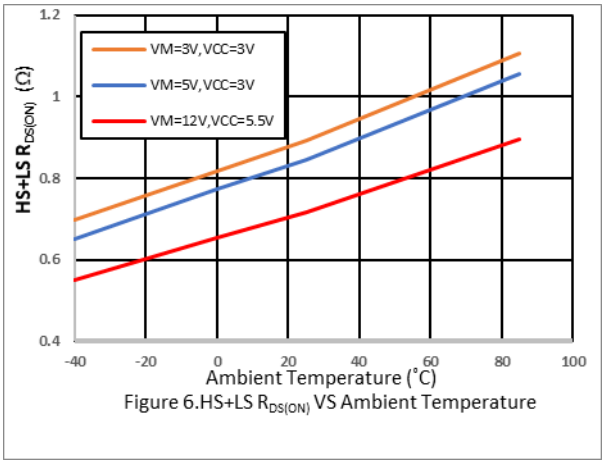


Figure 6.HS+LS $R_{DS(ON)}$ VS Ambient Temperature

Application Information

Detailed Description

The EHB0528 is an H-bridge driver that can drive one dc motor or other devices like solenoids. The outputs are controlled by using a PWM interface (IN1and IN2) on the EHB0528 device. A low-power sleep mode is included, which can be enabled using the nSLEEP pin. These devices greatly reduce the component count of motor driver systems by integrating the necessary driver FETs and FET control circuitry into a single device. In addition, the EHB0528 device adds protection features beyond traditional discrete implementations: undervoltage lockout, overcurrent protection, and thermal shutdown.

Bridge Control

The EHB0528 device is controlled using a PWM input interface, also called an IN-IN interface. Each output is controlled by a corresponding input pin. Table 1 shows the logic for the EHB0528 device.

Table 1. EHB0528 Device Logic

nSLEEP	IN1	IN2	OUT1	OUT2	FUNCTION (DC MOTOR)
0	X	X	Z	Z	Coast
1	0	0	Z	Z	Coast
1	0	1	L	H	Reverse
1	1	0	H	L	Forward
1	1	1	L	L	Brake

Sleep Mode

If the nSLEEP pin is brought to a logic-low state, then the EHB0528 device enters a low-power sleep mode. In this state, all unnecessary internal circuitry is powered down.

Power Supplies and Input Pins

The input pins can be driven within the recommended operating conditions with or without the VCC, VM or both power supplies present. Each input pin has a weak pulldown resistor (approximately 100 kΩ) to ground, thus no leakage current path is existent from the supply voltage to the ground.

The VCC and VM supplies can be applied and removed in any order. When the VCC supply is removed, the device enters a low-power state and draws very little current from the VM supply. The VCC and VM pins can be connected together if the supply voltage is between 2.8V and 5.5V.

The VM voltage supply does not have any undervoltage-lockout protection (UVLO) so as long as VCC >2.75V; the internal device logic remains active, which means that the VM pin voltage can drop to 0V. However, the load cannot be sufficiently driven at low VM voltages.

Protection Circuits

The EHB0528 device provides VCC protection circuitry against under voltage, over current, and over temperature events.

VCC Under Voltage Lockout

When the VCC voltage falls below the undervoltage lockout threshold voltage, all FETs of the H-bridge are disabled. The operation resumes when the VCC pin voltage rises above the UVLO threshold.

Over Current Protection (OCP)

An analog current-limit circuit on each FET limits the current through the FET by disabling the gate driver. If this analog current limit persists for a time longer than tDEG, then all FETs of the H-bridge are disabled. The operation resumes automatically after a period of time (tRETRY) has elapsed. Overcurrent conditions are detected on both the high-side and low-side FETs. Some scenarios will result in an over current condition such as a short to the VIN pin, a short to the GND pin, or a short from the OUT1 pin to the OUT2 pin, etc.

Thermal Shutdown

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled. After the die temperature falls to a safe level, the operation automatically resumes.

Fault Behavior

FAULT	CONDITION	H-BRIDGE	RECOVERY
VCC under voltage (UVLO)	VCC < 2.65V	Disabled	VCC > 2.75 V
Over current (OCP)	I_{OUT} > 1.2 A (MIN)	Disabled	t_{RETRY} elapses
Thermal shutdown (TSD)	T_J ~ 160°C (TYP)	Disabled	T_J ~ 130°C(TYP)

Device Functional Modes

The EHB0528 device is active unless the nSLEEP pin is brought to logic low. In sleep mode, the H-bridge FETs are disabled with a Hi-Z state. The EHB0528 is brought out of sleep mode automatically if nSLEEP is brought to logic high. The H-bridge outputs are disabled during under voltage lockout, over current, and over temperature fault conditions.

Operation Modes

MODE	CONDITION	H-BRIDGE
Operating	nSLEEP pin = 1	Operating
Sleep mode	nSLEEP pin = 0	Disabled
Fault encountered	Any fault condition met	Disabled

Power Supply Recommendations -Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor-drive system design. It is generally beneficial to have more bulk capacitance, though the disadvantages are increased cost and physical size. The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply capacitance and the capability to source current
- The amount of parasitic inductance between the power supply and the motor system
- The acceptable voltage ripple
- The type of motor used (brushed dc, brushless dc, and stepper)
- The motor braking method

The inductance between the power supply and motor drive system limits the rate at which current can change from the power supply. If the local bulk capacitance is too small, then the system needs to respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied. The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate size of bulk capacitor.

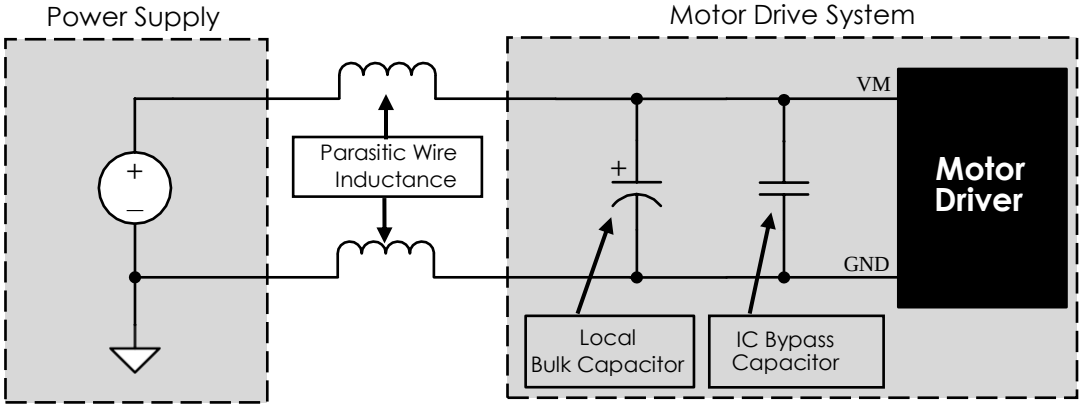
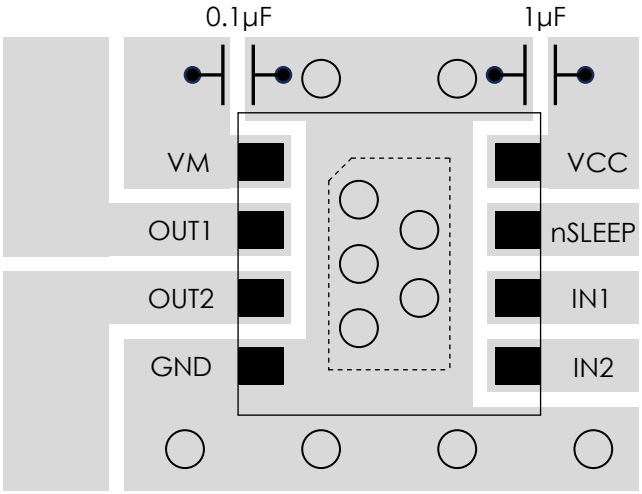


Figure 7 Example Setup of Motor Drive System with External Power Supply

To provide sufficient margin for the cases when the motor transfers energy to the supply, the voltage rating level for the bulk capacitors should be higher than the operating voltage。

Layout Design

The VM and VCC pins should be bypassed to GND using low-ESR ceramic bypass capacitors. In general, the recommended bypass capacitor value is 1μF for VCC supply and 0.1μF for VM supply, respectively. These capacitors should be placed as close to the VM and VCC pins as possible with a thick trace or ground plane connection to the device GND pin. In addition, bulk capacitance is required on the VM pin.



Power Dissipation

Power dissipation in the EHB0528 device is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Use Equation 1 to estimate the average power dissipation when running a brushed-DC motor.

$$P_{TOT} = R_{DS(ON)} \times (I_{OUT(RMS)})^2 \qquad \text{Equation 1}$$

where

- P_{TOT} is the total power dissipation
- $R_{DS(ON)}$ is the resistance of the HS plus LS FETs
- $I_{OUT(RMS)}$ is the RMS or DC output current being supplied to the load

The maximum amount of power that can be dissipated in the device is dependent on the ambient temperature andheatsinking.

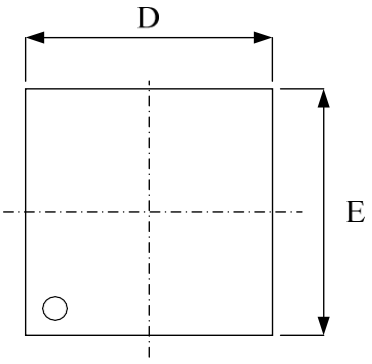
NOTE

The value of $R_{DS(ON)}$ increases with temperature, thus so as the device heats, the powerdissipation also increases.

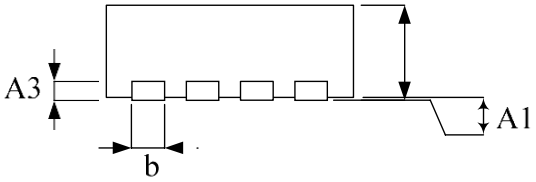
The EHB0528 device has thermal shutdown protection. If the die temperature exceeds approximately 150°C,then the device is disabled until the temperature drops to a safe level.

Any tendency for the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high ambient temperature.

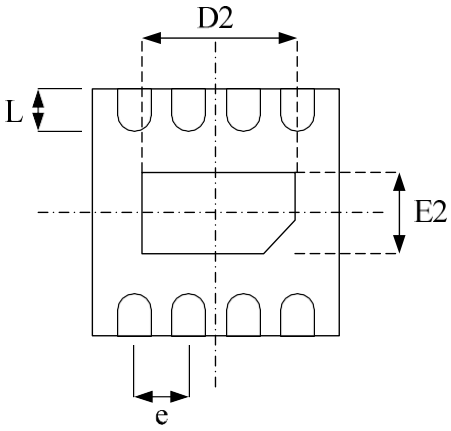
Package Outline Drawing
TDFN2x2-8



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	Dimension in mm	
	Min.	Max.
A	0.70	0.80
A1	0.00	0.05
A3	0.18	0.25
b	0.18	0.30
D	1.90	2.10
E	1.90	2.10
e	0.50 BSC	
L	0.20	
A	0.70	0.80
D2	1.15	1.65
E2	0.65	0.95

Revision History

Revision	Date	Description
1.0	2024.01.26	Original
1.1	2024.02.20	1) Modified Function Block Diagram. 2) Modified VM & VCC Recommended Operating Conditions.
1.2	2024.05.30	Modified VM Recommended Operating Range

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