FOC Motor Controller with 3-Phase 36V P/N Gate Driver

1. Overview

1.1. General Description

The EMG1130 includes a controller that integrates the 8051 core with peripheral circuits to perform Sine-Wave Field-oriented control (F.O.C.) of PMSM/BLDC motor applications. For rotor position detection, it support sensorless, Hall latch, Hall element, and BEMF input. In addition, system level peripheral functions, such as ADC, UART interface, IR decoder, watchdog timer, current sensing, short circuit protection (SCP) and locked-rotor protection are integrated to reduce component count, PCB size and system cost.

The device also includes a P/N gate-driver for 3-phase motor driving applications.

1.2. Features

Motor Controller

- Operation Frequency 24MHz
- High-performance 8051 Microcontroller
- Vector Interrupt Controller, 13 Interrupt Sources
- Operating Voltage Range: 4.5V to 5.5V
- Memory size :
  - 18KB Flash Program Memory
  - 256 x 8bit IRAM
  - 2K x 8bit XRAM
- Up to 18 General-Purpose Input / Output(GPIO) Pins
- Two 16-bit Timers and One 8-bit Timer
- Watchdog (WD) Timer
- 12 Channels 12bit 1MSPS ADC (AD0/1/2 internal used for current shunt, AD10 for 1.5V, AD11 for AVREF)
- 1 UART Serial Channel
  - CRC-8 Support
  - 40 bytes Transmit and Receive Data Buffers
- 16-bit PWM generator with Dead Time Control
- Flash Memory CRC-16 Support
- Deep Sleep Mode current less than 200uA
- Support
  - Sensorless + 1 or 3(2+1) shunts
  - 3 Hall ICs + 1 or 3(2+1) shunts
  - 1 Hall IC + 1 shunt
  - 1 Hall Element + 1 shunt
  - 2 Hall Elements + 1 shunt
  - 3 Hall Elements + 1 shunt
- Space Vector PWM (SVPWM)
- Field Oriented Control (FOC)
- Support Over-modulation control (OVM)
- Support 5&7 sector SVPWM control
- Support 2 Hall elements as loop control
- Initial Position Detection (IPD)
- Built in 3 OPAs (PGA, Max gain:32) & 5 Comparators
- Built in filter of current sense channels and OVP detection
- Support IR decode
- Support Torque/Speed/Power PID loop control
- Support LED brightness and color temperature control
- Support 120,000rpm for one pole pair motor
- Protections: OCP, UVLO and Locked-Rotor protection

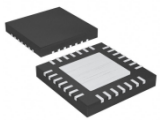
Gate Driver

- Operating Voltage Range: 8V to 36V
- Output 5V V_{GS} for both PMOS and NMOS
- Sourcing/Sinking Current : 100mA/100mA

1.3. Package Type

TSSOP-28L

TQFN5x5-28L

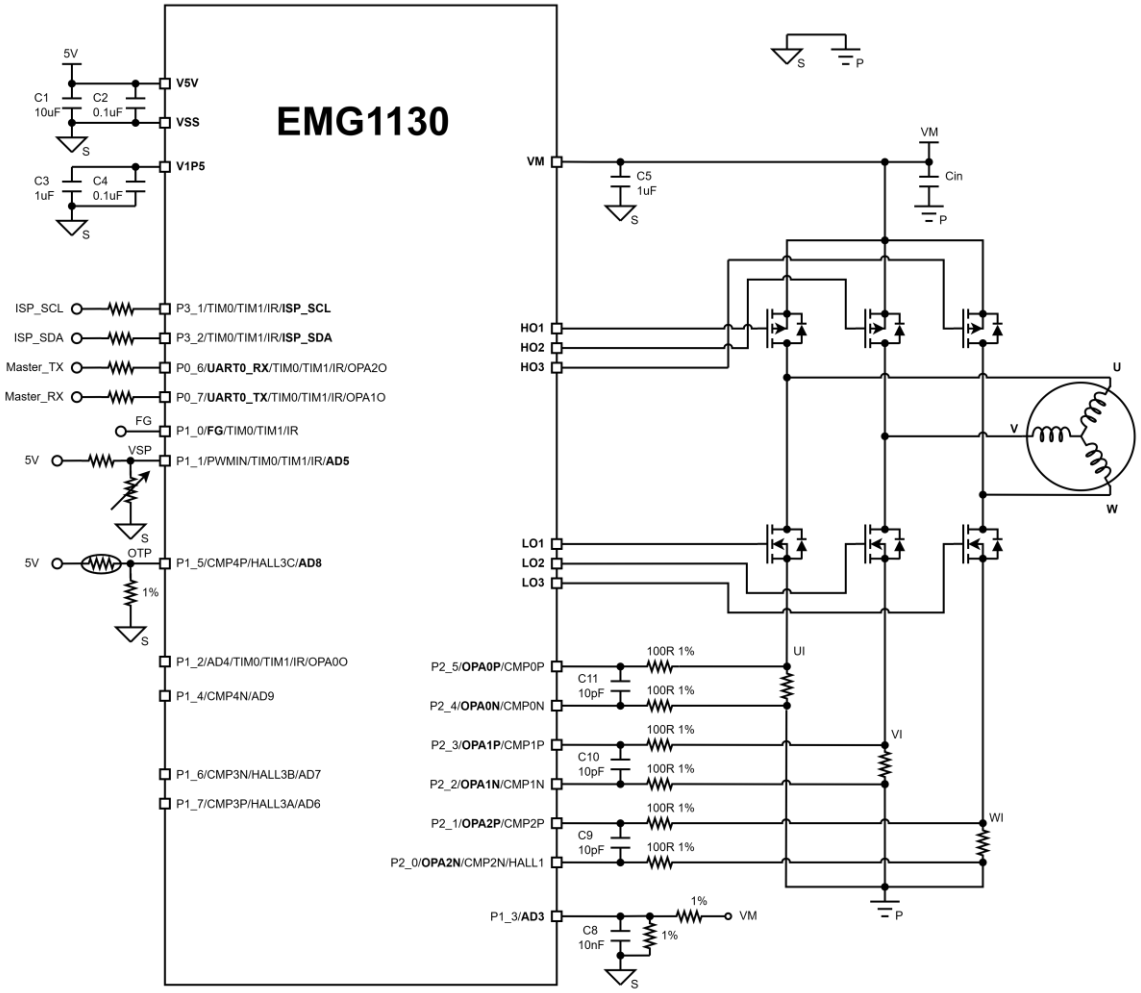


1.4. Applications

- 3-phase fan motor
- Pedestal fan
- Ventilation fan
- Exhaust fan
- Air cleaner
- Humidifiers
- Water pump
- Ceiling fan

1.5. Typical Application

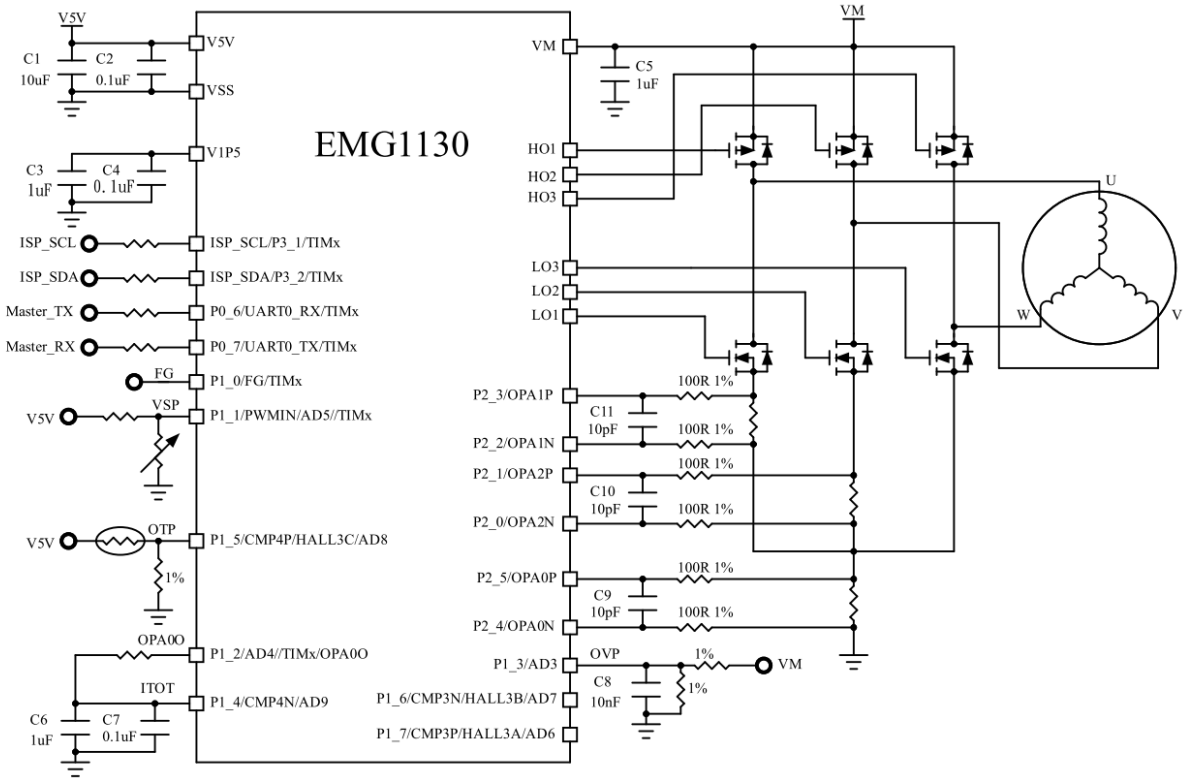
Sensorless + 3 Shunts



Note:

1. C1, C2, C3, C4, and C5 shall be placed as close to the controller as possible.
2. Value 1nF ~ 10nF is recommended for C8.
3. C9 to C11 and six 100R resistors shall be placed as close to the controller as possible.
4. Current sensing wirings shall be differential pairs for each phase from the shunt resistor to the controller.
5. Value 10pF ~ 1nF is recommended for C9 to C11
6. The Power ground(P) and Signal ground(S) are connected by a single point.

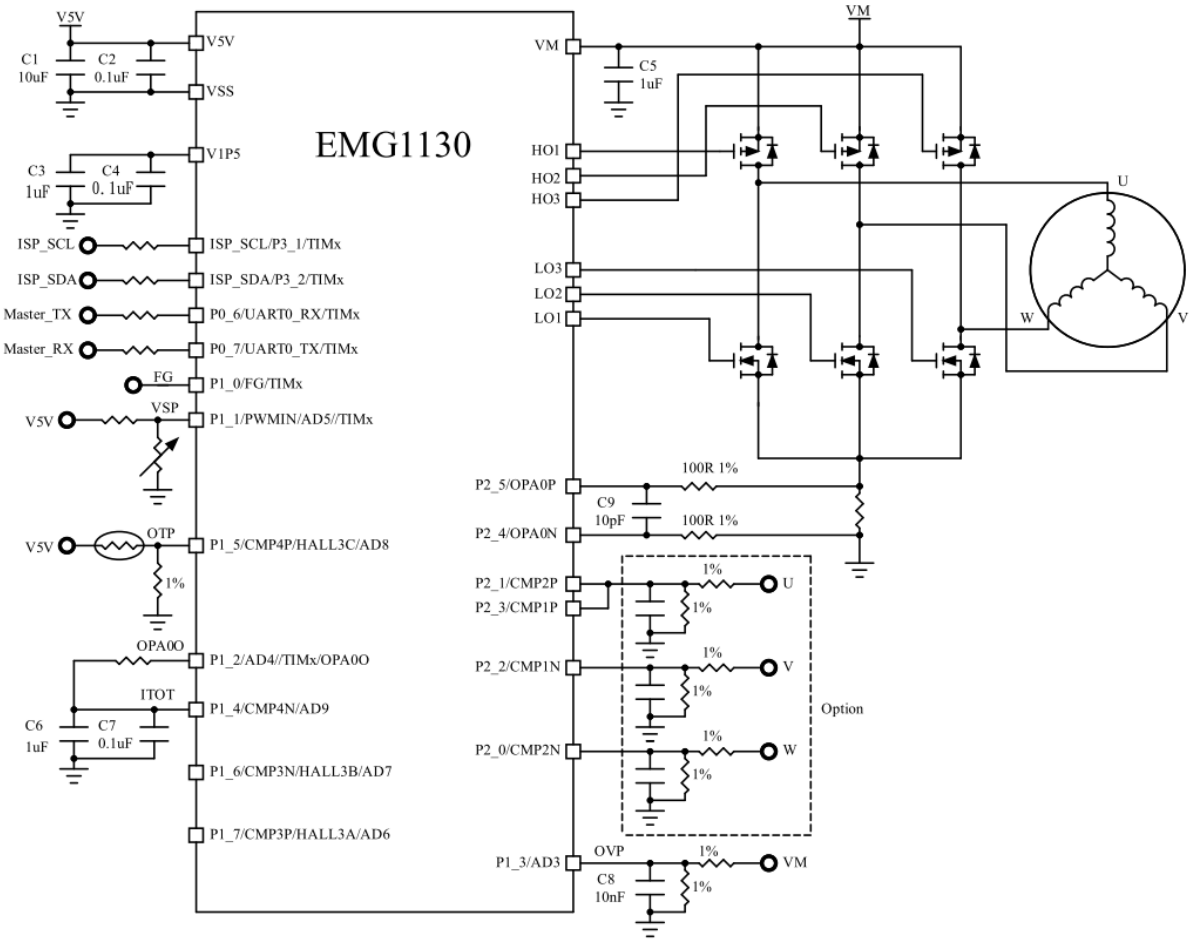
Sensorless + (2+1) Shunts



Note:

1. C1, C2, C3, C4, and C5 shall be placed as close to the controller as possible.
2. Value 1nF ~ 10nF is recommended for C8.
3. C9 to C11 and six 100R resistors shall be placed as close to the controller as possible.
4. Current sensing wirings shall be differential pairs for each phase from the shunt resistor to the controller.
5. Value 10pF ~ 1nF is recommended for C9 to C11

Sensorless + 1 Shunt



Note:

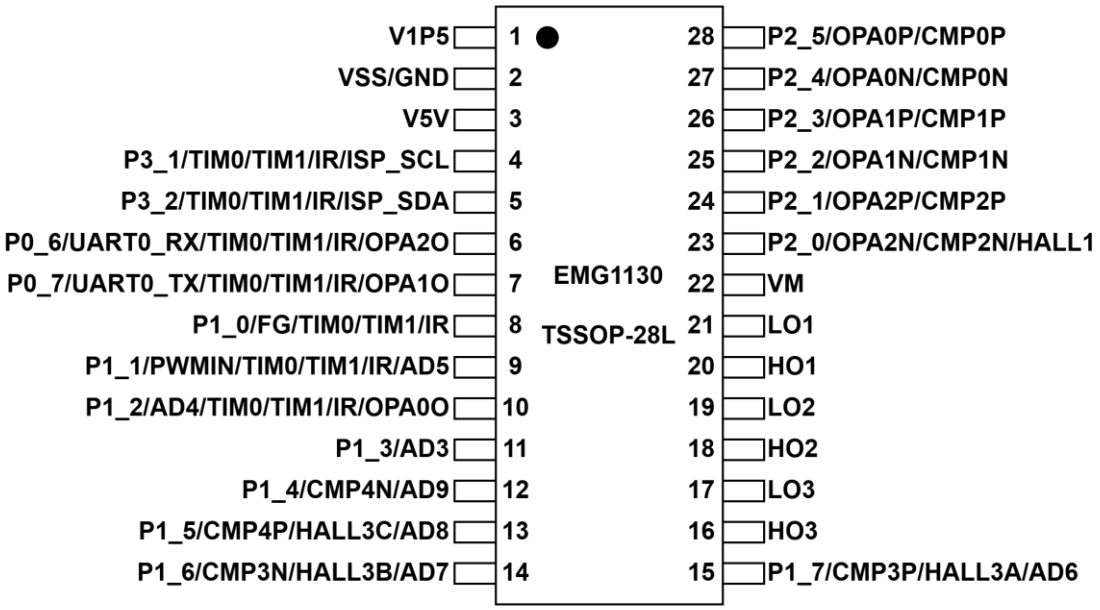
1. C1, C2, C3, C4, and C5 shall be placed as close to the controller as possible.
2. Value 1nF ~ 10nF is recommended for C8.
3. C9 and two 100R resistors shall be placed as close to the controller as possible.
4. Current sensing wirings shall be differential pairs for each phase from the shunt resistor to the controller.
5. Value 10pF ~ 1nF is recommended for C9.

1.6. Pinouts and pin description

The IO Types are defined as follows:

- DIO : Digital input/output pin.
- DI : Digital input pin.
- DO : Digital output pin.
- AI : Analog input pin.
- AO: Analog output pin.
- VI: Voltage input pin.
- VO: Voltage output pin.
- PI : Power Input pin.
- PO : Power output pin.
- GND: Ground pin.
- EP: Exposed Pad

1.6.1. EMG1130-TS28 Pinout



EMG1130 TSSOP-28L Pinout

1.6.2. EMG1130-TS28 Pin descriptions

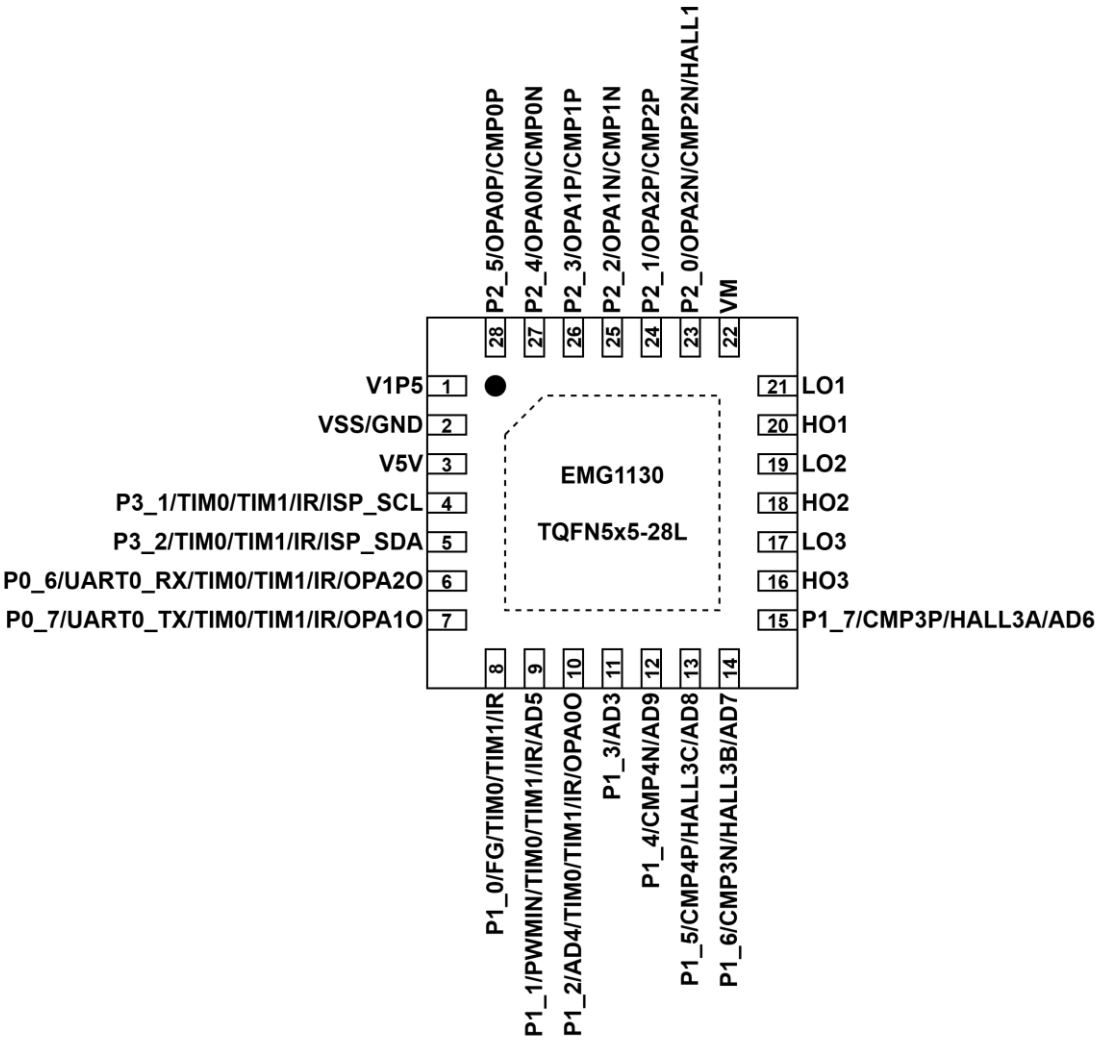
EMG1130 TSSOP-28L Pin Descriptions

Pin	Name	Type	Pin Function
1	V1P5	PO	Core power LDO 1.5V output pin. (for core use only)
2	VSS/GND	GND	Ground of MCU and Gate driver.
3	V5V	PI	5V power input pin.
4	ISP_SCL	DIO	ISP clock pin. [default]
	P3_1	DIO	Pin 1 of GPIO port 3.
	TIM0	DIO	Enhanced timer0 functions I/O
	TIM1	DIO	Enhanced timer1 functions I/O
	IR	DI	IR input function pin
5	ISP_SDA	DIO	ISP data pin. [default]
	P3_2	DIO	Pin 2 of GPIO port 3.
	TIM0	DIO	Enhanced timer0 functions I/O
	TIM1	DIO	Enhanced timer1 functions I/O
	IR	DI	IR input function pin
6	P0_6	DIO	Pin 6 of GPIO port 0.
	UART0_RX	DI	UART0 receiving pin.
	TIM0	DIO	Enhanced timer0 functions I/O
	TIM1	DIO	Enhanced timer1 functions I/O
	IR	DI	IR input function pin
	OPA2_O	AO	OPA2 output (configurable)
7	P0_7	DIO	Pin 7 of GPIO port 0.
	UART0_TX	DO	UART0 transmitting pin.
	TIM0	DIO	Enhanced timer0 functions I/O
	TIM1	DIO	Enhanced timer1 functions I/O
	IR	DI	IR input function pin
	OPA1_O	AO	OPA1 output (configurable)
8	P1_0	DIO	Pin 0 of GPIO port 1.
	FG	DO	FG signal output pin. [Special support as UART0 transmitting pin]
	TIM0	DIO	Enhanced timer0 functions I/O
	TIM1	DIO	Enhanced timer1 functions I/O
	IR	DI	IR input function pin
9	P1_1	DIO	Pin 1 of GPIO port 1.
	PWMIN	DI	PWM signal input pin. [Special support as UART0 receiving pin]

Pin	Name	Type	Pin Function
	TIM0	DIO	Enhanced timer0 functions I/O
	TIM1	DIO	Enhanced timer1 functions I/O
	IR	DI	IR input function pin
	AD5	AI	ADC Channel 5 input pin.
10	P1_2	DIO	Pin 2 of GPIO port 1.
	TIM0	DIO	Enhanced timer0 functions I/O
	TIM1	DIO	Enhanced timer1 functions I/O
	IR	DI	IR input function pin
	AD4	AI	ADC Channel 4 input pin.
	OPA0_O	AO	OPA0 output (configurable)
11	P1_3	DIO	Pin 3 of GPIO port 1.
	AD3	AI	ADC Channel 3 input pin.
12	P1_4	DIO	Pin 4 of GPIO port 1.
	CMP4N	AI	CMP4 N input pin
	AD9	AI	ADC Channel 9 input pin.
13	P1_5	DIO	Pin 5 of GPIO port 1.
	CMP4P	AI	CMP4 P input pin
	AD8	AI	ADC Channel 8 input pin.
	HALL3C	DI	HALL C input pin(3 HALL MODE)
14	P1_6	DIO	Pin 6 of GPIO port 1.
	CMP3N	AI	CMP3 N input pin (configurable)
	AD7	AI	ADC Channel 7 input pin.
	HALL3B	DI	HALL B input pin(3 HALL MODE)
15	P1_7	DIO	Pin 7 of GPIO port 1.
	CMP3P	AI	CMP3 P input pin
	AD6	AI	ADC Channel 6 input pin.
	HALL3A	DI	HALL A input pin(3 HALL MODE)
16	HO3	VO	High side gate driver output of phase C. Connect to PMOS
17	LO3	VO	Low side gate driver output of phase C. Connect to NMOS
18	HO2	VO	High side gate driver output of phase B. Connect to PMOS
19	LO2	VO	Low side gate driver output of phase B. Connect to NMOS
20	HO1	VO	High side gate driver output of phase A. Connect to PMOS
21	LO1	VO	Low side gate driver output of phase A. Connect to NMOS
22	VM	PI	8V~36V power input for P/N gate driver
23	P2_0	DIO	Pin 0 of GPIO port 2
	OPA2N	AI	OPA2 N input pin
	CMP2N	AI	CMP2 N input pin (configurable)

Pin	Name	Type	Pin Function
	HALL1	DI	HALL input pin (1 HALL MODE)
24	P2_1	DI	Pin 1 of GPI port 2. (only input)
	OPA2P	AI	OPA2 P- input pin
	CMP2P	AI	CMP2 P- input pin (configurable)
25	P2_2	DIO	Pin 2 of GPIO port 2.
	OPA1N	AI	OPA1 N- input pin
	CMP1N	AI	CMP1 N- input pin (configurable)
26	P2_3	DI	Pin 3 of GPI port 2. (only input)
	OPA1P	AI	OPA1 P- input pin
	CMP1P	AI	CMP1 P- input pin (configurable)
27	P2_4	DIO	Pin 4 of GPIO port 2.
	OPA0N	AI	OPA0 N- input pin
	CMP0N	AI	CMP0 N- input pin (configurable)
28	P2_5	DI	Pin 5 of GPI port 2. (only input)
	OPA0P	AI	OPA0 P- input pin
	CMP0N	AI	CMP0 N- input pin (configurable)

1.6.3. EMG1130-ND28 Pinout



EMG1130 TQFN5x5-28L Pinout

1.6.4. EMG1130-ND28 Pin descriptions

EMG1130 TQFN5x5-28L Pin Descriptions

Pin	Name	Type	Pin Function
1	V1P5	PO	Core power LDO 1.5V output pin. (for core use only)
2	VSS/GND	GND	Ground of MCU and Gate driver.
3	V5V	PI	5V power input pin.
4	ISP_SCL	DIO	ISP clock pin. [default]
	P3_1	DIO	Pin 1 of GPIO port 3.
	TIM0	DIO	Enhanced timer0 functions I/O
	TIM1	DIO	Enhanced timer1 functions I/O
	IR	DI	IR input function pin
5	ISP_SDA	DIO	ISP data pin. [default]
	P3_2	DIO	Pin 2 of GPIO port 3.
	TIM0	DIO	Enhanced timer0 functions I/O
	TIM1	DIO	Enhanced timer1 functions I/O
	IR	DI	IR input function pin
6	P0_6	DIO	Pin 6 of GPIO port 0.
	UART0_RX	DI	UART0 receiving pin.
	TIM0	DIO	Enhanced timer0 functions I/O
	TIM1	DIO	Enhanced timer1 functions I/O
	IR	DI	IR input function pin
	OPA2_O	AO	OPA2 output (configurable)
7	P0_7	DIO	Pin 7 of GPIO port 0.
	UART0_TX	DO	UART0 transmitting pin.
	TIM0	DIO	Enhanced timer0 functions I/O
	TIM1	DIO	Enhanced timer1 functions I/O
	IR	DI	IR input function pin
	OPA1_O	AO	OPA1 output (configurable)
8	P1_0	DIO	Pin 0 of GPIO port 1.
	FG	DO	FG signal output pin. [Special support as UART0 transmitting pin]
	TIM0	DIO	Enhanced timer0 functions I/O
	TIM1	DIO	Enhanced timer1 functions I/O
	IR	DI	IR input function pin
9	P1_1	DIO	Pin 1 of GPIO port 1.
	PWMIN	DI	PWM signal input pin. [Special support as UART0 receiving pin]

Pin	Name	Type	Pin Function
	TIM0	DIO	Enhanced timer0 functions I/O
	TIM1	DIO	Enhanced timer1 functions I/O
	IR	DI	IR input function pin
	AD5	AI	ADC Channel 5 input pin.
10	P1_2	DIO	Pin 2 of GPIO port 1.
	TIM0	DIO	Enhanced timer0 functions I/O
	TIM1	DIO	Enhanced timer1 functions I/O
	IR	DI	IR input function pin
	AD4	AI	ADC Channel 4 input pin.
	OPA0_O	AO	OPA0 output (configurable)
11	P1_3	DIO	Pin 3 of GPIO port 1.
	AD3	AI	ADC Channel 3 input pin.
12	P1_4	DIO	Pin 4 of GPIO port 1.
	CMP4N	AI	CMP4 N input pin
	AD9	AI	ADC Channel 9 input pin.
13	P1_5	DIO	Pin 5 of GPIO port 1.
	CMP4P	AI	CMP4 P input pin
	AD8	AI	ADC Channel 8 input pin.
	HALL3C	DI	HALL C input pin(3 HALL MODE)
14	P1_6	DIO	Pin 6 of GPIO port 1.
	CMP3N	AI	CMP3 N input pin (configurable)
	AD7	AI	ADC Channel 7 input pin.
	HALL3B	DI	HALL B input pin(3 HALL MODE)
15	P1_7	DIO	Pin 7 of GPIO port 1.
	CMP3P	AI	CMP3 P input pin
	AD6	AI	ADC Channel 6 input pin.
	HALL3A	DI	HALL A input pin(3 HALL MODE)
16	HO3	VO	High side gate driver output of phase C. Connect to PMOS
17	LO3	VO	Low side gate driver output of phase C. Connect to NMOS
18	HO2	VO	High side gate driver output of phase B. Connect to PMOS
19	LO2	VO	Low side gate driver output of phase B. Connect to NMOS
20	HO1	VO	High side gate driver output of phase A. Connect to PMOS
21	LO1	VO	Low side gate driver output of phase A. Connect to NMOS
22	VM	PI	8V~36V power input for P/N gate driver
23	P2_0	DIO	Pin 0 of GPIO port 2
	OPA2N	AI	OPA2 N input pin
	CMP2N	AI	CMP2 N input pin (configurable)

Pin	Name	Type	Pin Function
	HALL1	DI	HALL input pin (1 HALL MODE)
24	P2_1	DI	Pin 1 of GPI port 2. (only input)
	OPA2P	AI	OPA2 P- input pin
	CMP2P	AI	CMP2 P- input pin (configurable)
25	P2_2	DIO	Pin 2 of GPIO port 2.
	OPA1N	AI	OPA1 N- input pin
	CMP1N	AI	CMP1 N- input pin (configurable)
26	P2_3	DI	Pin 3 of GPI port 2. (only input)
	OPA1P	AI	OPA1 P- input pin
	CMP1P	AI	CMP1 P- input pin (configurable)
27	P2_4	DIO	Pin 4 of GPIO port 2.
	OPA0N	AI	OPA0 N- input pin
	CMP0N	AI	CMP0 N- input pin (configurable)
28	P2_5	DI	Pin 5 of GPI port 2. (only input)
	OPA0P	AI	OPA0 P- input pin
	CMP0N	AI	CMP0 N- input pin (configurable)
EP	Exposed Pad	EP	Connected to Ground

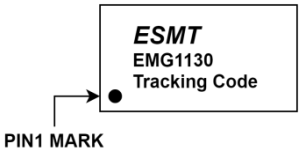
1.7. Ordering Information

Product ID	Package Type	Packing / MPQ	Comments
EMG1130-TS28NBR	TSSOP-28L	2500 Units / Reel	Green
EMG1130-ND28NBR	TQFN5x5-28L	5000 Units / Reel	Green

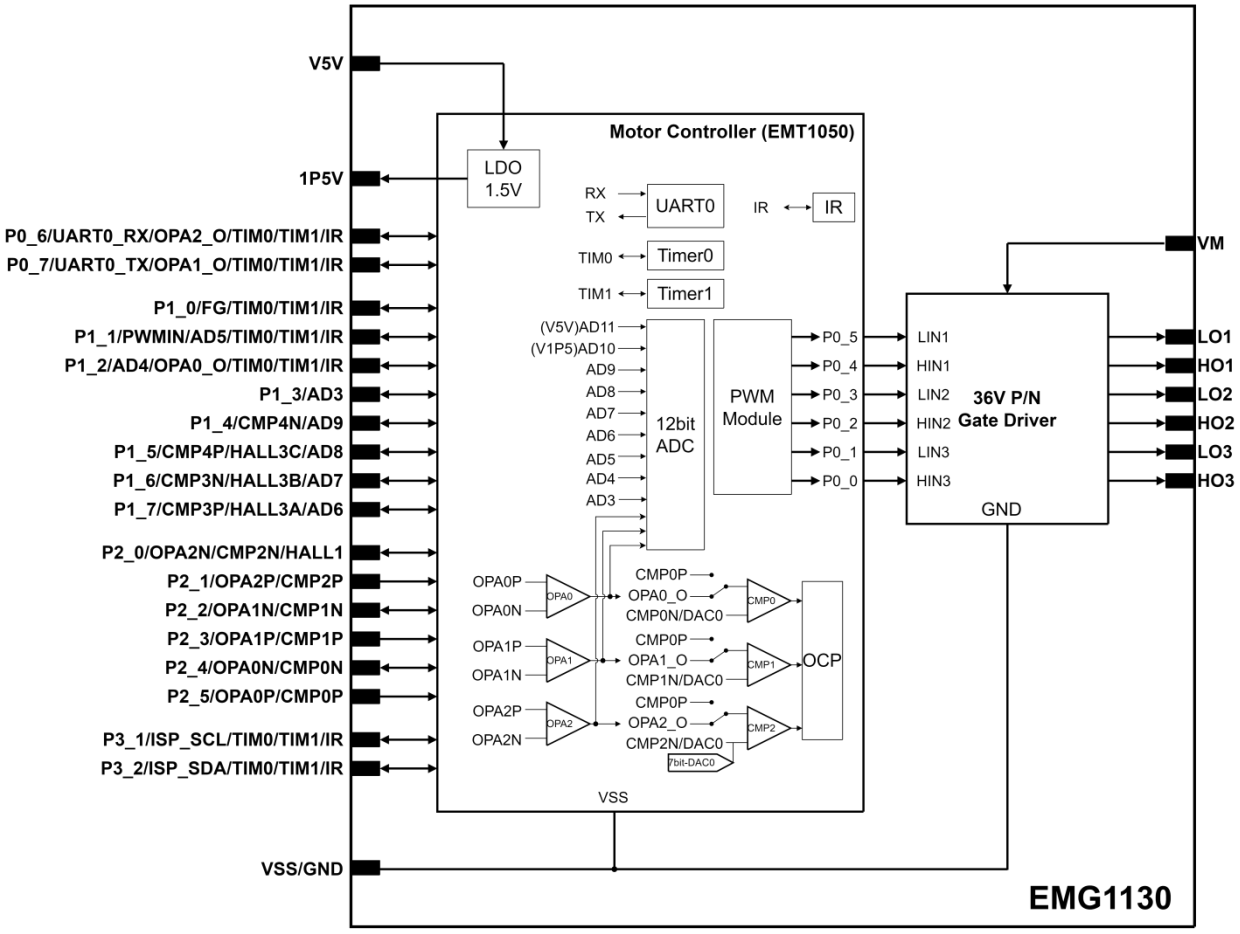
1.8. Marking Information

EMG1130

Line 1 : LOGO
Line 2 : Product No.
Line 3 : Tracking Code



1.9. EMG1130 Block Diagram



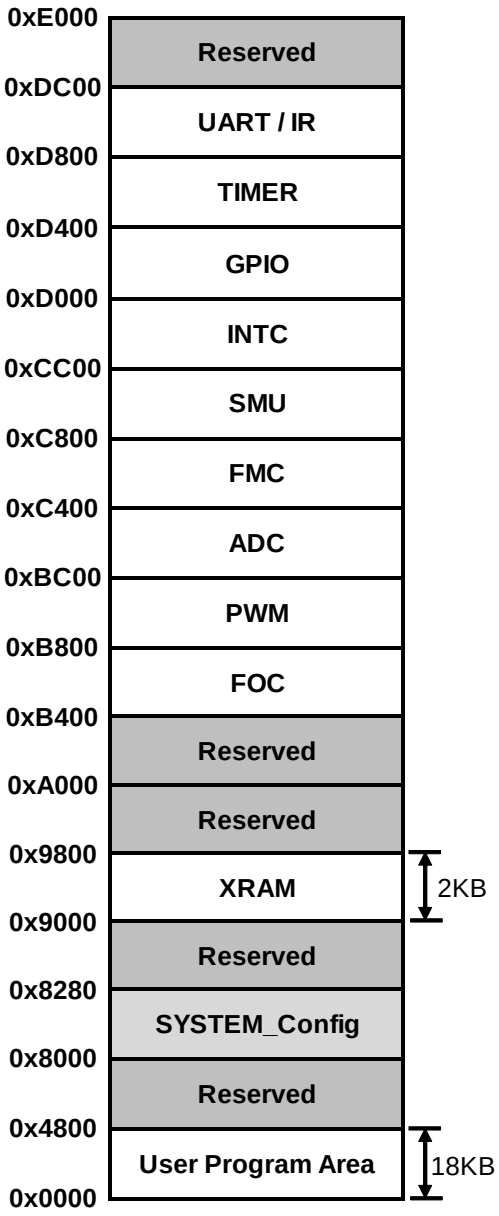
1.10. Memory map

SFRs Memory Map:

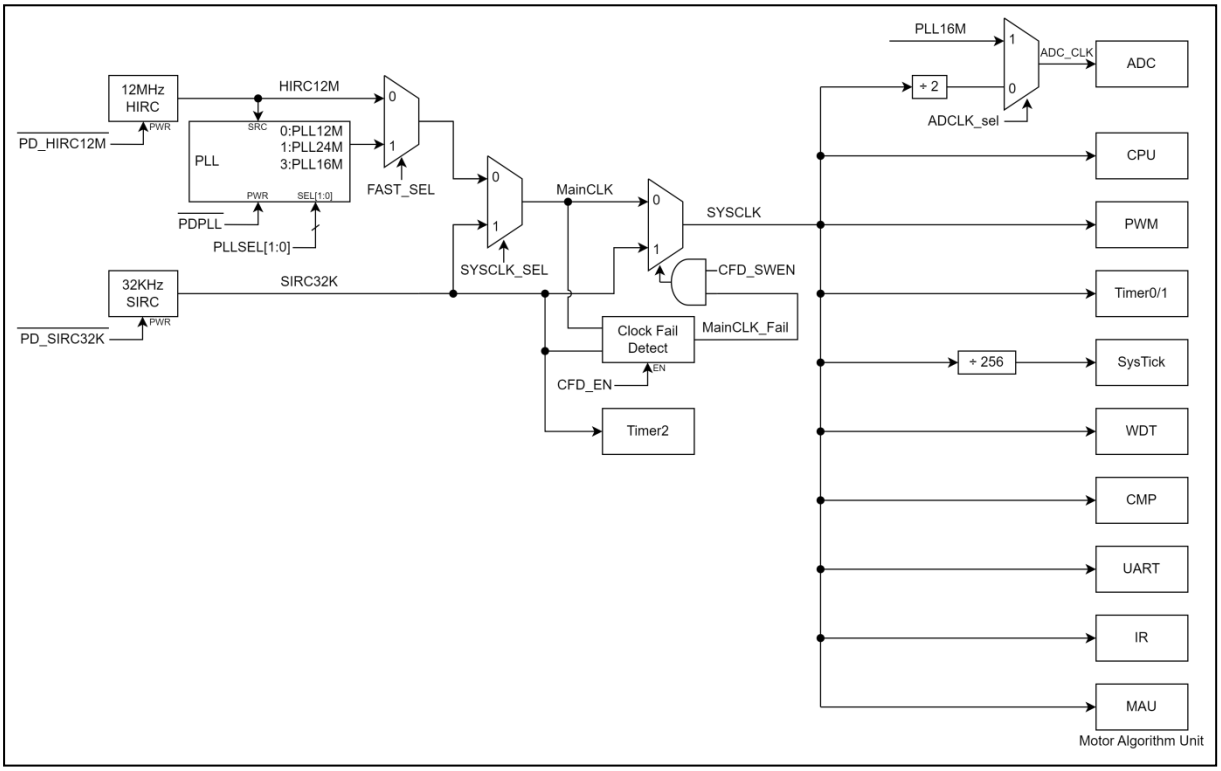
F8H									FFH
F0H	B								F7H
E8H		RX_DATA_35	RX_DATA_36	RX_DATA_37	RX_DATA_38	RX_DATA_39			EFH
E0H	ACC	RX_DATA_28	RX_DATA_29	RX_DATA_30	RX_DATA_31	RX_DATA_32	RX_DATA_33	RX_DATA_34	E7H
D8H		RX_DATA_21	RX_DATA_22	RX_DATA_23	RX_DATA_24	RX_DATA_25	RX_DATA_26	RX_DATA_27	DFH
D0H	PSW	RX_DATA_14	RX_DATA_15	RX_DATA_16	RX_DATA_17	RX_DATA_18	RX_DATA_19	RX_DATA_20	D7H
C8H		RX_DATA_7	RX_DATA_8	RX_DATA_9	RX_DATA_10	RX_DATA_11	RX_DATA_12	RX_DATA_13	CFH
C0H		RX_ATA_0	RX_DATA_1	RX_DATA_2	RX_DATA_3	RX_DATA_4	RX_DATA_5	RX_DATA_6	C7H
B8H		TX_DATA_35	TX_DATA_36	TX_DATA_37	TX_DATA_38	TX_DATA_39			BFH
B0H	P3	TX_DATA_28	TX_DATA_29	TX_DATA_30	TX_DATA_31	TX_DATA_32	TX_DATA_33	TX_DATA_34	B7H
A8H		TX_DATA_21	TX_DATA_22	TX_DATA_23	TX_DATA_24	TX_DATA_25	TX_DATA_26	TX_DATA_27	AFH
A0H	P2	TX_DATA_14	TX_DATA_15	TX_DATA_16	TX_DATA_17	TX_DATA_18	TX_DATA_19	TX_DATA_20	A7H
98H		TX_DATA_7	TX_DATA_8	TX_DATA_9	TX_DATA_10	TX_DATA_11	TX_DATA_12	TX_DATA_13	9FH
90H	P1	TX_DATA_0	TX_DATA_1	TX_DATA_2	TX_DATA_3	TX_DATA_4	TX_DATA_5	TX_DATA_6	97H
88H							DPPL	DPPH	8FH
80H	P0	SP	DPL	DPH					87H

Note: No reserved for user define.

XSFRs Memory Map:



1.11. Clock Block Diagram



2. Electrical Specifications

2.1. Absolute Maximum Ratings (Note1,2)

Supply Input Voltage, V5V	-0.3V to +5.8V	Storage Temperature Range	-55°C to 150 °C
Supply Input Voltage, VM	40V	Junction Temperature (T_J)	150 °C
PAD P2_1, P2_3, P2_5	-1.2V to +5.8V	ESD Rating (Note3)	
PAD HO1, HO2, HO3	VM-6V to VM+1V	Human Body Model	2KV
PAD LO1, LO2, LO3	-1V to 6V	Lead Temperature (Soldering,	260°C
I/O pins	-0.3V to 5.8V	10 sec.)	

2.2. Recommended Operating Conditions (Note1,2)

Supply Input Voltage, V5V	4.5V to 5.5V	Junction Temperature Range	-40°C to 125 °C
Supply Input Voltage, VM	8V to 36V	Ambient Temperature Range	-40°C to 105 °C
LDO capacitor on V5V	10μF+0.1uF		
LDO capacitor on V1P5	1μF+0.1uF		
Voltage of I/O Pin to GND	-0.3V to V_{V5V}+0.3V		
Analog Input Voltage	-0.3V to V_{V5V}+0.3V		

2.3. Electrical Characteristics

V_{V5V}=5V, VM=24V, T_A=25°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Motor Controller						
-Clock Section						
System Frequency	f_{SCLK}		12	24	--	MHz
Internal RC Oscillator						
Internal High RC Oscillator	f_{HIRC}		11.76	12	12.24	MHz
Internal Slow RC Oscillator	F_{SIRC}		24	32	45	KHz
-PLL Section						
PLL 24MHz Clock	f_{PLL24M}		23.52	24	24.48	MHz
-Power Management Section						
Supply input of V5V	V_{V5V}		4.5	5.0	5.5	V
Turn-On Voltage of V5V	V_{V5V_ON}	According to LVR or UVLO configuration, maximum between V_{LVR} and V_{UVLO}	--	V_{LVR} Or V_{UVLO}	--	V
V5V On-Off Hysteresis	V_{V5V_HYS}	Turn-off voltage = V_{V5V_ON} - V_{V5V_hys}	--	0.05	--	V
LVR **(Note 4)**	V_{LVR}		-3%	2.8	+3%	V
UVLO Level(4 level select)	V_{UVLO}	UVL_LEVEL: 00: 2.7V 01: 3.0V 10: 3.7V 11: 4.3V	-3%	- 2.7 3.0 3.7 4.3	+3%	V
V5V Current at Operation Mode	I_{V5V_OPER}	Typical sensor-less motor control mode	--	18	--	mA
V5V Current at Deep Sleep Mode	I_{V5V_DSLP}		--	200	--	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
-Internal 1.5V LDO (for core use only)						
LDO voltage for Internal Operation	V_{V1P5}	CL=0.1uF, IL=0mA	--	1.55	--	V
Line Regulation		CL=0.1uF, IL=0mA	--	--	10	mV
Support current			--	--	30	mA
-ADC Section (0V to 5V, 12-Bit, Single End Mode, Gain = 1) **(Note5)**						
ADC Input Voltage Range	V_{ADCIN}		0	--	V_{V5V}	V
Clock		ADC CLK=SYSCLK/2	6	12	16	MHz
Conversion Rate		16T ADC CLK	--	0.75	1	MSPS
Channel			--	12	--	
-Current Limit Comparator Section (CMP0/CMP1/CMP2, CMP3 option) **(Note5)**						
Input Range	V_{IN}		0.1	--	V_{V5V} - 0.625	V
Comparator Offset	V_{OFFSET}		-15	--	15	mV
Comparator Reference	V_{th}	7bit selection	0.039	--	0.875 x V_{V5V}	V
-General Purposed Comparator (CMP1/CMP2/CMP3/CMP4) **(Note5)**						
Input Range	V_{IN}		0	--	V_{V5V} - 0.625	V
Comparator Offset	V_{OFFSET}		-15	--	15	mV
-OPAMP (internal) **(Note 5)**						
Input Range(vofs<1mV)	V_{IN}		0	--	4.3	V
Output Range			0.05	--	4.95	V
Input Offset	V_{OFFSET}	Vout=2.5V	--	--	10	mV
Offset Bias adjust	$V_{OFFBIAS}$	VREF= V_{V5V} = 5V	--	VREF/2 VREF/80	--	V
-I/O of P0_0 to P0_7 , P1_0 to P1_7,P3_1 to P3_2 , P2_0, P2_2, P2_4 section						
Input High Voltage	V_{IH}		0.7 x V_{V5V}	--	--	V
Input Low Voltage	V_{IL}		--	--	0.3 x V_{V5V}	V
Pull-Up Resistor	R_{PD}		20	--	100	kΩ
Pull-Down Resistor	R_{DOWN}		20	--	100	kΩ
High Level Output Current	I_{OH}	@ 0.8 x V_{V5V}	--	15	--	mA
Low Level Output Current	I_{OL}	@ 0.2 x V_{V5V}	--	15	--	mA
-I/O of P2_1, P2_3, P2_5 section						
Input High Voltage	V_{IH}	Without internal Pull-up and Pull-down resistor	0.7 x V_{V5V}	--	--	V
Input Low Voltage	V_{IL}	Without internal Pull-up and Pull-down resistor	--	--	0.3 x V_{V5V}	V
Pull-Up Resistor	R_{PD}		20	--	100	kΩ
Pull-Down Resistor	R_{DOWN}		20	--	100	kΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
High Level Output Current	I_{OH}	@ 0.8 x V_{V5V}	--	15	--	mA
Gate Driver						
-POWER SUPPLIE						
Standby current	$I_{STANDBY}$	HINx=0, LINx=0	--	50	100	μA
Operation current	I_{VM}	HINx=0, LINx=1	--	220	400	μA
		HINx=1, LINx=0	--	270	400	μA
-Resistance						
Input pull-down resistance	R_{PD}		--	200	--	kΩ
Output resistance	R_{OH}	HINx=0, HOx=VM-0.2V	--	3	--	Ω
Output resistance	R_{OL}	LINx=0, LOx=0.2V	--	2	--	Ω
-Drive current						
High side source current	I_{H_ON}	HINx=1, HOx=VM	--	100	--	mA
High side sink current	I_{H_OFF}	HINx=0, HOx=VM-5V	--	100	--	mA
Low side source current	I_{L_ON}	LINx=1, LOx=0	--	100	--	mA
Low side sink current	I_{L_OFF}	LINx=0, LOx=5V	--	100	--	mA
-Timing						
Low side rising output rise	T_{LR}		--	52	--	ns
Low side falling output fall	T_{LF}		--	36	--	ns
High side rising output rise	T_{HR}		--	75	--	ns
High side falling output fall	T_{HF}		--	50	--	ns
-PROTECTIONS						
Internal dead time	T_D		--	150	--	ns
Under voltage lock out	UVLO		1.3	1.8	2.2	V

Note 1: Absolute maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device out of its rated operating conditions.

Note 2: All voltages are with respect to the potential at the ground pin.

Note 3: Devices are ESD sensitive. Handling precaution is recommended.

Note 4: Only default as 2.8V for LVR.

Note 5: Characterized, not tested at manufacturing.

3. Motor Controller Description

3.1. Core

The core of the EMG1130 is the high-performance 8051 processor, and capable of running at speed up to 24MHz.

3.2. Flash and RAM

The EMG1130 embedded 18KB Flash program memory, 256B of IRAM, and 2KB of XRAM memory for storing user application code and data.

3.3. Code Protection

The EMG1130 provides users with the ability to enable flash protection to protect the code area. This can be enabled by call function from Library or the ESMT link tool.

3.4. Cyclic Redundancy Check (CRC)

CRC is a calculation method that divides this message polynomial by a constant called the generating polynomial. (the polynomial $F(x) = X^{16} + X^{12} + X^5 + 1$ given in ISO/IEC13239, CRC16-CCITT-False). It offers a mechanism only for validating storage errors in flash memory with CRC-16.

UART module also provides an encoding mode and a check mode with CRC-8, and users can define the polynomial function.

3.5. Power Supply

The supply voltage V_{V5V} of controller ranges from 4.5V to 5.5V. All input/output (I/O) and internal voltage regulators are powered via the V_{V5V} pin externally.

3.6. LVR/POR/UVL

The EMG1130 integrates the Power-On Reset (POR) and Low-Voltage Reset (LVR) functions to ensure the system stability and initiates a reset when the voltage exceeds a threshold of 2.8V. Additionally, to prevent frequency reduction or erroneous data registration in low-voltage scenarios, the Under-Voltage Lockout (UVLO) feature employs programmable software to monitor voltage levels. It interrupts the system operation when the voltage drops below the preset threshold, providing the software with an opportunity to address the voltage anomaly.

3.7. Unique ID(UID)

The EMG1130 includes EMT1050 controller, and has the same chip identification value that is a constant value, and read from address 0xC818.

3.8. Vectored Interrupt Controller (VIC)

Interrupt source	Default Priority	Vector Address	Flag bit	Software Clear	Enable bit
Reset	Highest	0x0000	N/A	N/A	Keep on
PWM period interrupt [INT_PWM_RELOAD]	0	0x0003	IF0[0]	Y	IE0[0]
OCP detect, PWM braked interrupt [INT_PWM_BREAK] **(Note6)**	1	0x000B	IF0[1]	Y	IE0[1]
$I_a/I_b/I_c$ phase current convert done interrupt [INT_ADC_CURRENT]	2	0x0013	IF0[2]	Y	IE0[2]
AD3~AD5 and Itot auto convert done interrupt [INT_ADC_SEQ] **(Note7)**	3	0x001B	IF0[3]	Y	IE0[3]
INT_UART0_TX	4	0x0023	IF0[4]	Y	IE0[4]
INT_UART0_RX	5	0x002B	IF0[5]	Y	IE0[5]
TIMER0 interrupt [INT_TIMER0]	6	0x0033	IF0[6]	Y	IE0[6]
TIMER1 interrupt [INT_TIMER1]	7	0x003B	IF0[7]	Y	IE0[7]
CMP3 interrupt [INT_CMP3]	8	0x0043	IF1[0]	Y	IE1[0]
CMP4 interrupt [INT_CMP4]	9	0x004B	IF1[1]	Y	IE1[1]
Reserved	10	0x0053	IF1[2]	N/A	IE1[2]
TIMER2 interrupt [INT_TIMER2]	11	0x005B	IF1[3]	Y	IE1[3]
Under Voltage Lock-out interrupt [INT_UVL_ACTIVE]	12	0x0063	IF1[4]	Y	IE1[4]
System clock fail interrupt [INT_SYSCLK_FAIL]	13	0x006B	IF1[5]	Y	IE1[5]
Reserved	14	0x0073	IF1[6]	N/A	IE1[6]
Reserved	15	0x007B	IF1[7]	N/A	IE1[7]

The EMG1130 provides 13 interrupt sources as shown in the table above. In this table, lower priority number indicates higher priority.

Note6: H/W shunt OCP protected event.

Note7: Only one channel converted in one PWM period.

3.9. System Reset

The EMG1130 has 4 reset sources: low-voltage reset (LVR), power-on reset (POR), under-voltage lockout reset (UVLR), and watchdog timer reset (WDT). The reset enable references are related to configuration registers, where the EN_AUVLRST and WDT_ON control bits respectively enable the UVLR and WDT reset sources.

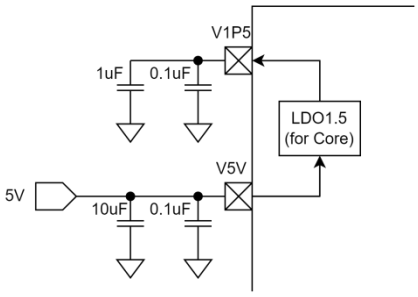
3.10. Clock

- 12MHz High speed Internal RC Oscillator (HIRC)
- 24~45KHz Slow speed Internal RC Oscillator (SIRC)
- 24MHz internal PLL (PLL)

While system reset and startup, the High speed Internal RC Oscillator is selected as default system clock.

3.11. Voltage Regulator

The voltage regulator powers the internal circuitry and the external VCAP capacitors are required.



3.12. Power Mode

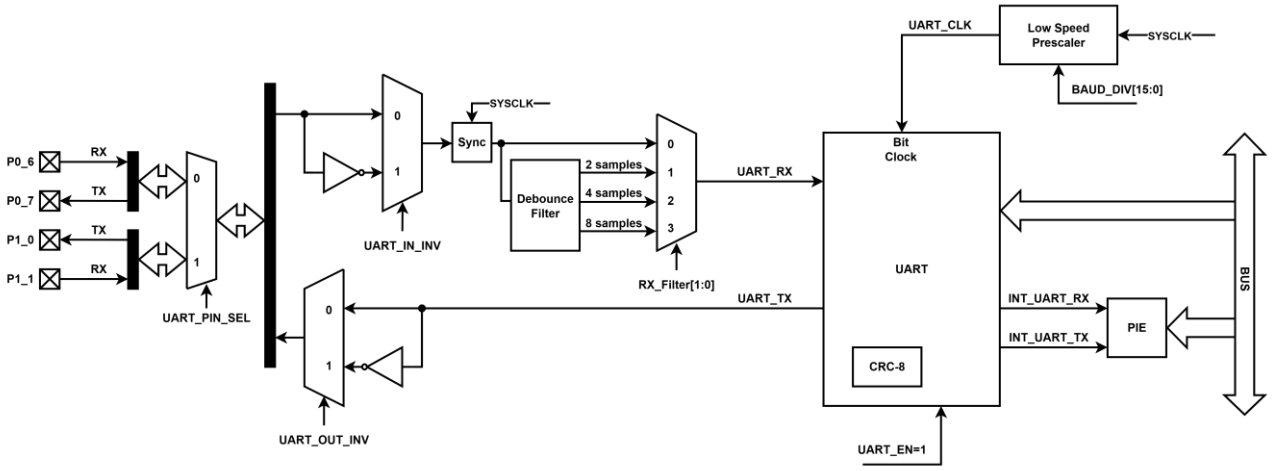
The controller supports 2 working modes:

- Operation mode: the CPU core and peripheral modules continue to operate.
- Deep-sleep mode: the main clock is turned off. The CPU core is halted. The peripheral modules shall be powered down manually by selecting the appropriate function before entering deep sleep.

While in the Deep-sleep mode, the controller can be awakened via a specific pin. During normal operation, users have options to operate in different config based on user: such as turn off the clock, or power down the unused peripherals, allowing for flexible switching between power consumption and performance.

3.13. Universal Asynchronous Receiver/Transmitter (UART0)

The UART0 is a computer hardware device designed for asynchronous serial communication with configurable CRC-8 and transmission speed. It transmits data bit by bit individually, starts from the least significant bit(LSB) to the most significant bit(MSB), and be framed by a start and a stop bit to ensure precise timing management by the communication channel. The controller controller has one UART module (UART0).



- Tx or Rx signal invert Support
- Baud rate programmable
- Data-byte format
  - One start bit
  - Eight data bits
  - no parity bit
  - One stop bit
- Half-Duplex/Full-Duplex support
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
- 40byte TX data buffers
- 40byte RX data buffers
- CRC-8 support, provides a programmable polynomial and uses 0x00 or 0xFF as the initial value for CRC-8 data.

3.14. Timers and Watchdog

The EMG1130 includes 2 enhanced timer, 1 basic timer, 1 system tick timer and 1 watchdog timer.

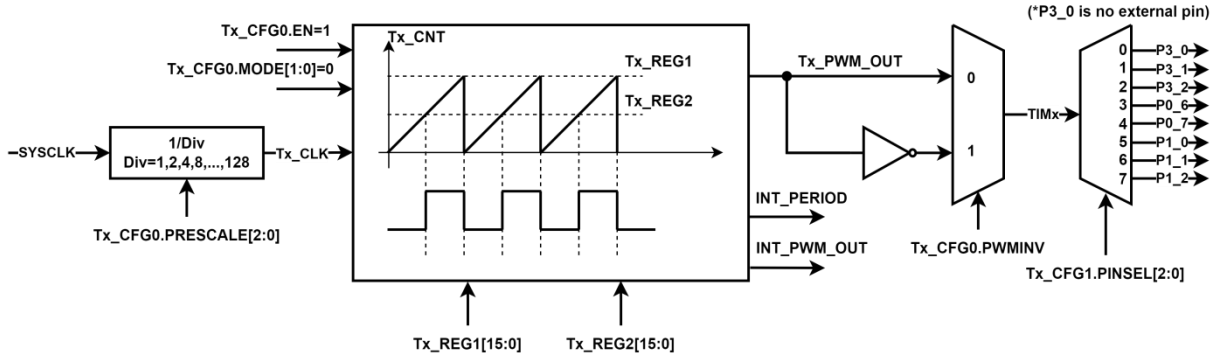
Timer and Watchdogs								
Timer Type	**Name**	**Clock Src.**	**Counter**	**Pre-scaler**	**Counting Dir.**	**Interrupt**	**PWM**	**Capture Compare Channel**
Enhanced	Timer0	Sysclk	16 bits	1/2/4/8/16/32/64/128	Inc.	Yes	Yes	Yes
Enhanced	Timer1	Sysclk	16 bits	1/2/4/8/16/32/64/128	Inc.	Yes	Yes	Yes
Basic	Timer2	SIRC	8 bits	No	Inc.	Yes	No	No
System tick	SysTick	Sysclk	16 bits	256 fixed	Inc.	No	No	No
Watchdog	WDT	Sysclk	16 bits	8 bits	Inc.	Yes	No	No

-Enhanced Timer (Timer0/1)

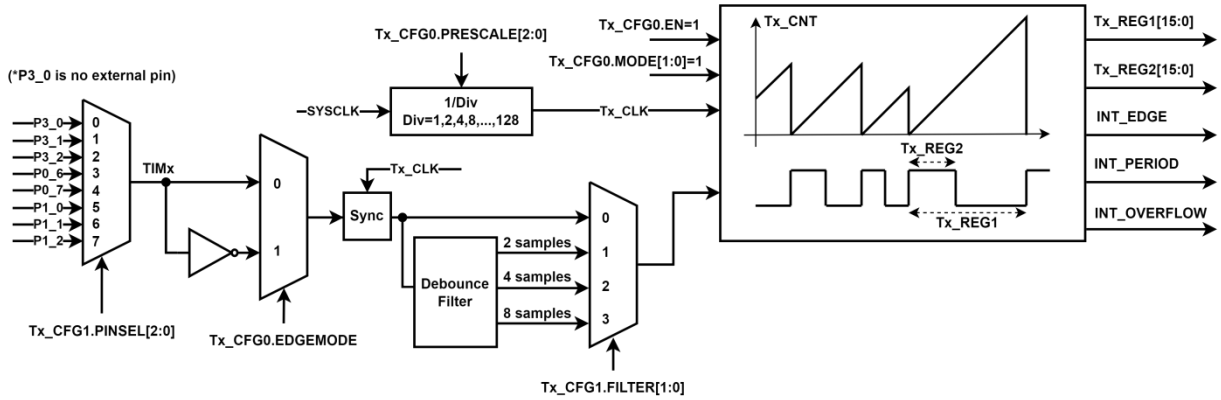
Timer0/1 each has an independent 16-bit advanced counter with automatic reload. The counting source of the counter is the system clock. Timer0/1 has the following features:

1. 16-bit up counter with automatic reload, the reload function can also be turned off.
2. 8 programmable pre-scalers.
3. Three modes of application are available:
   a) PWM generator or Timer only.
   b) Capture.
   c) Counter.
4. Interrupt event:
   a) Period interrupt.
   b) PWM out interrupt.
   c) Edge trigger interrupt.
   d) Match count interrupt.
   e) Overflow interrupt.
5. 8 input sources can switch for capture/counter.
6. 8 output pins can switch for PWM generator.
7. Edge detection.
8. 4 input filter sampling options.

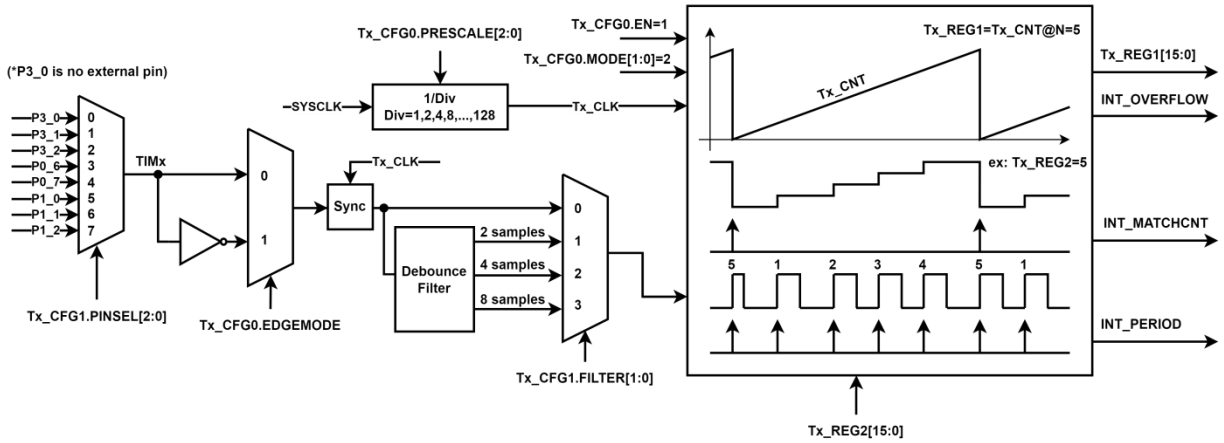
PWM generator Mode: (x=0,1)



Capture Mode: (x=0,1)

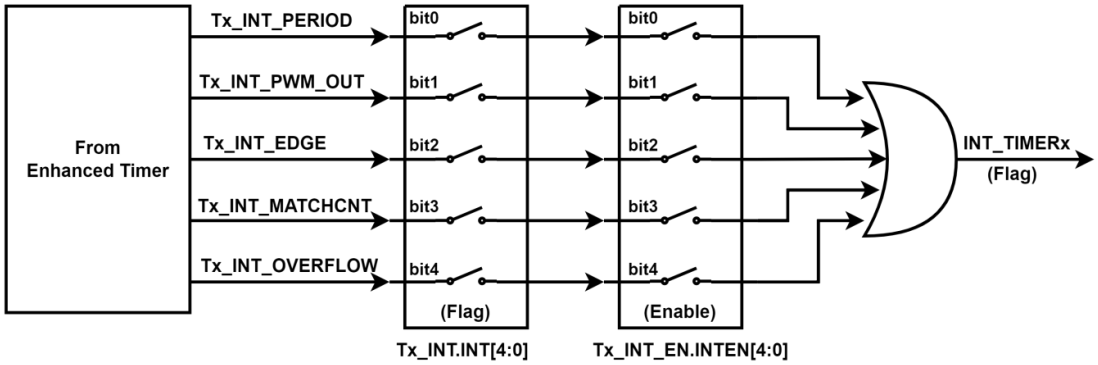


Counter Mode: (x=0,1)



INT_TIMER Interrupt relations: (x=0,1)

To clear the INT_TIMERx flag, you must also clear the enhanced timer's interrupt flag.



-Basic Timer (Timer2)

Timer2 is an 8-bit timer comprised of an 8-bit register: T2_CNT. It operates in a flexible 8-bit auto-reload mode, utilizing an 8-bit register: T2_PERIOD.

-System Tick Timer (SysTick)

SysTick is a 16-bit system tick timer up counter driven by system clock. The system tick timer operates of the main clock with automatic reload, and divided by 256.

-Watchdog Timer (WDT)

The WDT is a 16-bit up counter driven by the WDT_CLK. The WDT_CLK operates independently of the main clock. This watchdog can function as a safety mechanism to reset the device in case of CPU malfunctions, or function as a free-running timer for timeout management.

WDT_CLK = SYS_CLK/(4n+1), n=0~255

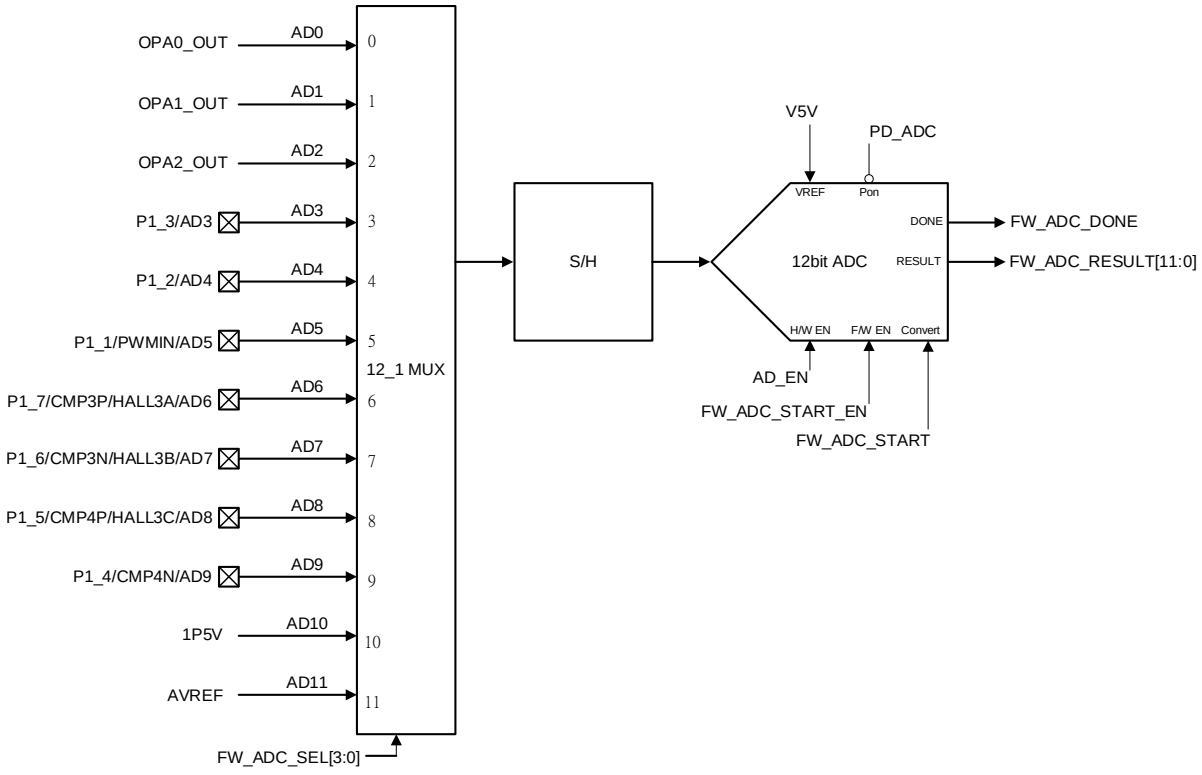
3.15. General Purpose Input/Output (GPIO)

1. The P0[7:0], P1[7:0], P2[5:0] and P3[2:1] registers are mapping to I/O pins P0_0~P0_7, P1_0~P1_7, P2_0~P2_5 and P3_1~P3_2 respectively.
2. PORT0_OE, PORT1_OE, PORT2_OE and PORT3_OE registers are used to configure the logic output enable settings of P0_0~P0_7, P1_0~P1_7, P2_0~P2_5 and P3_1~P3_2. However, for P2_1, P2_3, and P2_5, if set as output enable, they support source output function only and cannot support sink output.
3. PORT0_OD, PORT1_OD, PORT2_OD, and PORT3_OD registers are used to configure the output open-drain mode for P0_0~P0_7, P1_0~P1_7, P2_0, P2_2, P2_4, and P3_1~P3_2. By default [value: 0], they operate in push-pull mode. For P2_1, P2_3, and P2_5 pins, there are no output open-drain mode.
4. PORT0_IE, PORT1_IE, PORT2_IE, and PORT3_IE registers are used to configure the logic input enable settings for P0_0~P0_7, P1_0~P1_7, P2_0~P2_5, and P3_1~P3_2.
5. All ports can be enabled weak pull-up via PORT0_PU, PORT1_PU , PORT2_PU and PORT3_PU.
6. All ports can be enabled weak pull-down via PORT0_PD, PORT1_PD, PORT2_PD, and PORT3_PD.
7. P0_6, P0_7, P1_0~P1_7, and P2_0~P2_5 pins are multi-function pins with analog input of ADC, OPAMP, and comparator. Each analog module has an Enable register to enable the function or not.
8. P3_1, P3_2 are default as dedicated function for ISP_SCL, and ISP_SDA. RSTN_I2C_GPIO register can define them to GPIO function.
9. The PWM_HL_EN register controls the three-phase outputs AH/BH/CH and AL/BL/CL. These outputs are from P0_0 to P0_5. And P0_0 to P0_5 are internal connected for 36V P/N gate driver.

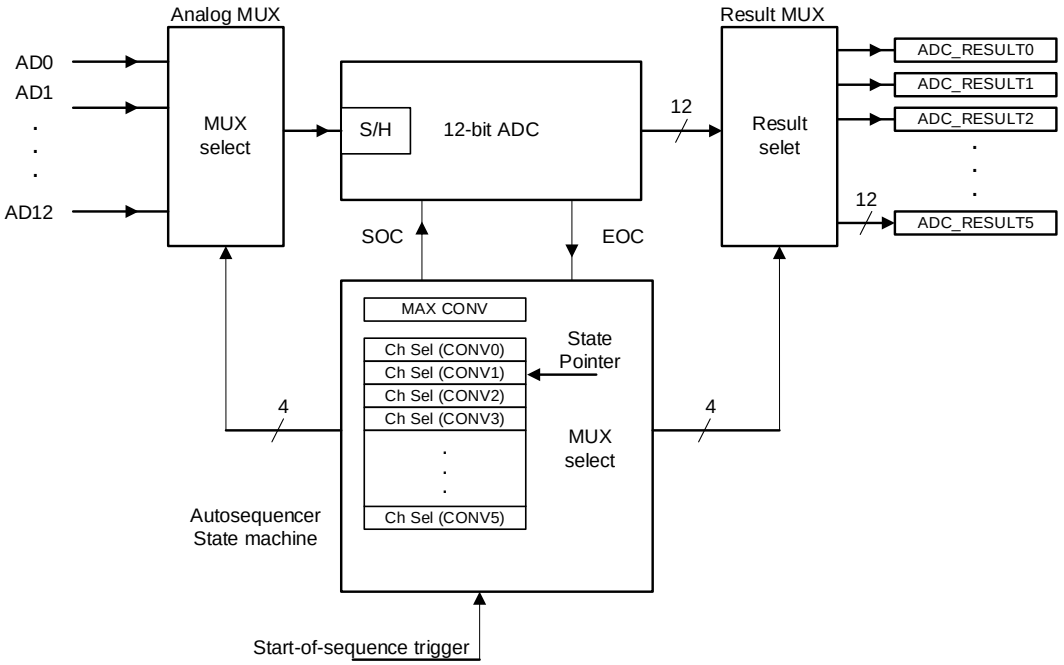
3.16. Analog to Digital Converter (ADC)

In the EMG1130, there is a 12-bit 12 channels SAR ADC. AD0/AD1/AD2 are connected to the outputs of internal operational amplifiers, AD10 is connected to the internal core voltage, and AD11 is connected to the internal AVREF voltage. (The AVREF voltage is the same as the V5V voltage).

- For software ADC sampling, FW_ADC_START_EN must be set to 1.
- Set the FW_ADC_START bit to 1 to launch one time of ADC sampling and conversion. Once the conversion is done, the FW_ADC_START bit will be cleared automatically.
- Configure the FW_ADC_SEL[3:0] to select different input channels for sampling. The ADC result is stored in the FW_ADC_RESULT[11:0] after each AD conversion.
- 16 ADC_CLK is needed for each ADC sampling conversion. (16T ADC_CLK = 32T SYS_CLK, system clock)
- When the SVM Mode function is activated, it is important to set the FW_ADC_START_EN bit to 0 to prevent interference with the real-time automatic trigger mode of the internal circuitry, especially during the motor drive timing sequences operation.

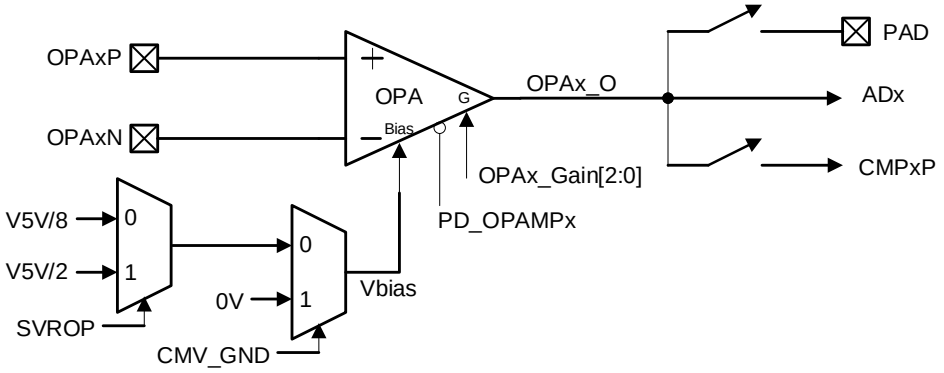


EMG1130 also provides an auto-sequence ADC converter, there are maximum six queues for convert ADC channel that user queued by CONVx registers. And the result will obtained from ADC_RESULTx register. Maximum convert number is configured from MAX_CONV register.



3.17. OPAMP(OPA)

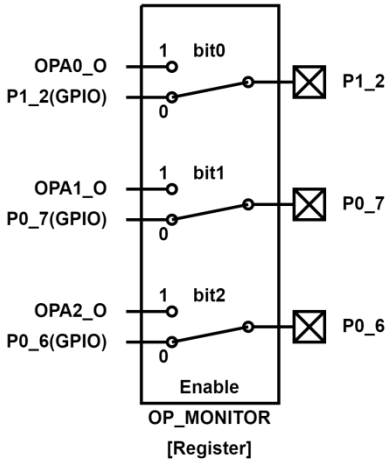
The EMG1130 has 3 independent operational amplifiers, OPA0, OPA1, and OPA2. Each OPA has its own power-down bit, PD_OPAMPx. PD_OPAMPx=1 indicates that the OPAx is powered down, oppositely setting it to 0 indicates that the OPAx is powered on. The same bias voltage (Vbias) for all OPAs can be selected as 0V, V5V/8, or V5V/2 by configuring the settings of CMV_GND and SRVOP.



The output (Vo) of the operational amplifier is connected to the ADx interface internally and given by Vo = Vin × Gain + Vbias.

OPAs has optional PAD output for monitor, and comparator plus terminal connection for OCP. OPAs Gain options include 1x, 2x, 4x, 8x, 16x, 20x, and 32x.

The EMG1130 also provides the option for amplifier output connections. If the amplifier output signal is needed, the user can configure it through the OP_MONITOR register. When the function of OPA output to pad is enabled, the GPIO function of the pad will be disabled internally.

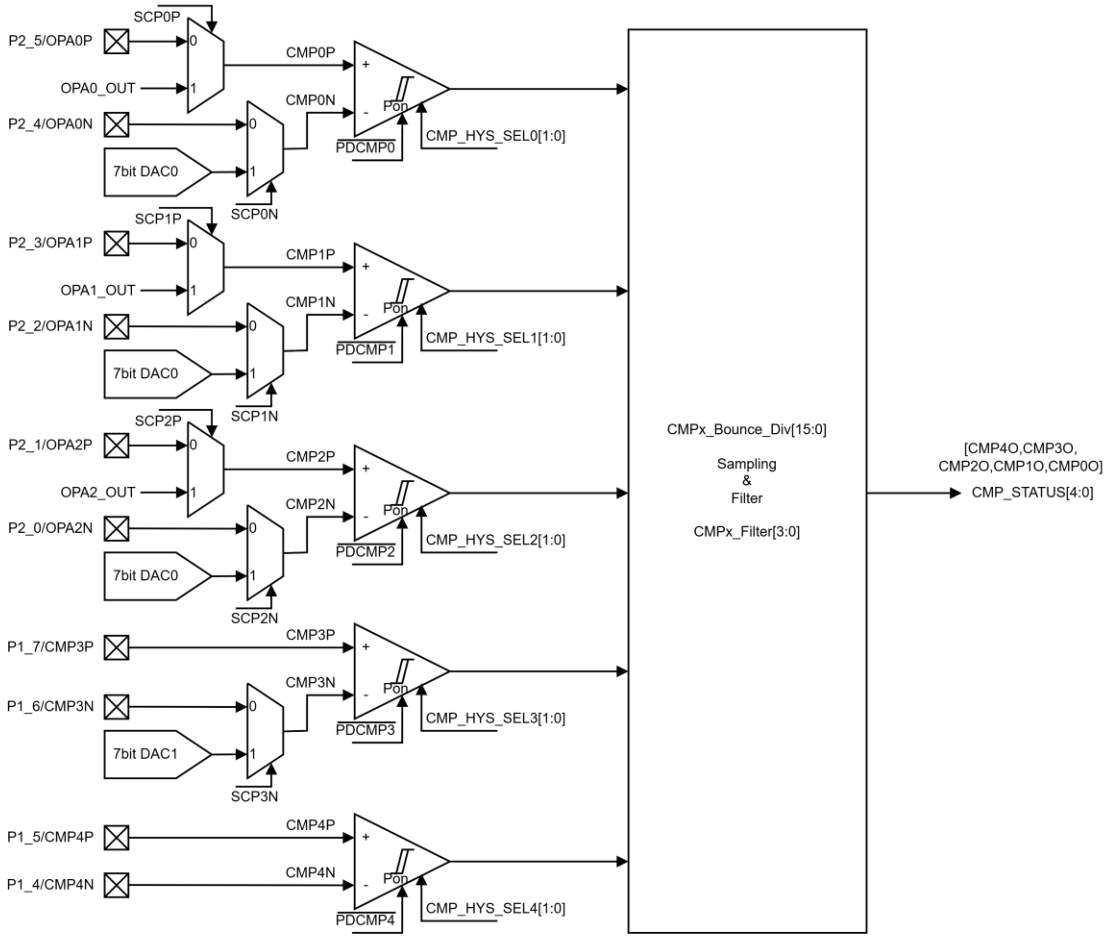


3.18. Comparator (CMP)

The EMG1130 provides 5 independent analog comparators. Three of them (CMP0/CMP1/CMP2) are primarily used for over-current sensing. CMP3 and CMP4 are reserved. Each comparator has its own power-down bit, PDCMPx. PDCMPx=1 indicates that the comparator is powered down, oppositely setting it to 0 indicates that the comparator is powered on.

Additionally, the sampling division (CMPx_Bounce_Div) and digital signal filtering (CMPx_Filter) functions are available. (Noted: When using the CMP module, it is important to set HW_EN=1 to enable the module.)

CMP0/CMP1and CMP2 have either the configurable internal OPA out or the external pin as plus CMP0/CMP1/CMP2 and CMP3 also have negative input with internal configurable voltage or the external pin



3.19. PWMIN(h_SPD)

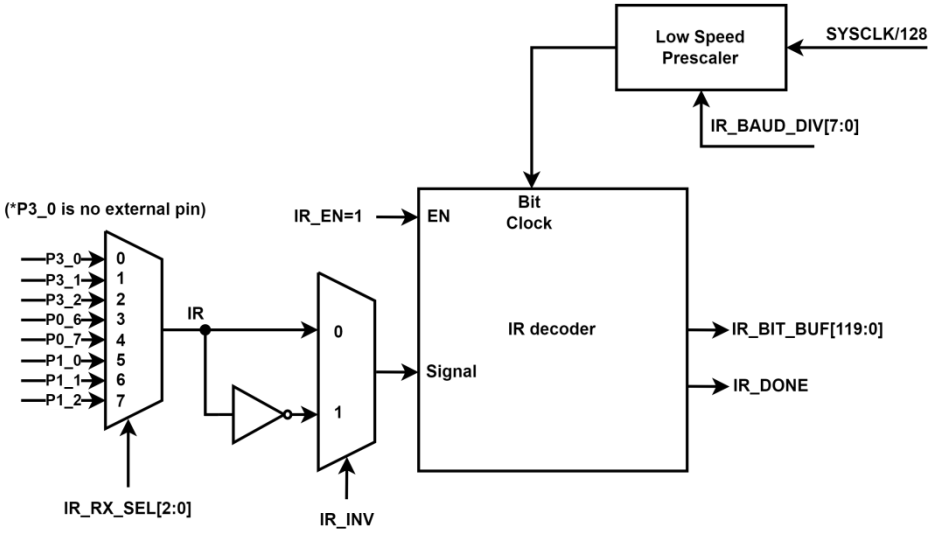
The duty cycle comparator input is connected to a specific pin, PWMIN. The frequency range of PWM input signal for detection is 1k to 100kHz. Duty cycle result(0 to 4095) is obtained from the combination of two 8-bit registers: h_SPD_H (high byte) and h_SPD_L (low byte).

3.20. Pulse Width Modulation (PWM)

The motor control pulse width modulated (PWM) output on its specific-pin. The frequency of the output is dependent on the time base for the PWM_CNT, and the setting of the PWM cycle length (16-bits). It is important to note that all channels configured for 16-bit PWM mode will use the same cycle length. It is not possible to configure one channel for different cycle length. However, the PWM timer composed of two 8-bit registers: PWM_CNT_H (high byte) and PWM_CNT_L (low byte). PWM timer may be clocked by the system clock. The cycle length composed of two 8-bit registers: REG_PWM_PRD_H (high byte) and REG_PWM_PRD_L (low byte).

3.21. IR decoder

EMG1130 provides an IR decoder module, decoding waveforms include NEC, RC-5, RC-6, and Sharp. As well as user can custom IR decoder to fit variety protocols.



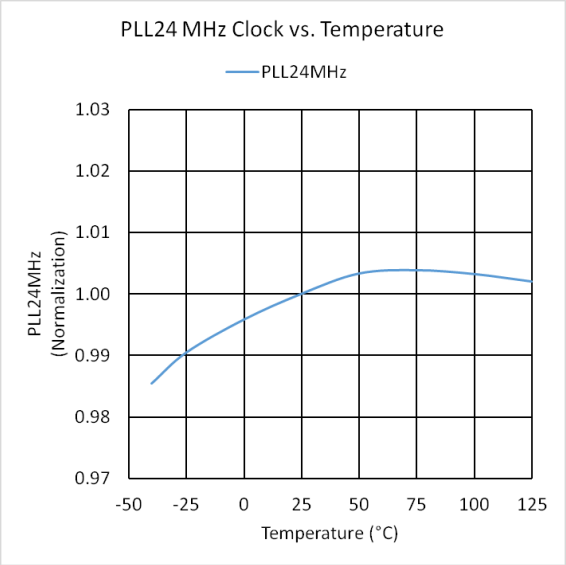
3.22. Motor Arithmetic Unit (MAU)

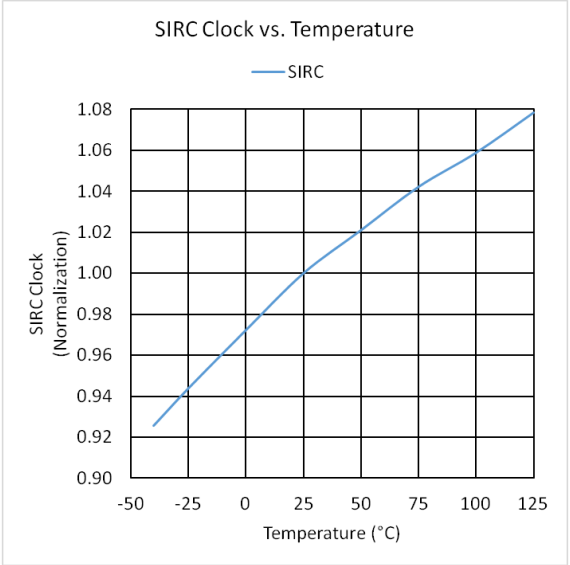
The EMG1130 fully inherits the features of EMT1050 that incorporates advanced Field-oriented control (FOC) technology to deliver precise and efficient BLDC motor control. The FOC method allows for optimal torque and speed performance by controlling the d-q axis currents, ensuring smooth operation across a wide range of motor conditions. Additionally, the MAU integrates a robust sensorless control algorithm, enabling motor operation without the need for physical position sensors, further reducing system complexity and cost.

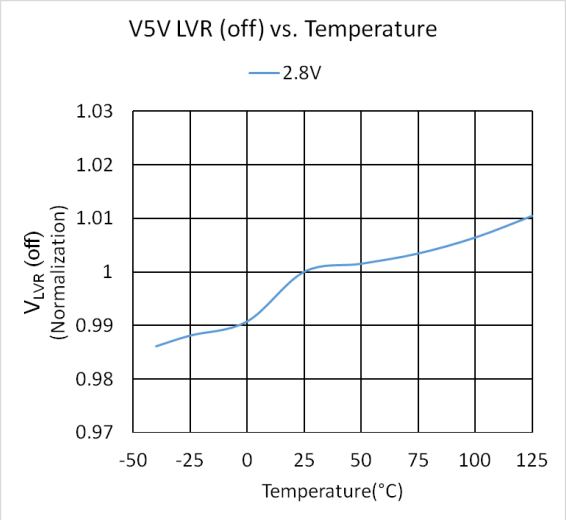
To address the complexities of modern BLDC motor applications, the MAU integrates a comprehensive set of digital circuit modules, including:

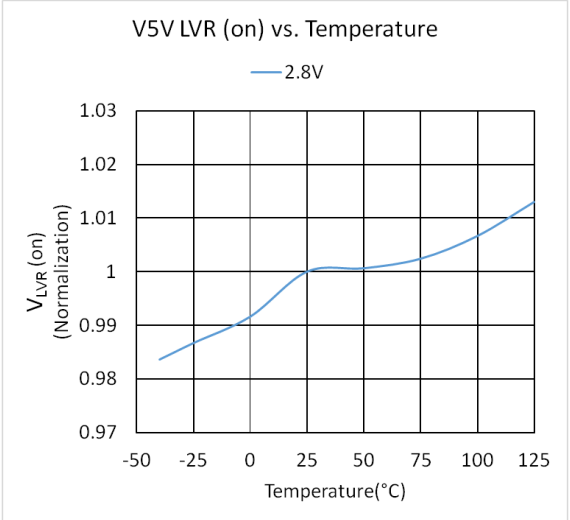
1. Speed loop PID module
2. d-q axis current control module
3. Initial position detection module
4. SVPWM module with 5/7 SVPWM switching capability
5. ADC Low Pass Filter (LPF) module
6. High PWM resolution algorithm module
7. Voltage feedforward compensation module
8. Speed Observer module
9. Sensorless control for sensorless operation

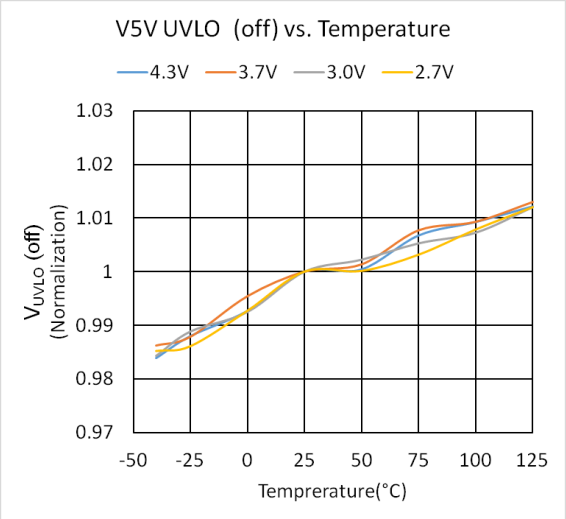
3.23. Typical Operating Characteristics

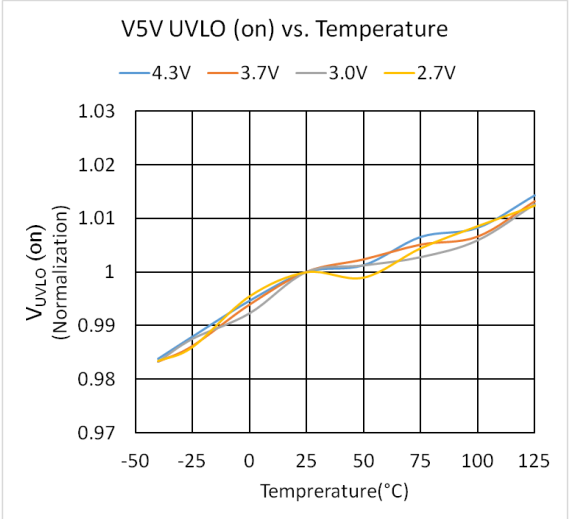








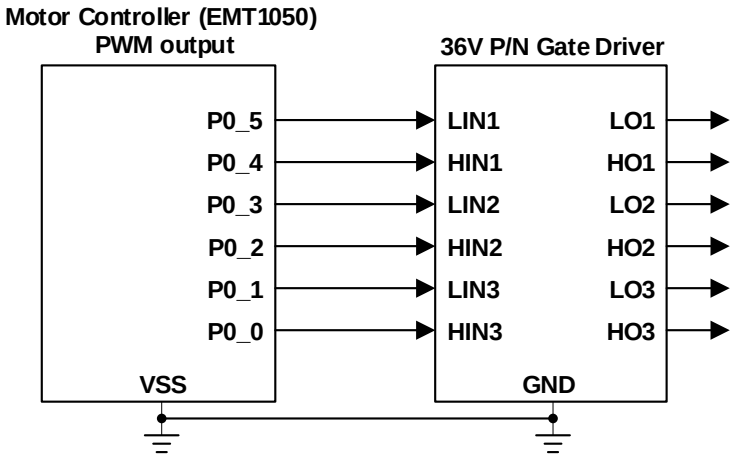




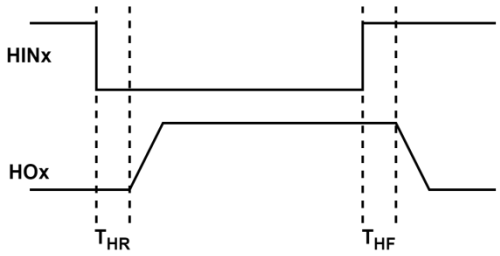
4. Gate Driver Description

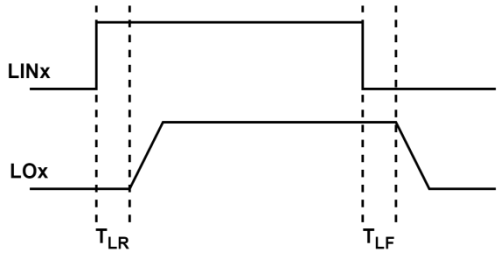
4.1. Internal Connection Signal

EMG1130 includes both FOC motor controller (EMT1050) and 36V P/N gate driver. Blow figure shows the internal connection between EMT1050 PWM output and 36V P/N gate driver input.



4.2. Logic and Timing

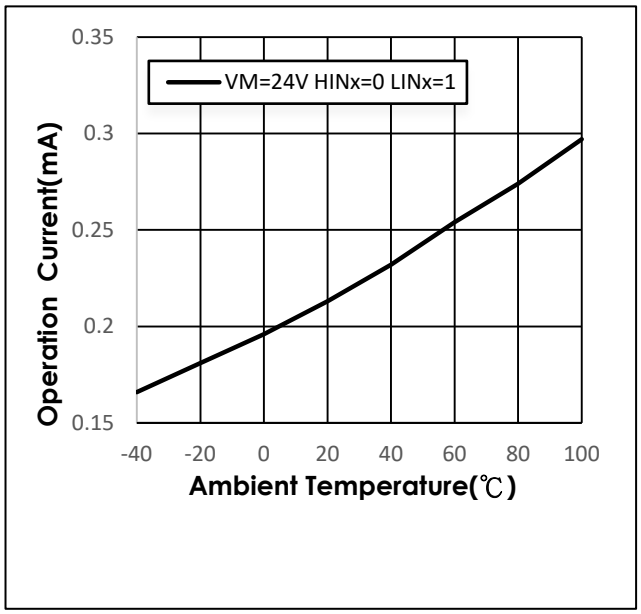




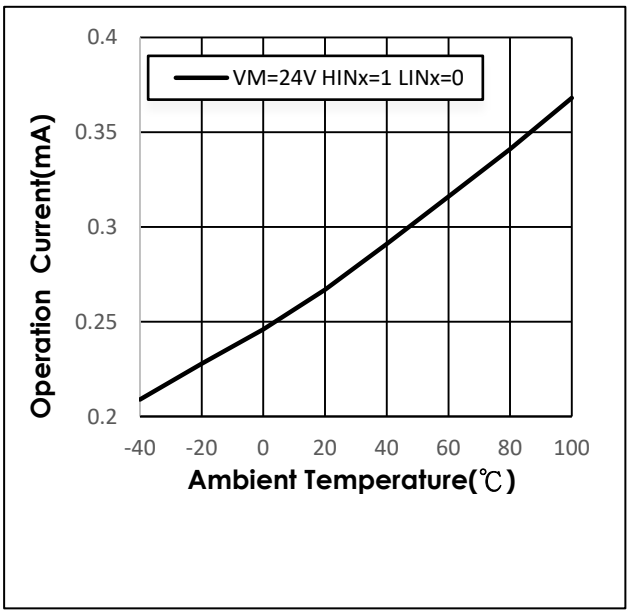
4.3. Typical Characteristics

Plots generated using characterization data.

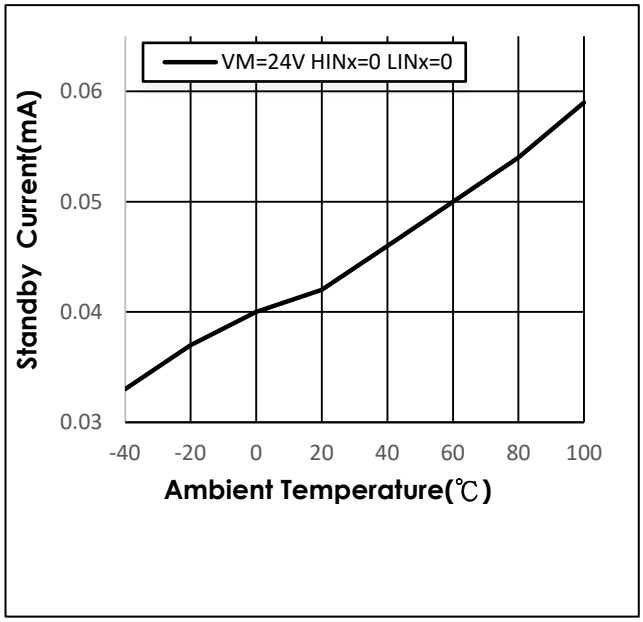
VM Operation Current VS Ambient Temperature



VM Operation Current VS Ambient Temperature



VM Standby Current VS Ambient Temperature



4.4. Shoot Through Prevention Function

The gate driver has shoot through prevention circuitry monitoring the high and low side control inputs. It can be designed to prevent outputs of high and low side from turning on at the same time, as shown below Figure 1 and Figure 2.

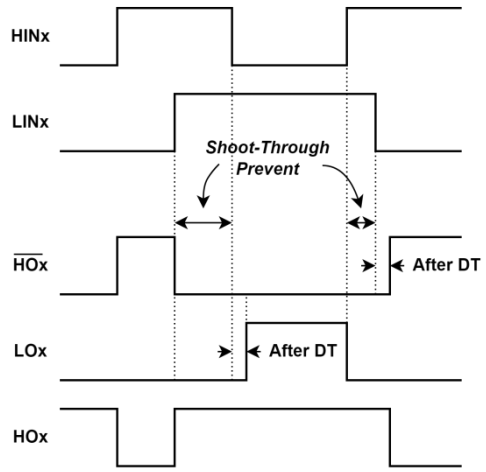


Figure 1

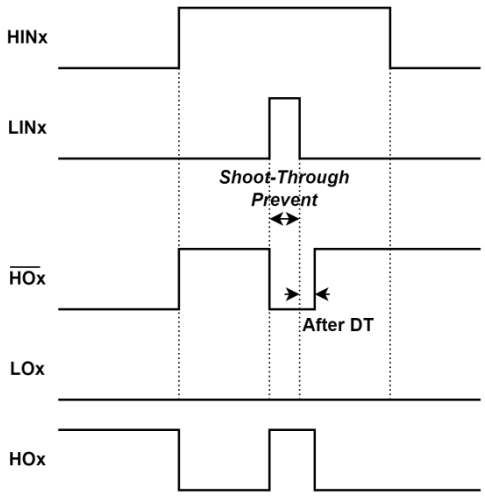
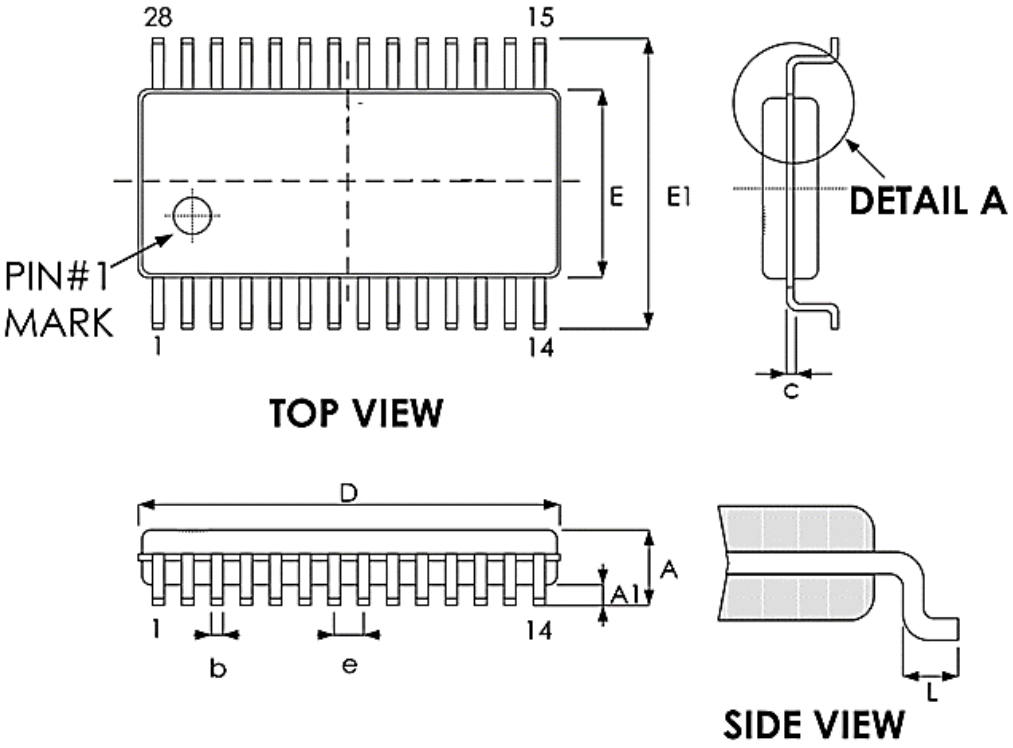


Figure 2

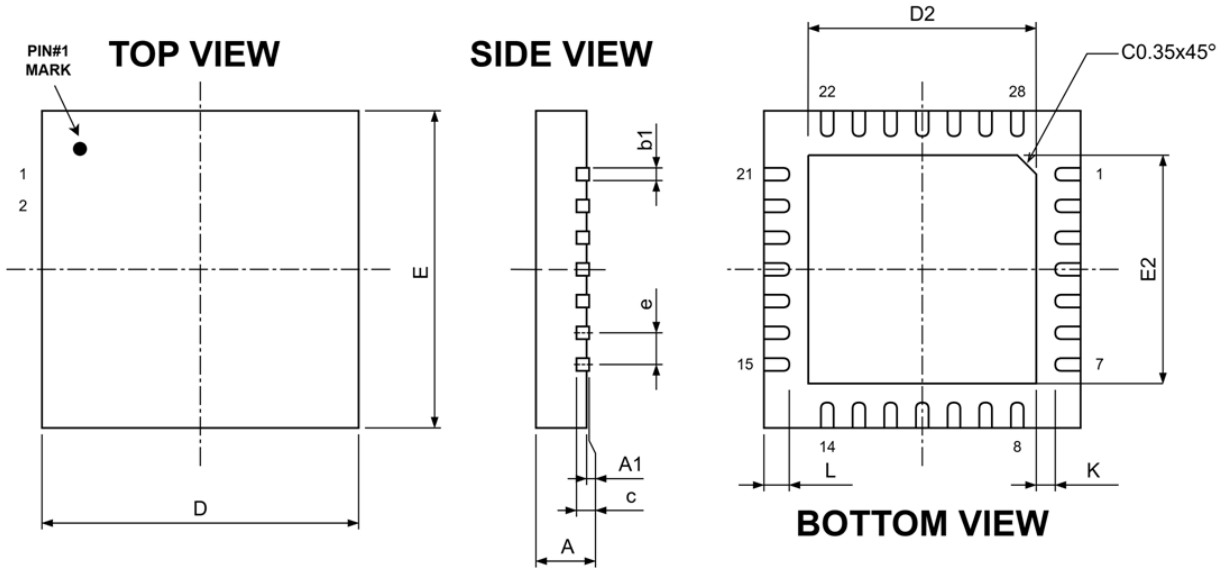
5. Package Outline Drawing

TSSOP-28L (173 mil)



Symbol	Dimension in mm	
	Min.	Max.
A	--	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.09	0.20
D	9.60	9.80
E	4.30	4.50
E1	6.30	6.50
e	0.65 BSC	
L	0.45	0.75

TQFN5x5-28L (Pitch : 0.5mm) (EMG1130-ND28)



Symbol	Dimension in mm	
	Min.	Max.
A	0.70	0.80
A1	0.00	0.05
b1	0.18	0.30
c	0.203 REF.	
D	5.00 BSC	
E	5.00 BSC	
e	0.50 BSC	
L	0.50	0.60
K	0.20	--

Exposed pad

Symbol	Dimension in mm	
	Min.	Max.
D2	3.20	3.30
E2	3.20	3.30

6. Revision History

Revision	Date	Description
1.0	2025.02.24	Original
1.1	2026.03.06	1. Added TQFN5x5-28L package type (Page 1) 2. Added Sensorless + 3-Shunt application (Page 2) 3. Added TQFNx5x-28L pinouts and Modified Pinouts and pin descriptions (Page 5-12) 4.Added TQFNx5x-28L order information (Page13) 5.Updated Comparator input max range as V_{V5V}-0.625 (Pages 19) 6.Updated Comparator reference max range as 0.875 x V_{V5V} (Pages 19) 7. Updated VIH/VIL definitions (Pages 19) 8. Modified uart figure (Page 24) 9. Modified 15 ADC_CLK to 16 (Page 29) 10. Modified 15T ADC_CLK = 30T SYS_CLK to 16T ADC_CLK = 32T SYS_CLK (Page 29) 11. Modified comparator figure (Page 32) 12. Added TQFN5x5-28L POD (Page 40)

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