64KB Flash, 4KB SRAM, 12bit 1MSPS ADC, M0+ MCU

- 2.5V to 5.5V operation voltage range
- 7CH 12-bit 1MSPS SAR ADC
  - 1MSPS data rate
  - Max. 16 Channels
  - 0 ~ VDD input dynamic range
  - Configurable 16/20 conversion cycles
  - Support end-of-conversion interrupt
- ARM Cortex M0+ MCU architecture
  - 64KB Flash/4KB SRAM
  - 10 x 16-bit timer/counter
  - 16 Interrupt sources
- 3 power modes management
  - Normal mode
  - Sleep mode
  - Deep-sleep mode
- Support multi-clock sources
  - 4~24MHz external high speed clock (HSE)
  - 4~24 MHz internal high speed clock (HSI)
  - 32.768KHz external low speed clock (LSE)
  - 32.768KHz internal high speed clock (LSI)
- 16 configurable GPIOs
- Real-time clock with programmable alarm control
- Up to 10 Times
- Buzzer controller
- Serial communication interfaces
  - 2 UARTs
  - 1 LPUART
  - 1 SPI
  - 1 I2C
  - 1 OWI
- Analog peripheral function
  - LVD
  - LVR
- -40 ~85℃ operation temperature
- Package Type
  - TSSOP-20L、LQFP48

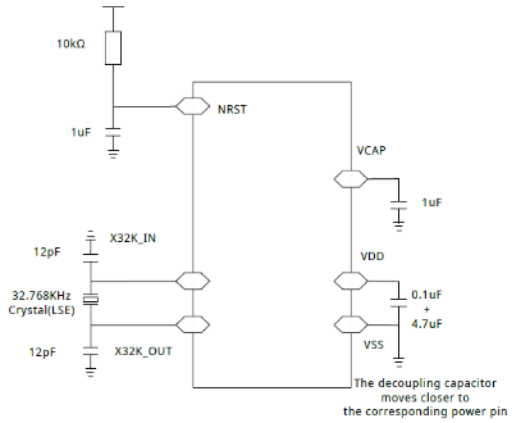
Applications

- Instrumentation signal measurements
- Temperature measurements
- Gas detectors and Smoke detectors
- Weigh scale facilities
- Pressure measurements
- Industrial system controller
- Smart Home sensor analog front-end controller
- Home appliance sensor signal processor

Description

ESMT FE82100 incorporates an ARM Cortex M0+ core processor, operating at 24MHz frequency, 64KB Flash and 4KB SRAM. The operation supply voltage is 2.5~5.5V and the temperature range from -40 to 85℃. FE82100 package in TSSOP-20L with 16 configurable GPIOs. Internal up to 7 channels high speed SAR ADC can operates at 1MSPS for industrial measurement application.

Brief Supply Connections



Product Features

Features	FE82100	
Pin counts	20	32
Master frequency	24MHz	
Supply voltage	2.5 ~ 5.5V	
Operation temperature	-40 ~ 85℃	
Flash protection	YES	
GPIOs	16	28
External interrupts	16	28
Advanced Timer (TIM1)	1	
General Timers (TIM2)	1	
Timer array (PCA)	1	
TIM10/11	2	
ADC channels	7	16
Flash size	64KB	
SRAM size	4KB	
IWDG	1	
WWDG	1	
OWI	1	
UART	2	
LPUART	1	
SPI	1 (12Mbps)	
I2C	1	
Buzzer	1	
QWK	1	
RTC	1	
LVD	1	
LVR	1	
CRC16	1	
Packages	TSSOP-20L	LQFP32

GPIO Multiplexing Table

Package		GPIO Multiplexing											
LQFP32	TSSOP	name	0	1	2	3	4	5	6	7	8	9	F
29	1		PD4	TIM1_CH1	PCA_CH0	RTC_1HZ	TIM10_TOG	UART1_TXD	TIM10_EXT	BEEP	TIM2_CH1		VCMPIN2
30	2		PD5	TIM1_CH1N	PCA_CH4	SPI_MISO	I2C_SCL	UART2_TXD	TIM10_GATE	UART1_TXD	TIM2_CH4		AIN5
31	3		PD6	TIM1_CH2	PCA_CH3	SPI_MOSI	I2C_SDA	UART2_RXD	LPTIM_EXT	UART1_RXD	TIM2_CH2		AIN6
1	4	NRST											
2	5		PA1	TIM1_CH2N		SPI_CLK	I2C_SDA	UART1_RXD	TIM10_TOG	UART2_RXD			OSC_IN
3	6		PA2	TIM1_CH3		SPI_NSS	I2C_SCL	UART1_TXD	TIM10_TOGN	UART2_TXD	TIM2_CH2		OSC_OUT
4	7	VSS											
5	8	VCAP											
6	9	VDD											
7	10		PA3	TIM1_CH3N	PCA_CH2	SPI_NSS	RTC_1HZ	LPUART_RXD	PCA_ECI	VCMP0_OUT	TIM2_CH3	UART2_TXD	
11	11		PB5	TIM1_BKIN	PCA_CH4	SPI_CLK	I2C_SDA	UART1_RXD	TIM11_TOG	LVD_OUT	TIM2_CH1		X32K_IN
12	12		PB4	LPTIM_GATE	PCA_ECI	SPI_NSS	I2C_SCL	UART1_TXD	TIM11_TOGN				X32K_OUT
20	13		PC3	TIM1_CH3	TIM1_CH1N		I2C_SDA	UART2_TXD	PCA_CH1	1-WIRE	TIM2_CH3		AIN1
21	14		PC4	TIM1_CH4	TIM1_CH2N		I2C_SCL	UART2_RXD	PCA_CH0	CLK_MCO	TIM2_CH4		AIN2
22	15		PC5	TIM1_BKIN	PCA_CH0	SPI_CLK		LPUART_TXD	TIM11_GATE	LVD_OUT	TIM2_CH1		VCMPIN1
23	16		PC6	TIM1_CH1	PCA_CH3	SPI_MOSI		LPUART_RXD	TIM11_EXT	CLK_MCO	TIM2_CH4		AIN0
24	17	SWDIO	PC7	TIM1_CH2	PCA_CH4	SPI_MISO		UART2_RXD	LSI_OUT	LSE_OUT			
26	18	SWDCLK	PD1		PCA_ECI			UART2_TXD	HSE_OUT	VCMP0_OUT			
27	19		PD2	TIM1_CH2	PCA_CH2	SPI_MISO	RTC_1HZ	LPUART_TXD	LPTIM_TOG	1-WIRE	TIM2_CH3		AIN3/ VCMPIN0
28	20		PD3	TIM1_CH3N	PCA_CH1	SPI_MOSI	LSE_OUT	UART1_RXD	LPTIM_TOGN		TIM2_CH2		AIN4
8			PA4	TIM1_CH2N		SPI_CLK	I2C_SDA	UART1_RXD	TIM10_TOG	UART2_RXD			AIN14
9			PB7	TIM1_CH3N	PCA_CH2	SPI_NSS	RTC_1HZ	LPUART_RXD	PCA_ECI	VCMP0_OUT	TIM2_CH3		AIN8
10			PB6	TIM1_CH1N	PCA_CH4	SPI_MISO	I2C_SCL	UART2_TXD	TIM10_GATE	UART1_TXD	TIM2_CH4		AIN9
13			PB3	TIM1_CH2	PCA_CH3	SPI_MOSI	I2C_SDA	UART2_RXD	LPTIM_EXT	UART1_RXD	TIM2_CH2		AIN10
14			PB2	TIM1_CH3N	PCA_CH1	SPI_MOSI	LSE_OUT	UART1_RXD	LPTIM_TOGN		TIM2_CH2		AIN11
15			PB1	TIM1_CH1	PCA_CH0	RTC_1HZ	TIM10_TOG	UART1_TXD	TIM10_EXT	BEEP	TIM2_CH1	TIM1_CH2N	AIN12
16			PB0	TIM1_CH3	TIM1_CH1N		I2C_SDA	UART2_TXD	PCA_CH1	1-WIRE	TIM2_CH3		AIN13
17			PC0	TIM1_CH3		SPI_NSS	I2C_SCL	UART1_TXD	TIM10_TOGN	UART2_TXD	TIM2_CH2	TIM1_CH1N	AIN15
18			PC1	TIM1_CH1	PCA_CH3	SPI_MOSI		LPUART_RXD	TIM11_EXT	CLK_MCO	TIM2_CH4	TIM1_CH2N	
19			PC2	TIM1_CH2	PCA_CH2	SPI_MISO	RTC_1HZ	LPUART_TXD	LPTIM_TOG	1-WIRE	TIM2_CH3	TIM1_CH3N	
25			PD0	TIM1_BKIN	PCA_CH0	SPI_CLK		LPUART_TXD	TIM11_GATE	LVD_OUT	TIM2_CH1		
32			PD7	TIM1_CH4	TIM1_CH2N	I2C_SCL		UART2_RXD	PCA_CH0	CLK_MCO	TIM2_CH4		

Pin Function Description

Pin		Name	Type	Function
LQFP32	TSSOP20			
29	1	PD4	PD4	PD4 GPIO
			TIM1_CH1	TIM1 PWM1 output
			PCA_CH0	PCA input capture/Output compare 0
			RTC_1HZ	RTC 1Hz output
			TIM10_TOG	TIM10 toggle output
			UART1_TX	UART1 TX
			TIM10_EXT	TIM10 external pulse
			BEEP	Buzzer output
			TIM2_CH1	TIM2 input capture/output compare 1
			VCMPIN2	Comparator input CH2
30	2	PD5	PD5	PD5 GPIO
			TIM1_CH1N	TIM1 PWM1 inverting output
			PCA_CH4	PCA input capture/output compare 4
			SPI_MISO	SPI host input slave output signal
			I2C_SCL	I2C clock
			UART2_TX	UART2 TX
			TIM10_GATE	TIM10 gating
			UART1_TX	UART1 TX
			TIM2_CH4	TIM2 input capture/output compare 4
			AIN5	SAR ADC analog input, CH5
31	3	PD6	PD6	PD6 GPIO
			TIM1_CH2	TIM1 PWM2
			PCA_CH3	PAC input capture/output compare 3
			SPI_MOSI	SPI host output slave input signal
			I2C_SDA	I2C data
			UART2_RX	UART2 RX
			LPTIM_EXT	LPTIM external pulse input
			UART1_RX	UART1 RX
			TIM2_CH2	TIM2 input capture/output compare 2
			AIN6	SAR ADC analog input, CH6

1	4	NRST	NRST	Reset input port, low active
2	5	PA1	PA1	PA1 GPIO
			OSC_IN	External clock source input
			TIM1_CH2N	TIM1 PWM2 inverting output
			SPI_CLK	SPI clock signal
			I2C_SDA	I2C data
			UART1_RX	UART1 RX
			TIM10_TOG	TIM10 toggle output
			UART2_RX	UART2 RX
3	6	PA2	PA2	PA2 GPIO
			OSC_OUT	External clock source output
			TIM1_CH3	TIM1 PWM3
			SPI_NSS	SPI slave chip select
			I2C_SCL	I2C clock
			UART1_TX	UART1 TX
			TIM10_TOGN	TIM10 toggle inverting output
			UART2_TX	UART2 TX
			TIM2_CH2	TIM2 input capture/output compare 2
4	7	VSS	GND	Ground
5	8	VCAP	Power	LDO power supply filtering capacitor
6	9	VDD	Power	Power
7	10	PA3	PA3	PA3 GPIO
			TIM1_CH3N	TIM1 PWM3 inverting output
			PCA_CH2	PCA input capture/output compare 2
			SPI_NSS	SPI slave chip select
			RTC_1HZ	RTC 1Hz output
			LPUART_RX	LPUART RX
			PCA_ECI	PCA external clock
			VCMP0_OUT	Voltage comparator 0 output terminal
			TIM2_CH3	TIM2 input capture/output compare 3
8		PA4	AIN14	ADC Analog input channel 14
			PA4	PA4 GPIO
			TIM1_CH2N	TIM1 PWM output 2 Inverting
			SPI_CLK	SPI Module clock signal

			I2C_SDA	I2C data
			UART1_RX	UART1 RX
			TIM10_TOG	TIM10 Toggle output
			UART2_RX	UART2 RX
9		PB7	PB7	PB7 GPIO
			TIM1_CH3N	TIM1 PWM output 3 Inverting
			PCA_CH2	PCA Input capture/Output compare 2
			SPI_NSS	SPI module slave chip selects signals
			RTC_1HZ	RTC 1HZ output
			LPUART_RX	LPUART RX
			PCA_ECI	PCA External clock
			VC0_OUT	Voltage comparator 0 output
			TIM2_CH3	TIM2 Input capture/Output compare 3
			AIN8	ADC Analog input channel 8
10		PB6	PB6	PB6 GPIO
			TIM1_CH1N	TIM1 PWM output 1 Inverting
			PCA_CH4	PCA Input capture/Output compare 4
			SPI_MISO	SPI module host input slave output signal
			I2C_SCL	I2C clock
			UART2_TX	UART2_TX
			TIM10_GATE	TIM10 gating
			UART1_TX	UART1 TX
			TIM2_CH4	TIM2 Input capture/Output compare 4
			AIN9	ADC Analog input channel 9
11	11	PB5	PB5	PB5 GPIO
			X32K_IN	External 32K clock source input
			TIM1_BKIN	TIM1 brake signal input
			PCA_CH4	PCA input capture/output compare 4
			SPI_CLK	SPI clock signal
			I2C_SDA	I2C data
			UART1_RX	UART1 RX
			TIM11_TOG	TIM11 toggle output
			LVD_OUT	LVD comparator output
			TIM2_CH1	TIM2 input capture/output compare 1

12	12	PB4	PB4	PB4 GPIO
			X32K_OUT	External 32K clock source output
			LPTIM_GATE	LPTIM gating
			PCA_ECI	PCA external clock
			SPI_NSS	SPI slave chip select
			I2C_SCL	I2C clock
			UART1_TX	UART1 TX
			TIM11_TOGN	TIM11 toggle inverting output
13		PB3	PB3	PB3 GPIO
			TIM1_CH2	TIM1 PWM output 2
			PCA_CH3	PCA Input capture/Output compare 3
			I2C_SDA	I2C data
			SPI_MOSI	SPI module host output slave input signal
			UART2_RXD	UART2 RXD
			LPTIM_EXT	LPTIM External pulse input
			UART1_RXD	UART1 RXD
			TIM2_CH2	TIM2 Input capture/Output compare 2
			AIN10	ADC Analog input channel 10
14		PB2	PB2	PB2 GPIO
			TIM1_CH3N	TIM1 PWM output 3 Inverting
			PCA_CH1	PCA Input capture/Output compare 1
			SPI_MOSI	SPI module host output slave input signal
			LSE_OUT	External high frequency crystal output
			UART1_RX	UART1 RX
			LPTIM_TOGN	LPTIM Toggle inverting output
			TIM2_CH2	TIM2 Input capture/Output compare 2
			AIN11	ADC Analog input channel 11
15		PB1	PB1	PB1 GPIO
			TIM1_CH1	TIM1 PWM output 1
			PCA_CH0	PCA Input capture/Output compare 0
			RTC_1HZ	RTC 1HZ output
			TIM10_TOG	TIM10 Toggle output
			UART1_TXD	UART1 TXD
			TIM10_EXT	TIM10 External pulse

			BEEP	Buzzer output
			TIM2_CH1	TIM2 Input capture/Output compare 1
			AIN12	ADC Analog input channel 12
			TIM1_CH2N	TIM1 PWM output 2 Inverting
16		PB0	PB0	PB0 GPIO
			TIM1_CH3	TIM1 PWM output 3
			TIM1_CH1N	TIM1 PWM output 1 Inverting
			I2C_SDA	I2C data
			UART2_TX	UART2 TX
			PCA_CH1	PCA Input capture/Output compare 1
			1-WIRE	1-wire Input/output
			TIM2_CH3	TIM2 Input capture/Output compare 3
			AIN13	ADC Analog input channel 13
17		PC0	PC0	PC0 GPIO
			TIM1_CH3	TIM1 PWM output 3
			SPI_NSS	SPI module slave chip selects signals
			I2C_SCL	I2C clock
			UART1_TXD	UART1 TXD
			TIM10_TOGN	TIM10 Toggle inverting output
			UART2_TXD	UART2 TXD
			TIM2_CH2	TIM2 Input capture/Output compare 2
			TIM1_CH1N	TIM1 PWM output 1 Inverting
			AIN15	ADC Analog input channel 15
18		PC1	PC1	PC1 GPIO
			TIM1_CH1	TIM1 PWM output 1
			PCA_CH3	PCA Input capture/Output compare 3
			SPI_MOSI	SPI module host output slave input signal
			LPUART_RX	LPUART RX
			TIM11_EXT	TIM11 External pulse input
			CLK_MCO	CPU Clock output
			TIM2_CH4	TIM2 Input capture/Output compare 4
			TIM1_CH2N	TIM1 PWM output 2 Inverting
19		PC2	PC2	PC2 GPIO
			TIM1_CH2	TIM1 PWM output 2

			PCA_CH2	PCA Input capture/Output compare 2
			SPI_MISO	SPI module host input slave output signal
			RTC_1HZ	RTC 1HZ output
			LPUART_TX	LPUART TX
			LPTIM_TOG	LPTIM Toggle output
			1-WIRE	1-wire Input/output
			TIM2_CH3	TIM2 Input capture/Output compare 3
			TIM2_CH3N	TIM1 PWM output 3 Inverting
20	13	PC3	PC3	PC3 GPIO
			TIM1_CH3	TIM1 PWM3 output
			TIM1_CH1N	TIM1 PWM1 inverting output
			I2C_SDA	I2C data
			UART2_TX	UART2 TX
			PCA_CH1	PCA input capture/output compare 1
			SWD	1-wire input/output
			TIM2_CH3	TIM2 input capture/output compare 3
			AIN1	SAR ADC analog input CH1
21	14	PC4	PC4	PC4 GPIO
			TIM1_CH4	TIM1 PWM4 output
			TIM1_CH2N	TIM1 PWM2 inverting output
			I2C_SCL	I2C clock
			UART2_RX	UART2 RX
			PCA_CH0	PCA input capture/output compare 0
			CLK_MCO	MCU clock output
			TIM2_CH4	TIM2 input capture/output compare 4
			AIN2	SAR ADC analog input CH2
22	15	PC5	PC5	PC5 GPIO
			TIM1_BKIN	TIM1 brake signal input
			PCA_CH0	PCA input capture/output compare 0
			SPI_CLK	SPI clock signal
			LPUART_TX	LPUART TX
			TIM11_GATE	TIM11 gating
			LVD_OUT	Low voltage detection output
			TIM2_CH1	TIM2 input capture/output compare 1

			VCMPIN1	Analog voltage comparator input CH1
23	16	PC6	PC6	PC6 GPIO
			TIM1_CH1	TIM1 PWM1
			PCA_CH3	PCA input capture/output compare 3
			SPI_MOSI	SPI host output slave input
			LPUART_RX	LPUART RX
			TIM11_EXT	TIM11 external pulse input
			CLK_MCO	MCU clock output
			TIM2_CH4	TIM2 input capture/output compare 4
			AIN0	SAR ADC analog input CH1
24	17	PC7	PC7	PC7 GPIO
			SWDIO	1-wire I/O
			TIM1_CH2	TIM1 PWM2
			PCA_CH4	PCA input capture/output compare 4
			SPI_MISO	SPI host input slave output
			UART2_RX	UART2 RX
			LSI_OUT	Internal low frequency RC clock 38.4KHz output
			X32K_OUT	External low frequency XTAL output
25		PD0	PD0	PD0 GPIO
			TIM1_BKIN	TIM1 Brake signal input
			PCA_CH0	PCA Input capture/Output compare 0
			SPI_CLK	SPI Module clock signal
			LPUART_TXD	LPUART TXD
			TIM11_GATE	TIM11 gating
			LVD_OUT	Low voltage detection comparator output
			TIM2_CH1	TIM2 Input capture/Output compare 1
26	18	PD1	PD1	PD1 GPIO
			SWDCLK	SWD Clock
			PCA_ECI	PCA external clock
			UART2_TX	UART2 TX
			HSE_OUT	Internal high frequency 24MHz clock output
			VCMP0_OUT	Analog comparator output

27	19	PD2	PD2	PD2 GPIO
			TIM1_CH2	TIM1 PWM2
			PCA_CH2	PCA input capture/output compare 2
			SPI_MISO	SPI host input slave output
			RTC_1HZ	RTC 1Hz output
			LPUART_TX	LPUART TX
			LPTIM_GOG	LPTIM toggle output
			SWD	1-wire input/output
			TIM2_CH3	TIM2 input capture/output compare 3
			VCMPIN0	Analog voltage comparator input CH0
			AIN3	SAR ADC analog input CH3
28	20	PD3	PD3	PD3 GPIO
			TIM1_CH3N	TIM1 PWM3 inverting output
			PCA_CH1	PCA input capture/output compare 1
			SPI_MOSI	SPI host output slave input
			LSE_OUT	External high frequency XTAL output
			UART1_RX	UART1 RX
			LPTIM_TOGN	LPTIM toggle inverting output
			TIM2_CH2	TIM2 input capture/output compare 2
			AIN4	SAR ADC analog input CH4
32		PD7	PD7	PD7 GPIO
			TIM1_CH4	TIM1 PWM output 4
			TIM1_CH2N	TIM1 PWM output 2 Inverting
			I2C_SCL	I2C clock
			UART2_RX	UART2 RX
			PCA_CH0	PCA Input capture/Output compare 0
			CLK_MCO	CPU Clock output
			TIM2_CH4	TIM2 Input capture/Output compare 4

Pin Configuration

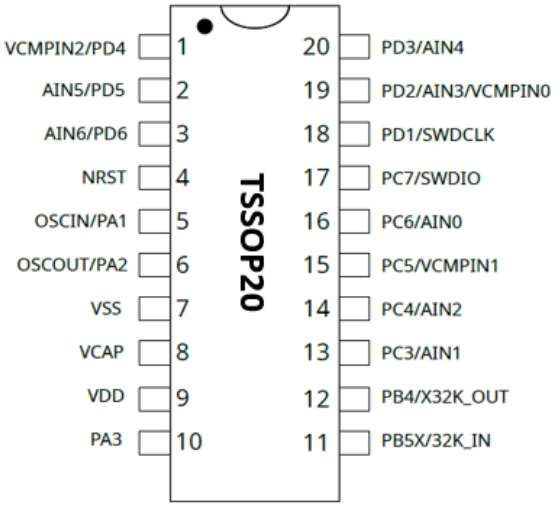


Figure 1. TSSOP20

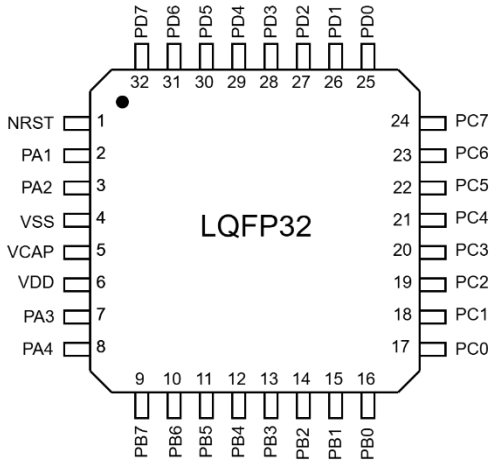
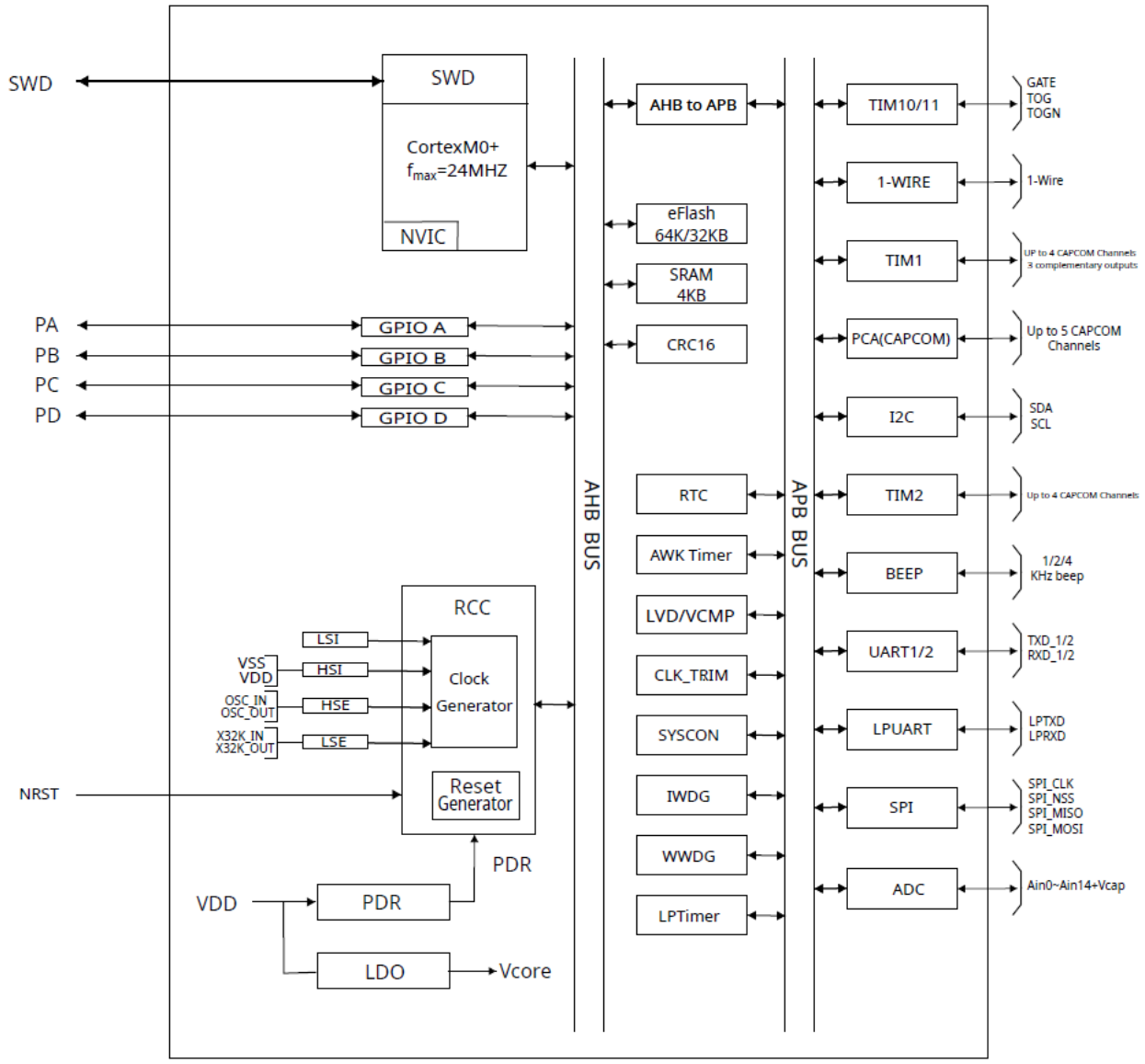


Figure 2. LQFP32

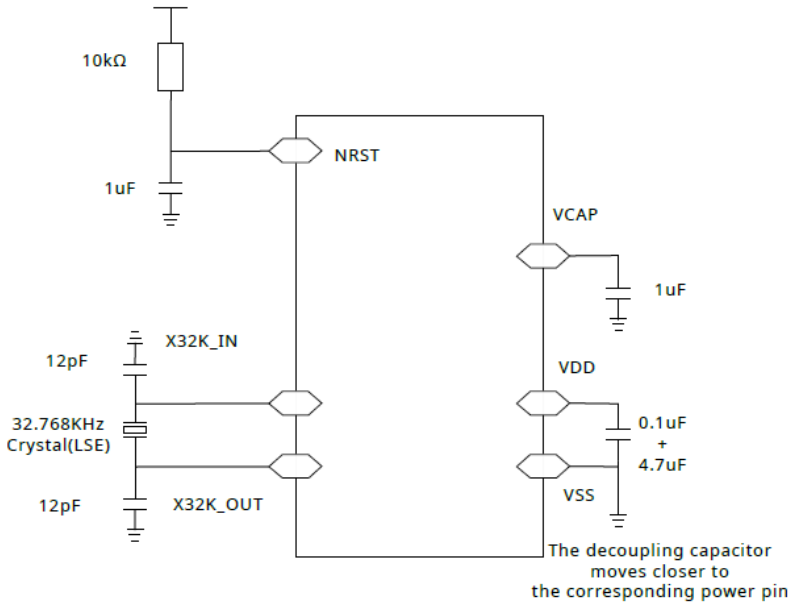
Ordering Information

Product ID	Package Type	Packing	Comments
FE82100	TSSOP20	3000 Units/Reel	Green

Functional Block Diagram



Application Circuit



Absolute Maximum Rating

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
VDD	Supply voltage	VDD to VSS	-0.3	6.0	V
V_{IO}	Digital I/O ports	All I/O ports	-0.3	VDD+0.3	V
CLK_{MCU}	MCU core clock		32.768K	24	MHz
T_A	Operating ambient temperature range		-40	85	°C
T_J	Maximum junction temperature		–	150	°C
T_{stg}	Storage temperature range		-40	150	°C
ESD	Human Body Model		±4K		V
	Charged Device Model		±1K		

Recommended Operating Conditions

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
VDD	Supply voltage	VDD to VSS	2.5	5.5	V
V_{IO}	I/O ports	All I/O ports	2.5	5.5	V
VCAP	VCAP capacitor	C_S connection	0.47	2.2	uF
RC_{OSC}	Internal RC clock oscillator		—	24	MHz
T_{OP}	Operating temperature range		-40	85	°C

Electrical Characteristics

- VDD=3.3V, at T_A=-40 ~ 85°C, unless otherwise noted

SYMBOL	PARAMETER	CONDITION			MIN	TYP	MAX	UNIT
VDD	Supply voltage	Normal operation			2.2	—	3.6	V
POR	Power On Reset				2.2	2.25	2.3	V
$I_{Q,ACTIVE}$	Active mode current consumption	VDD=3.3V	HSI clock (peripheral clock on)	4MHz	—	468	542	uA
				8MHz	—	839	966	
				16MHz	—	1575	1811	
				24MHz	—	2298	2549	
			HSI clock (peripheral clock off)	4MHz	—	397	698	uA
				8MHz	—	696	1246	
				16MHz	—	1291	1442	
				24MHz	—	1871	2377	
			LSE clock 32.768KHz (peripheral clock on)	-40~25℃	—	34	46	uA
				85℃	—	41	54	
			LSE clock 32.768KHz (peripheral clock off)	-40~25℃	—	34	51	uA
				85℃	—	44	56	
			HSE clock(peripheral clock on)	-40~25℃	—	2.56	2.96	mA
			HSE clock(peripheral clock off)	-40~25℃	—	2.15	2.73	mA
$I_{Q,SLEEP}$	Sleep mode current consumption	VDD=3.3V	HSI clock (peripheral clock on)	4MHz	—	181	211	uA
				8MHz	—	282	324	
				16MHz	—	486	537	
				24MHz	—	689	813	
			HSI clock (peripheral clock off)	4MHz	—	122	147	uA
				8MHz	—	166	194	
				16MHz	—	252	296	
				24MHz	—	338	415	
			LSE clock 32.768KHz (peripheral clock on)	-40~25℃	—	26	41	uA
				85℃	—	32	44	
			LSE clock 32.768KHz (peripheral clock off)	-40~25℃	—	25	40	uA
				85℃	—	32	48	
			HSE clock(peripheral clock on)	-40~25℃	—	884	1030	uA
			HSE clock(peripheral clock off)	-40~25℃	—	534	643	uA
$I_{Q,DeepSLEEP}$	Deep sleep mode current consumption	VDD=3.3V	LSE 32.768KHz Peripheral clock off AWK,IWDG,LTIM,RTC on	-40~25℃	—	1.20	1.28	uA
				85℃	—	3.04	3.44	
			LSE 32.768KHz Peripheral clock off, IWDG on	-40~25℃	—	1.20	1.33	uA
				85℃	—	4.53	4.93	
			LSE 32.768KHz	-40~25℃	—	1.18	1.31	uA

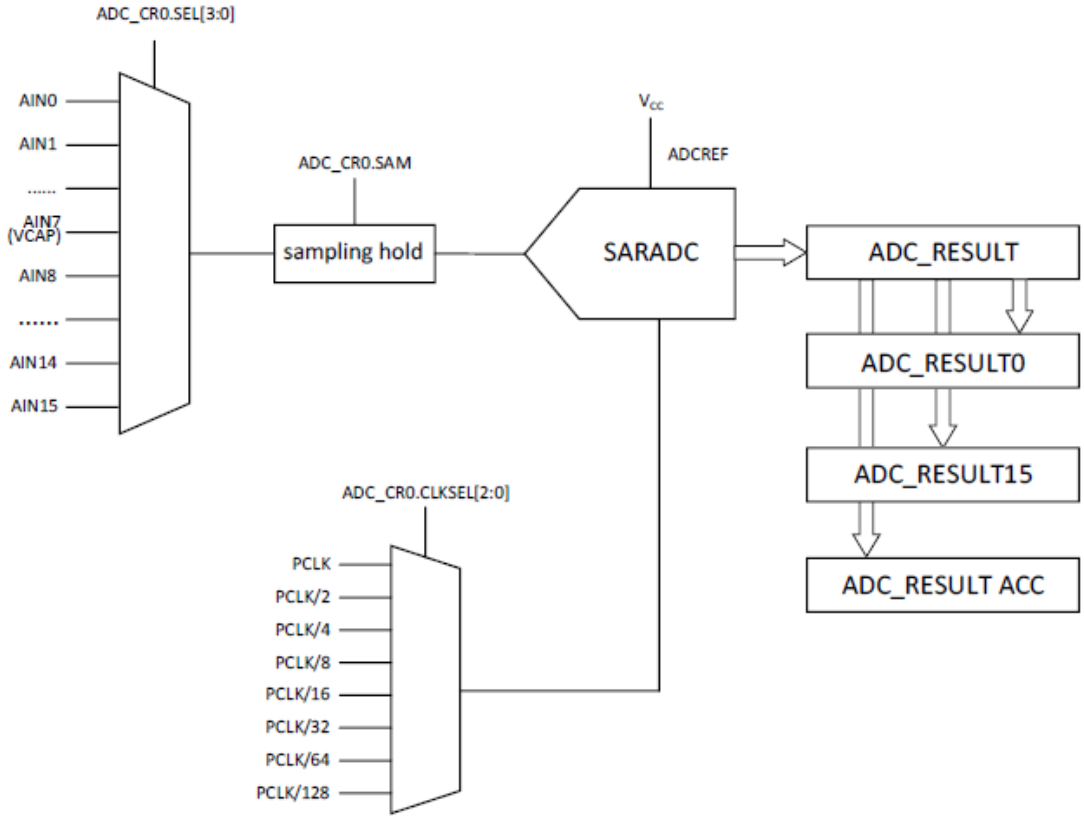
			Peripheral clock off, LPTIM on	85℃	—	4.46	4.85	
			LSE 32.768KHz Peripheral clock off, RTC on	-40~25℃	—	1.19	1.59	uA
				85℃	—	6.74	7.98	
			HIS 4MHz	-40~25℃	—	0.89	1.19	uA
				85℃	—	5.04	5.93	
General Purpose I/O ports								
V_{OH}	Logic output Hi threshold	VDD = 3.3V, source 4mA		VDD-0.2	—	—	V	
		VDD = 3.3V, source 6mA		VDD-0.3	—	—	V	
V_{OL}	Logic output Lo threshold	VDD = 3.3V, sink 4mA		—	—	VSS+0.2	V	
		VDD = 3.3V, sink 6mA		—	—	VSS+0.3	V	
V_{OHD}	Logic output Hi at Dual source current	VDD = 3.3V, source 8mA		VDD-0.2	—	—	V	
		VDD = 3.3V, source 12mA		VDD-0.3	—	—	V	
V_{OLD}	Logic output Lo at Dual source current	VDD = 3.3V, sink 8mA		—	—	VSS+0.2	V	
		VDD = 3.3V, sink 12mA		—	—	VSS+0.3	V	
Port PA, PB, PC, PD								
V_{IT+}	Positive input threshold voltage	VDD=2.5V		1.4	—	—	V	
		VDD=3.3V		1.8	—	—		
		VDD=5.5V		3.0	—	—		
V_{IT-}	Negative input threshold voltage	VDD=2.5V		—	—	0.9	V	
		VDD=3.3V		—	—	1.3		
		VDD=5.5V		—	—	2.4		
V_{HYS}	V_{IT+} - V_{IT-}	VDD=2.5V		—	0.5	—	V	
		VDD=3.3V		—	0.5	—		
		VDD=5.5V		—	0.6	—		
R_{PU}	Pull up resistor			40	50	60	KΩ	
C_{IN}	Input capacitance			—	5	—	pF	
I_{LEAK}	Input leakage current	VDD=2.5~3.6V		—	—	±50	nA	
Timer								
T_{INT}	External interrupt	External interrupt triggering		30	—	—	ns	
T_{CAP}	Timer capture time	TIM1/TIM2 capture pulse width at 4MHz		0.5	—	—	us	
TMR_{EXT}	Timer clock	TIM1/2/10/11 external clock at 4MHz		0	—	$f_{TIMCLK}/2$	MHz	
T_{PCA}	PCA clock	PCA external clock at 4MHz		0	—	$f_{PCACLK}/2$	MHz	
Internal High Speed Clock								
HIS	HSI	Internal high speed RC oscillator clock		4	16	24	MHz	
$T_{START,HSI}$	HSI Start up time	HSI=4MHz		2	2.4	4.7	us	
		HSI=8MHz		1.15	1.47	3.01		
		HSI=16MHz		1.04	1.31	2.74		
		HSI=24MHz		1.1	1.30	2.71		
IDD	Current consumption	HSI=4MHz		31	56	113	uA	

		HSI=8MHz	40	72	151	
		HSI=16MHz	71	143	298	
		HSI=24MHz	93	196	383	
HSI_{DUTY}	Duty cycle		45	50	55	%
HSI_{ACC}	HCI Frequency accuracy	VDD=2.5~5.5V, T_A =-40~85℃	-2.5	±1	+2.5	
		VDD=2.5~5.5V, T_A =-40~85℃	-2.0	±1	+2.0	
Internal Low Speed Clock						
LSI	LSI	Internal low speed RC oscillator clock	37.8 32.2	38.4 32.77	38.7 33.26	KHz
$T_{START,LSI}$	LSI Start up time		50	75	150	us
IDD	Current consumption		0.2	0.25	0.35	uA
LSI_{DUTY}	Duty cycle		45	50	55	%
LSI_{ACC}	LSI Frequency accuracy	VDD=2.5~5.5V, T_A =-40~85℃	-2.0	±1	+2.0	
		VDD=2.5~5.5V, T_A =-40~85℃	-1.5	±1	+1.5	
External High Speed Clock						
HSE	HSE	External high speed RC oscillator clock	4	16	24	MHz
$T_{START,HSE}$	HSE Start up time		—	250	—	us
IDD	Current consumption	XTAL=24MHz, ESR=30Ω, HSE_{LOAD}=12pF	—	300	—	uA
HSE_{DUTY}	Duty cycle		45	50	55	%
HSE_{ESR}	Equivalent resistance		30	60	1500	Ω
HSE_{LOAD}	External load		—	12	—	pF
External Low Speed Clock						
LSE	LSE	External low speed RC oscillator clock	32.75	32.768	32.78	MHz
$T_{START,LSE}$	LSE Start up time		—	2	—	s
IDD	Current consumption	ESR=65KΩ, LSE_{LOAD}=12pF	200	250	350	nA
HSE_{DUTY}	Duty cycle		40	50	60	%
HSE_{ESR}	Equivalent resistance		40	65	85	KΩ
HSE_{LOAD}	External load		—	12	—	pF
SAR ADC Characteristics						
V_{SARIN}	SAR ADC input voltage	Single-ended input	0	—	VDD	V
$VREF_{SAR}$	Reference voltage		—	VDD	—	V
I_{SAR}	SAR ADC input voltage		0.65	0.9	1.23	mA
C_{SAR}	SAR input capacitance		3.5	4	4.5	pF
CLK_{SAR}	SAR ADC sampling clock		0.5	4	16	MHz
T_{SARSH}	SAR S/H time		2	3	4	us
$T_{SARCONV}$	SAR conversion time		16	16	20	cycles
ENOB	Efficient number of bits		10	10.5	11	bits
DNL	SAR differential nonlinearity		-1.5	±1	1.5	LSB
INL	SAR Integral nonlinearity		-2	±1	2	LSB

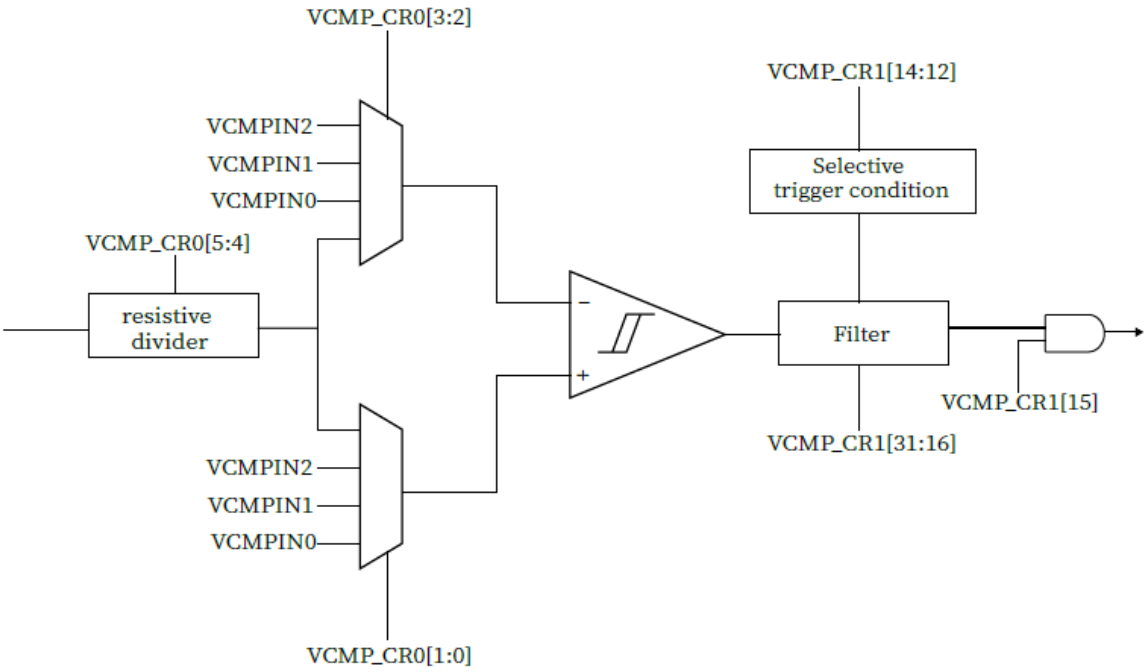
VOS_{SAR}	SAR ADC offset error		-2	±1	2	LSB
GE_{SAR}	SAR ADC gain error		-2	±1	2	LSB
Analog Voltage Comparator						
$V_{IN,CMP}$	Comparator input voltage		0	–		V
$V_{CM,CMP}$	Input Common mode		0	–		V
$V_{OS,CMP}$	Input offset voltage		-10	±5	10	mV
I_{CMP}	Current consumption		–	12	–	uA
$T_{D,CMP}$	Response time		–	5	–	us
Low Voltage Detection						
V_{LVD}	LVD threshold voltage	LVD_CR[3:0] = 0000	Typ.-0.1	4.4	Typ.+0.1	V
		LVD_CR[3:0] = 0001		4.0		
		LVD_CR[3:0] = 0010		3.6		
		LVD_CR[3:0] = 0011		3.3		
		LVD_CR[3:0] = 0100		3.1		
		LVD_CR[3:0] = 0101		2.9		
		LVD_CR[3:0] = 0110		2.7		
		LVD_CR[3:0] = 0111		2.5		
I_{LVD}	LVD current		1	1.5	2	uA
T_{LVD}	LVD delay time	Triggering delayed	30	50	80	us
$T_{SETUP,LVD}$	LVD setup time		3	5	10	us
Low Power Mode Wakeup Time						
T_{WAKEUP}	Deep sleep mode wake up time	4MHz	11.8	12.5	12.8	us
		8MHz	11.3	11.6	12.5	
		16MHz	11.2	11.4	12.0	
		24MHz	10.5	11.3	11.8	
Flash Memory Characteristics						
EC_{NVM}	Block erase cycles		20K	–	–	Cycles
RET_{NVM}	Data retention		20	–	–	Year
T_{PROG}	Programming time		–	–	20	us
$T_{ERASE,BLOCK}$	Block erase time		–	–	8	ms
$T_{ERASE,CHIP}$	Chip erase time		20	–	40	ms

Signal Chain Networking

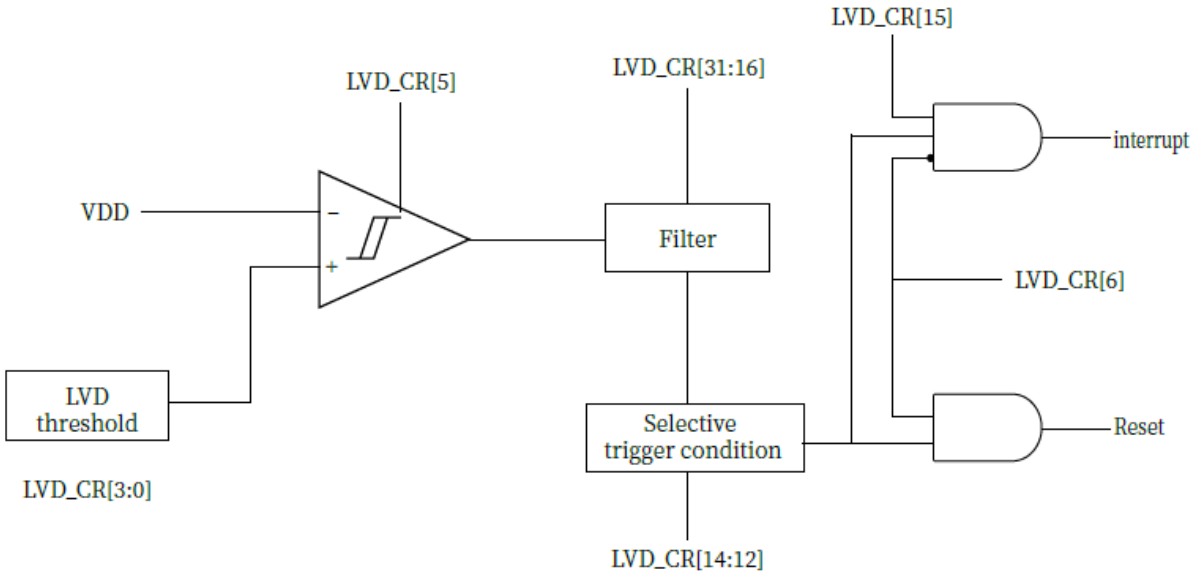
- **SAR ADC Singal network**



■ Analog voltage comparator network



■ Low voltage detection (LVD) network



FE82100 Memory Map

Bus	Address	Size	Module
	0xE000_0000 ~ 0xE00F_FFFF	1MB	M0+ peripheral
	0x4003_0000 ~ 0XDFFF_FFFF		Reserved
AHB	0x4002_1000 ~ 0x4002_1FFF	1K	GPIOD
	0x4002_1000 ~ 0x4002_1BFF	1K	GPIOC
	0x4002_1000 ~ 0x4002_17FF	1K	GPIOB
	0x4002_1000 ~ 0x4002_13FF	1K	GPIOA
	0x4002_0C00 ~ 0x4002_0FFF	1K	reserved
	0x4002_0800 ~ 0x4002_0BFF	1K	CRC16
	0x4002_0400 ~ 0x4002_07FF	1K	FMC
	0x4002_0000 ~ 0x4002_03FF	1K	RCC
	0x4002_5400 ~ 0x4001_FFFF	1K	reserved
APB	0x4000_5000 ~ 0x4000_53FF	1K	LPUART
	0x4000_4C00 ~ 0x4000_4FFF	1K	DEBUG
	0x4000_4800 ~ 0x4000_4BFF	1K	BEEP
	0x4000_4400 ~ 0x4000_47FF	1K	LPTIM
	0x4000_4000 ~ 0x4000_43FF	1K	LVD/VCMP
	0x4000_3C00 ~ 0x4000_3FFF	1K	TIM2
	0x4000_3800 ~ 0x4000_3BFF	1K	OWIER
	0x4000_3400 ~ 0x4000_37FF	1K	CLKTRIM
	0x4000_3000 ~ 0x4000_33FF	1K	RTC
	0x4000_2C00 ~ 0x4000_2FFF	1K	ADC
	0x4000_2800 ~ 0x4000_2BFF	1K	AWK
	0x4000_2400 ~ 0x4000_27FF	1K	IWDT
	0x4000_2000 ~ 0x4000_23FF	1K	WWDT
	0x4000_1C00 ~ 0x4000_1FFF	1K	SYSCON
	0x4000_1800 ~ 0x4000_1BFF	1K	TIM10/11
	0x4000_1400 ~ 0x4000_17FF	1K	PCA
	0x4000_1000 ~ 0x4000_13FF	1K	TIM1
	0x4000_0C00 ~ 0x4000_0FFF	1K	I2C
	0x4000_0800 ~ 0x4000_0BFF	1K	SPI
	0x4000_0400 ~ 0x4000_07FF	1K	UART2
	0x4000_0000 ~ 0x4000_03FF	1K	UART1
AHB	0x2000_1000 ~ 0x3FFF_FFFF		Reserved
	0x2000_0000 ~ 0x2000_0FFF	4K	SRAM
	0x1800_0100 ~ 0x1FFF_FFFF		Reserved
	0x1800_0000 ~ 0x1800_00FF	256	System configuration
	0x0800_0200 ~ 0x17FF_FFFF		Reserved
	0x0800_0000 ~ 0x0800_01FF	512	Byte option
	0x0001_0000 ~ 0x07FF_FFFF		Reserved
	0x4000_0000 ~ 0x0000_FFFF	64K	Main Flash memory

Device Description

■ Core

The core of the FE82100 is the ARM ® Cortex™-M0+ processor, capable of running at speeds up to 24 MHz, and offering a the MCU to attain both high performance and low power consumption.

■ Flash and SRAM

The FE82100 embedded 64KB Flash memory and 4KB of SRAM memory for storing user application code and data.

■ Cyclic Redundancy Check (CRC)

CRC calculations are a calculation method that divides this message polynomial by a constant called the generating polynomial. (the polynomial $F(x) = X^{16} + X^{12} + X^5 + 1$ given in ISO/IEC13239). It offers a mechanism for validating storage errors in flash memory, computing the real-time signature of the software, and comparing the generated signatures throughout software execution.

■ Power Supply

The FE82100 supply voltage VDD ranges from 2.5V to 5.5V. All input/output (IO) and internal voltage regulators are externally powered via the VDD pin.

■ POR/BOR/LVD

The FE82100 integrates power-on reset (POR) and brown-out reset (BOR) to ensure the system voltage, and reset when the system voltage above a threshold of 2.5V. Besides, to avoid lowering the frequency or registering incorrect information in a low voltage environment, the Low Voltage Detection (LVD) utilizes programmable software to monitor the voltage and interrupt the system when the voltage falls below the set value, giving the software a window to handle the voltage abnormality.

■ Unique ID (UID)

The FE82100 are shipped with a unique 16-byte device identification number. (0x180000F0-0x180000FF).

■ Nested Vectored Interrupt Controller (NVIC)

The FE82100 embedded a NVIC, which is part of the ARM Cortex-M processor. It is responsible for real-time control, handling exceptions and interrupting related programs.

- Up to 32 interrupt requests (IRQ) Input
- Early processing of interrupts
- Handle late-arriving higher-level interrupts
- 4 interrupt priority levels
- Provide low-latency interrupt handling
- The entry address of the interrupt vector leads directly to the core
- Tightly coupled NVIC interface

Interrupt Controller					
Ext. interrupt	**Address**	**Interrupt source**	**Name**	**Wake up from sleep**	**Wake up from deep sleep**
0	0x0000 0040	GPIO_PA	GPIOA Interrupt	Yes	Yes
1	0x0000 0044	GPIO_PB	GPIOB Interrupt	Yes	Yes
2	0x0000 0048	GPIO_PC	GPIOC Interrupt	Yes	Yes
3	0x0000 004C	GPIO_PD	GPIOD Interrupt	Yes	Yes
4	0x0000 0050	Flash	Flash Interrupt	No	No
5	0x0000 0054	Reserve	-	-	-
6	0x0000 0058	UART1	UART1 Interrupt	Yes	No
7	0x0000 005C	UART2	FUART2 INT	Yes	No
8	0x0000 0060	LPUART	LPUART INT	Yes	Yes
9	0x0000 0064	Reserve	-	-	-
10	0x0000 0068	SPI	SPI INT	Yes	No
11	0x0000 006C	Reserve	-	-	-
12	0x0000 0070	I2C	I2C INT	Yes	No
13	0x0000 0074	Reserve	-	-	-
14	0x0000 0078	TIM10	TIM10 INT	Yes	No
15	0x0000 007C	TIM11	TIM11 INT	Yes	No
16	0x0000 0080	LPTIM	LPTIM INT	Yes	Yes
17	0x0000 0084	Reserve	-	-	-
18	0x0000 0088	TIM1	TIM1 INT	Yes	No
19	0x0000 008C	TIM2	TIM2 INT	Yes	No
20	0x0000 0090	Reserve	-	-	-
21	0x0000 0094	PCA	PCA INT	Yes	No
22	0x0000 0098	WWDG	WWDG INT	Yes	No
23	0x0000 009C	IWDG	IWDG INT	Yes	Yes
24	0x0000 00A0	ADC	ADC INT	Yes	No
25	0x0000 00A4	LVD	LVD INT	Yes	Yes
26	0x0000 00A8	VCMP	VCMP INT	Yes	Yes
27	0x0000 00AC	Reserve	-	-	-
28	0x0000 00B0	AWK	AWK INT	Yes	Yes
29	0x0000 00B4	OWIRE	OWIRE INT	Yes	No
30	0x0000 00B8	RTC	RTC INT	Yes	Yes
31	0x0000 00BC	CLKTRIM	CLKTRIM INT	Yes	Yes

System Reset

The FE82100 has 9 reset sources, each reset source can trigger the system reset which reset most of the registers, the program counter will point to the reset address (0x0000 0000).

- Power-on reset (POR) and brown-out reset (BOR)
- External Reset Pin (ERP) reset
- Independent watchdog reset
- Window watchdog reset
- Software reset
- Low Voltage Detect (LVD) reset
- Lockout reset
- CPURST reset
- MCURST reset

Clock

- 4M~24MHz external high-speed crystal oscillator (HSE)
- 32.768KHz external low-speed crystal oscillator(LSE)
- 4M~24MHz internal high-speed clock (HSI)
- 32.768KHz/38.4KHz internal low-speed clock (LSI)

Internal RC frequency deviation over full voltage and full temperature range<±2.5%.

While system clock selection startup, the internal high-speed oscillator is selected as default CPU clock on reset.

Voltage Regulator

The voltage regulator powers the internal circuitry and the VCAP capacitor is connected externally.

Power Mode

The FE82100 supports 3 working modes:

- Run mode: The CPU core and peripheral modules continue to operate.
- Sleep mode: The core clock is turned off. Only the CPU halted. All peripherals continue to operate and wake up the CPU when an interrupt/event occurs.
- Deep-sleep mode: The main clock is turned off. The CPU core and peripherals are halted, only the low-power modules continue to operate.

The system clock operates on 38.4/32.768 KHz low-speed frequency, which can be interrupted by RTC, AWK or external interrupt to wake up the chip device. In the normal operate mode, you can choose to work in frequency division mode or turn off the clock of some unused peripherals to achieve flexible switching between power consumption and performance.

Real Time Clock (RTC)

The real-time clock provides a set of continuous counting counters, which can be configured by software to provide clock calendar functions, and can also provide warning interrupts and periodic interrupts.

I²C Bus

I²C bus is a serial communication bus that uses a multi-master-slave architecture to establish communication between two or more different circuits. They can support standard, fast and high-speed modes, the maximum data transmission speed can reach 1Mbps.

Universal Asynchronous Receiver/Transmitter (UART1/UART2)

The UART is a computer hardware device designed for asynchronous serial communication, allowing configurable data formats and transmission speeds. This device transmits data bits individually, from the least significant to the most significant, framed by start and stop bits to ensure precise timing managed by the communication channel.

The FE82100 has 2 UART for asynchronous communication.

Automatic Wake-up Timer (AWK)

The AWK is a pivotal component in electronic systems designed to manage and optimize power consumption by facilitating automated wake-up events. This timer is specifically engineered to enhance energy efficiency in devices by allowing them to enter low-power states and periodically wake up to perform necessary tasks. The time base is clocked by the internal low speed RC oscillator clock (LSI) or by the prescaled HSE crystal clock.

Clock Trim/Monitoring Module (CLKTRIM)

The clock calibration circuit embedded in the FE82100 allows for the calibration of the internal RC clock using either an external precise crystal oscillator clock or the internal RC clock to verify the proper functioning of the external crystal oscillator clock.

Embedded Debug System

The Embedded Debug System typically includes features such as real-time debugging, breakpoints, watchpoints, and trace capabilities, which cooperates with standard mature Keil/IAR and other debugging and development software, allowing developers to gain insights into the behavior of the embedded system during runtime.

Supports 4 hard breakpoints and multiple soft breakpoints.

Embedded Debug (DBG)

An encrypted embedded debugging solution that provides a full-featured real-time debugger.

■ Timers and Watchdogs

The FE82100 includes 1 advanced timer,1 general purpose timer,1 programmable counter, 2 basic timer,1 low power timer,1 window watchdog,1 stand-alone watchdog and 1 Systick (SysTick) Timer.

Timer and Watchdogs							
Timer Type	**Name**	**Counter**	**Prescaler**	**Counting Direction**	**Complementary output**	**PWM**	**Capture Compare Channel**
Advanced	TIM1	16 bits	1/2/4/8/16/64/256/1024	Increase, Decrease, Increase/Decrease	3 pairs	Yes	4
General	TIM2	16 bits	1/2/4/8/16/64/256/1024	Increase, Decrease, Increase/Decrease	No	Yes	4
PCA	PCA	16 bits	2/4/8/16/32	Increase	No	Yes	5
Low Power	LPTIM	16 bits	No	Increase	No	No	No
Basic	TIM10	16/32 bits	1/2/4/8/16/32/64/128	Increase	No	No	No
	TIM11	16/32 bits	1/2/4/8/16/32/64/128	Increase	No	No	No

- Advanced Timer (TIM1)

1 advanced control timer(TIM1) can be seen as a three-phase PWM generator assigned to 6 channels, It has a complementary PWM output with dead-time insertion and can also be used as a complete general-purpose timer. Four independent channels can be used for:

- Input capture
- Output comparison
- Generate PWM (edge or center aligned)
- Single-shot pulse output TIM1 the same function as TIM2 timer when configured as 16-bit general-purpose timer. It has full modulation capability(0~100%)when configured as 16-bit PWM generator.

In debug mode, the timers can be frozen and the PWM outputs disabled, cutting off the power switches controlled by these outputs. The Advanced Timer shares most functions and has an identical internal structure to the general timer, allowing it to collaborate with the TIM timer through the timer link function, offering synchronization or event linking capabilities.

- General Purpose Timer (TIM2)

The FE82100 has a 16-bit autoload up/down counter, a 16-bit prescaler and four independent channels. Each channel can be used for input capture, output compare, PWM and single-pulse mode output. Furthermore, these channels can work with Advanced Timers through the timer link function, offering synchronization or event chaining capabilities. In debug mode, the counter can be frozen, and any general-purpose timer can be utilized to generate PWM outputs.

- **Programmable Counter Array (PCA)**

The PCA supports up to five 16-bit capture/comparison modules. These timing/counters serve as general-purpose clock counting/event counters for capture/comparison functions. Each channel of the PCA can be individually programmed to provide input capture/output compare or pulse width modulation.

- **Low Power Timer (LPTIM)**

The LPTIM are optional 16-bit timers. Even the system clock is deactivated, they can still count by LSI or LSE, allowing the system to be awakened from low power mode by an interrupt.

- **Basic Timer (TIM10/11)**

The Basic Timer consists of 2 16/32-bit selectable timers, TIM10 and TIM11. Both them have same functions, operating as synchronous timers with the flexibility to choose between heavy load mode and non-heavy load mode. They are capable of counting external pulses or serving as a system timer.

- **Independent Watchdog (IWDG)**

The IWDG is a 20-bit down counter, driven by an internal independent LSI. Because the internal LSI operates independently of the main clock, it remains count even in shutdown and standby modes. This watchdog can function as a safety mechanism to reset the device in case of CPU malfunctions or as a free-running timer for application timeout management. The counters can be frozen in debug mode for effective troubleshooting.

- **System Watchdog (WWDG)**

The WWDG is based on an 8-bit down-counter with a 20-bit prescaler, driven by the APB clock (PCLK) as the action clock source. It functions as a watchdog to reset the device in the event of system issues, includes an early warning interrupt feature, and allows the counters to be frozen in debug mode.

- **SysTick Timer (SysTick)**

The SysTick is designed for real-time operating systems but can also function as a standard down counter, possessing the following properties:

- 24-bit down counter
- Auto-reload function
- Generate a maskable system interrupt when the counter counts to 0
- Programmable clock source (HCLK or HCLK/4)

■ Low Power Universal Asynchronous Receiver/Transmitter (LPUART)

The FE82100 has 1 LPUART that can work in low power mode, providing asynchronous communication.

■ Serial Peripheral Interface (SPI)

The SPI is capable of communicating at rates up to 12Mb/s in full‑duplex and simplex communication modes, master and slave modes.

■ General Purpose Input/Output (GPIO)

GPIO can awaken the MCU from both edge-triggered and level-triggered interrupts, turn it to work mode. Each of these interrupts can be software configured as either a push-pull or open-drain output without pull-up/pull-down. The output drive capability is configurable, and the maximum drive current is 12mA. Generic IO supports external asynchronous interrupts.

■ Analog to Digital Converter (ADC)

The 12-bit SAR ADC achieves a sampling rate of 1MSPS when operating with a 16MHz ADC clock. The power supply can serve as the reference voltage. The 20 Pin package contains 7 external channels, and the 32 Pin package contains 16 external channels. The ADC supports single, scan, and cycle conversion modes, automatically converting on a selected set of analog inputs in scan/loop mode.

- Input voltage range: 0 to VCC
- Conversion cycles: 16/20 clock cycles
- Support trigger ADC from external terminals, internal TIM1, TIM2, TIM10/11, voltage comparator etc.
- End of Conversion (EOC) Interrupt

■ Voltage Comparator (VCMP)

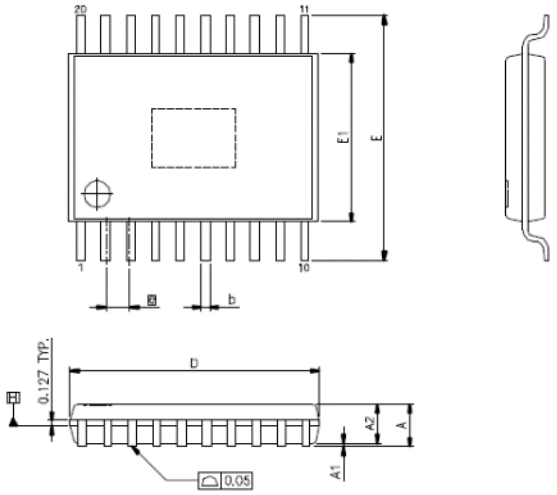
There are three configurable positive/negative external input channels and one internal bandgap reference voltage (FE82100=2.5V). The VCMP output is accessible for timers TIM1, TIM10/11, LPTIM, and PCA, supporting capture, gating, and external count usage. Asynchronous interrupts can be generated based on rising or falling edges, providing the capability to wake up the MCU from low power mode.

■ Buzzer (BEEP)

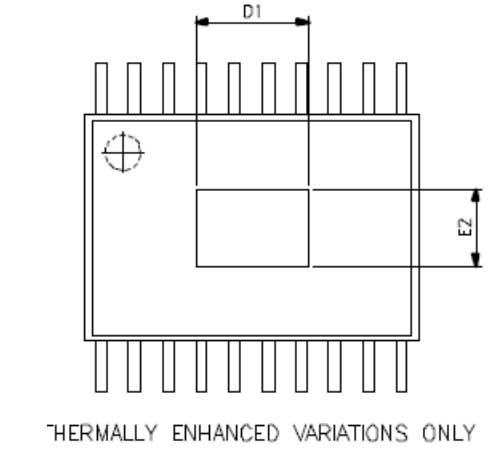
A 1/2/4KHz BEEP signal can be generated on the BEEP pin, which is used to drive the external buzzer. The Buzzer is often programmable, enabling developers to control the frequency, duration, and intensity of the emitted sound.

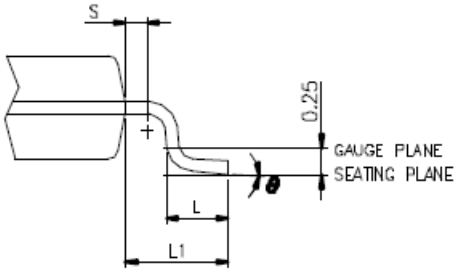
The FE82100 embedded 2 basic timers TIM10/11 and 1 LPTIM can function as multiplexed outputs.

Package Outline Dimensions



SYMBOLS	MIN.	TYP.	MAX.
A	—	—	1.20
A1	0	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
D	6.4	6.5	6.6
E1	4.3	4.4	4.5
e	6.40 BSC		
E	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.2	—	—
θ	0	—	8^{O}





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