EN25QT256A (2V)
256 Megabit 3.3V Serial Flash Memory with 4Kbyte Uniform Sector

FEATURES

- Single power supply operation
  - Full voltage range: 2.3-3.6V
- Serial Interface Architecture
  - SPI Compatible: Mode 0 and Mode 3
- 256 M-bit Serial Flash
  - 256 M-bit / 32,768 KByte / 131,072 pages
  - 256 bytes per programmable page
- Standard, Dual or Quad SPI
  - Standard SPI: CLK, CS#, DI, DO, WP#, HOLD#
  - Dual SPI: CLK, CS#, DQ_0, DQ_1, WP#, HOLD#
  - Quad SPI: CLK, CS#, DQ_0, DQ_1, DQ_2, DQ_3
- High performance
  - 166MHz Single, Dual/Quad SPI Fast Read
  - 108MHz Normal Read
  - 108 MHz DTR Read
  - Configurable dummy cycle number for fast read operation
- Low power consumption
  - 6mA typical active current
  - 12μA typical standby current
  - 0.5μA typical deep power down current
- Uniform Sector Architecture
  - 8,192 sectors of 4-Kbyte
  - 512 blocks of 64-Kbyte
  - 1,024 blocks of 32-Kbyte
  - Any sector or block can be erased individually
- Software and Hardware Write Protection
  - Write Protect all or portion of memory via software
  - Enable/Disable protection with WP# pin
- High performance program/erase speed
  - Page program time: 0.25ms typical
  - Sector erase time: 25ms typical
  - 32KB Block erase time 80ms typical
  - 64KB Block erase time 120ms typical
  - Chip erase time: 40 Seconds typical
- Write suspend and Write resume
- Volatile Status Register Bits.
- Lockable 3x2048 byte OTP security sectors
- Support Serial Flash Discoverable Parameters (SFDP) signature
- Read 128-bit Unique ID Number
- More than 100K endurance cycles
- More than 20-year data retention
- Package Options
  - VDFN / WSON8 6x8mm
  - All Pb-free packages are compliant RoHS, Halogen-Free and REACH.

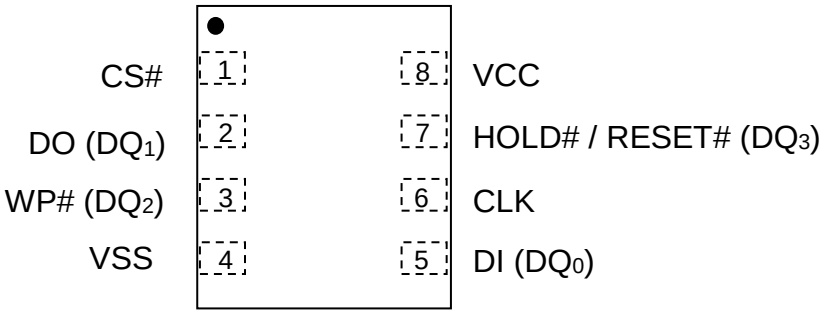
GENERAL DESCRIPTION

The device is a 256 Megabit (32,768K-byte) Serial Flash memory, with advanced write protection mechanisms. The device supports the single bit and four bits serial input and output commands via standard Serial Peripheral Interface (SPI) pins: Serial Clock, Chip Select, Serial DQ_0 (DI) and DQ_1 (DO), DQ_2 (WP#) and DQ_3 (HOLD#/RESET#). The memory can be programmed 1 to 256 bytes at a time, using the Page Program instruction.

By providing the ability to protect and unprotect blocks, a system can unprotect blocks to modify their content while keeping the remaining blocks of the memory array securely protected. This is useful in applications where program code is patched or updated on a subroutine or module basis or in applications where data storage segments need to be modified without running the risk of errant modifications to the program code segments.

The device is designed to allow either single Sector/Block at a time or full chip erase operation. The device can be configured to protect part of the memory as the software protected mode. This device can sustain a minimum of 100K program/erase cycles on each sector or block.

CONNECTION DIAGRAMS (TOP VIEW)



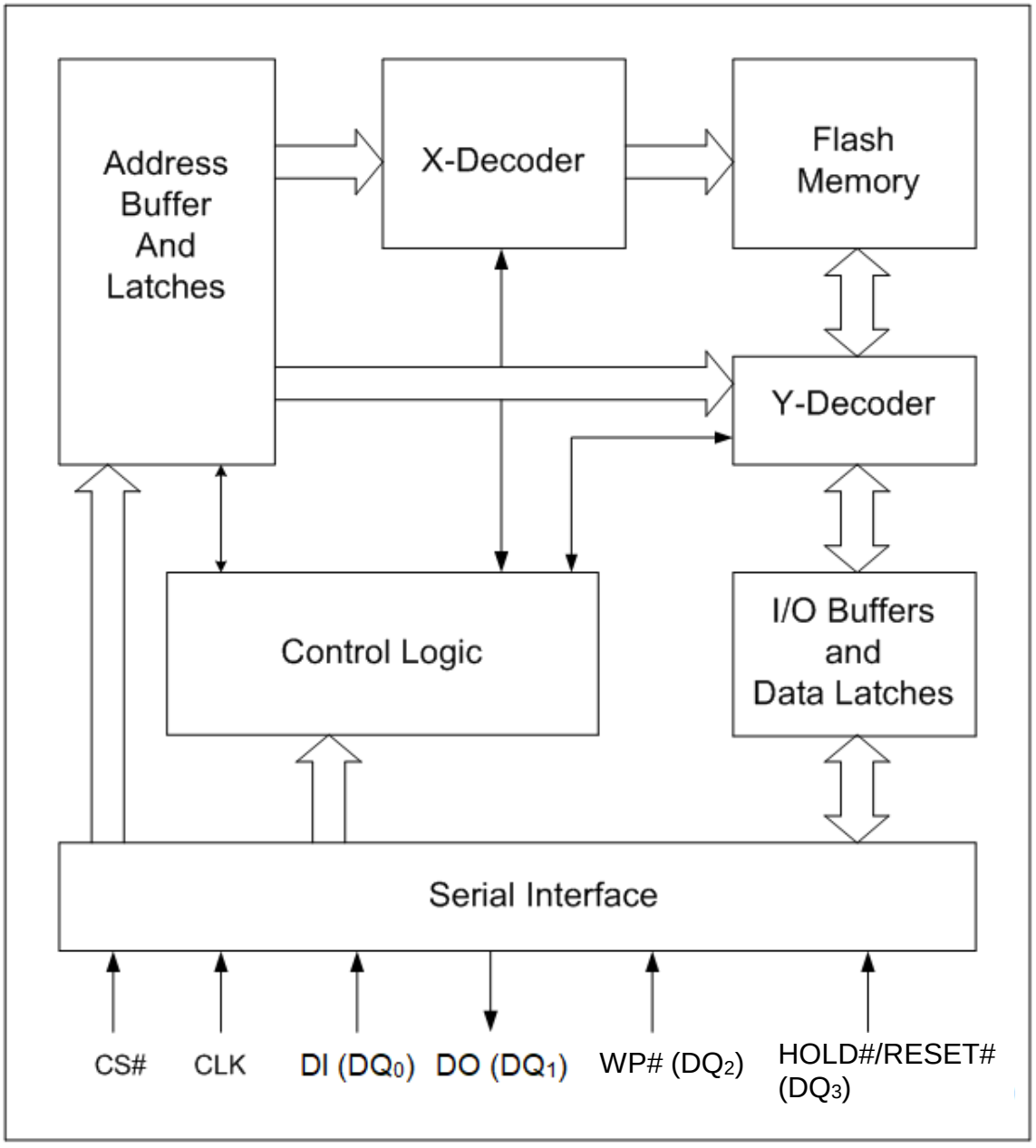
USON / DFN / WSON

Pin Names

Symbol	I/O	Pin Name
CLK	I	Power Supply
DI (DQ_0)	I/O	Data Input (Data Input Output 0)[1]
DO (DQ_1)	I/O	Data Output (Data Input Output 1)[1]
CS#	I	Chip Select Input
WP# (DQ_2)	I/O	Write Protect Input (Data Input Output 2)[2]
HOLD#/RESET# (DQ_3)	I/O	HOLD or RESET Input (Data Input Output 3)[2]
V_{SS}		Ground
V_{CC}		Power Supply

Note:
1. DQ_0 and DQ_1 are used for Standard and Dual SPI instructions.
2. DQ_0 ~ DQ_3 are used for Quad SPI instructions, WP# & HOLD# (or RESET#) functions are only available for Standard/Dual SPI.
   Factory default for Quad Enabled part numbers with differentiation code. (**Please refer to ORDERING INFORMATION**).

BLOCK DIAGRAM



SIGNAL DESCRIPTION

Serial Data Input, Output and IOs (DI, DO and DQ_0, DQ_1, DQ_2, DQ_3)

The device support standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge CLK.

Dual and Quad SPI instruction use the bidirectional IO pins to serially write instruction, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. The Quad SPI instructions demand that the non-volatile Quad Enable bit (QE) in Status Register-2 be set. When QE=1, the WP# pin turns into DQ_2 and HOLD#/RESET# pin becomes DQ_3.

Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides timing for serial input and output operations.

Chip Select (CS#)

The SPI Chip Select (CS#) pin enables and disables the device. When CS# is high, the device is deselected and the serial data output (DO, or DQ_0, DQ_1, DQ_2, DQ_3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle in progress. When CS# is low the device will be selected, power consumption will increase to the active levels and instructions can be written to and data read from the device. After power-up, CS# must change from high to low before a new instruction will be accepted. The CS# input must track the V_{CC} supply level at power-up and power-down (as indicated in “Write Protection”). Note that there was an internal pull-up resistor on the CS# pin to achieve this.

Write Protect (WP#)

The WP# pin can be configured to prevent the Status Register from being written. When the Status Register’s Block Protect (CMP, BP4, BP3, BP2, BP1 and BP0) bits work together with the Status Register Protect (SRP) bits, can be protected by hardware protected, the WP# pin is active low. When the QE =1 is set to Quad I/O, the WP# pin function is not available as WP# pin is used for DQ_2. Note that there was an internal pull-up resistor on the WP# pin to avoid accidentally trigging WP function by pin floating.

HOLD (HOLD#)

The HOLD# pin allows the device to be paused while it is actively selected. When HOLD# is set low, the DO pin will be under high impedance as CS# is low and the signals on the DI and CLK pins will be ignored (don’t care). When HOLD# is set high, device operation can be resumed. The HOLD# function can be helpful when multiple devices share the same SPI signals. The HOLD# pin is active low. When the QE = 1, the HOLD# pin function is not available since this pin is being used for DQ_3. Note that there was an internal pull-up resistor on the HOLD# pin to avoid accidentally trigging HOLD function by pin floating.

RESET (RESET#)

The RESET# pin enables the controller to reset the device(HRSW=1). For 8-pin packages, when QE=0, the DQ_3 pin can be configured as either the HOLD# pin or the RESET# pin, depending on Status Register setting. When QE=1, the HOLD# or RESET# function is not available for the 8-pin configuration. Note that there was an internal pull-up resistor on the RESET# pin to avoid accidentally trigging RESET function by pin floating.

MEMORY ORGANIZATION

The memory is organized as:

- 33,554,432 bytes
- Uniform Sector Architecture
  512 blocks of 64-Kbyte
  1,024 blocks of 32-Kbyte
  8,192 sectors of 4-Kbyte
  131,072 pages (256 bytes each)

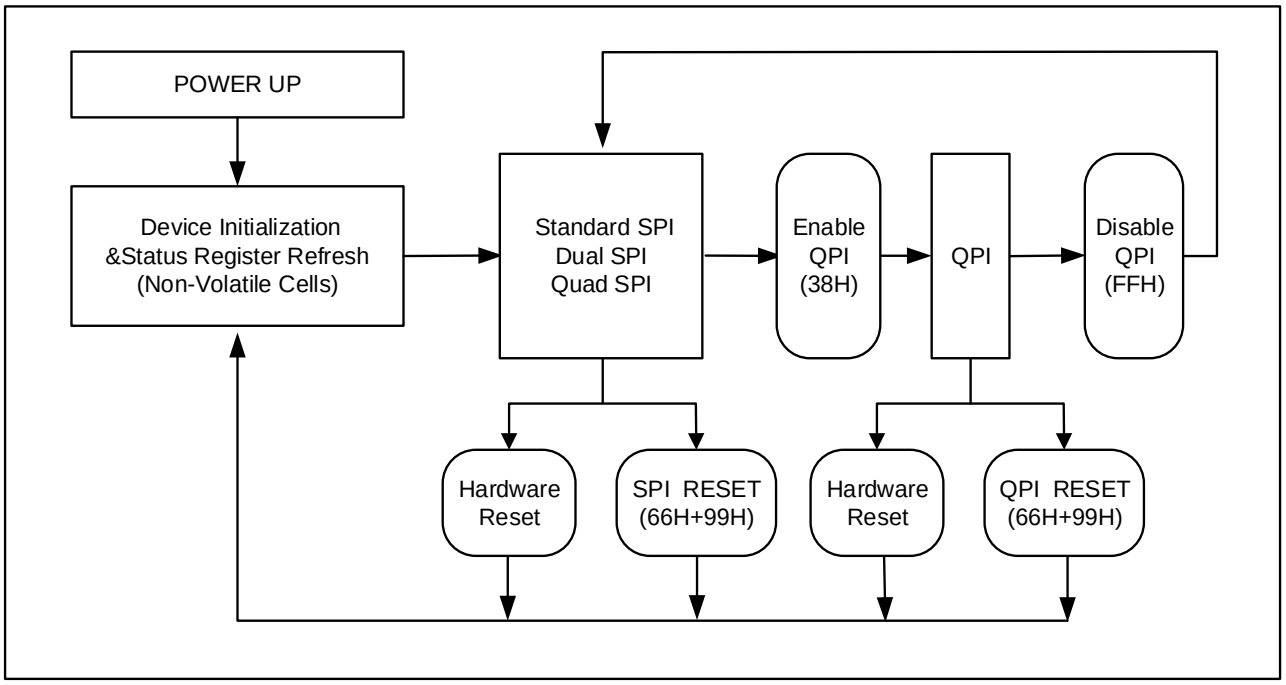
Each page can be individually programmed (bits are programmed from 1 to 0). The device is Sector, Block or Chip Erasable but not Page Erasable.

Uniform Block Sector Architecture

64KB Block	32KB Block	Sector	Address range		64KB Block	32KB Block	Sector	Address range	
511	1023	8191	1FFF000h	1FFFFFFh	255	511	4095	0FFF000h	0FFFFFFh
	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮
	1022	8176	1FF0000h	1FF0FFFh		510	4080	0FF0000h	0FF0FFFh
510	1021	8175	1FEF000h	1FEFFFFh	254	509	4079	0FEF000h	0FEFFFFh
	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮
	1020	8160	1FE0000h	1FE0FFFh		508	4064	0FE0000h	0FE0FFFh
509	1019	8159	1FDF000h	1FDFFFFh	253	507	4063	0FDF000h	0FDFFFFh
	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮
	1018	8144	1FD0000h	1FD0FFFh		506	4048	0FD0000h	0FD0FFFh
508	1017	8143	1FCF000h	1FCFFFFh	252	505	4047	0FCF000h	0FCFFFFh
	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮
	1016	8128	1FC0000h	1FC0FFFh		504	4032	0FC0000h	0FC0FFFh
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
259	519	4159	103F000h	103FFFFh	3	7	63	003F000h	003FFFFh
	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮
	518	4144	1030000h	1030FFFh		6	48	0030000h	0030FFFh
258	517	4143	102F000h	102FFFFh	2	5	47	002F000h	002FFFFh
	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮
	516	4128	1020000h	1020FFFh		4	32	0020000h	0020FFFh
257	515	4127	101F000h	101FFFFh	1	3	31	001F000h	001FFFFh
	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮
	514	4112	1010000h	1010FFFh		2	16	0010000h	0010FFFh
256	513	4111	100F000h	100FFFFh	0	1	15	000F000h	000FFFFh
	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮
	512	4096	1000000h	1000FFFh		0	0	0000000h	0000FFFh

OPERATING FEATURES

SPI / QPI Operations



Serial Flash Memory Operation Diagram

Standard SPI Instructions

The device is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (DI) and Serial Data Output (DO). Both SPI bus mode 0(0, 0) and mode 3(1, 1) are supported. The Input data is latched on the rising edge of CLK and data shifts out on the falling edge of CLK. For Mode 0, the CLK signal is typically low on the falling and rising edges of CS#. For Mode 3, the CLK signal is typically high on the falling and rising edges of CS#.

Dual SPI Instructions

The flash supports Dual SPI operations when using “Fast Read Dual Output (3Bh/3Ch)” and “Fast Read Dual I/O (BBh/BCh)”. These instructions allow data to be transferred to or from the device at twice the rate of the standard SPI. When working in the Dual SPI instructions, the DI and DO pins act as bidirectional I/O pins: DQ_0 and DQ_1.

Quad SPI Instructions

When using the “Quad Output Fast Read” and “Quad I/O Fast Read” (6BH/6Ch, EBH/ECh) instructions, the Quad SPI operation is supported in the device. These instructions allow data to be transferred to or from the device at four times the rate of the standard SPI. When working in the Quad SPI instructions, the DI and DO pins act as bidirectional I/O pins: DQ_0 and DQ_1, and the WP# and HOLD# pins act as bidirectional I/O pins: DQ_2 and DQ_3. The Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register set to 1.

SPI / QPI DTR Read Instructions

Throughput of read operations can be effectively improved without increasing the serial clock frequency by device introducing multiple DTR (Double Transfer Rate) Read instructions that support Standard/Dual/Quad SPI and QPI modes. Similar to all other SPI/QPI instructions, the Byte-long instruction code is still latched into the device on the rising edge of the serial clock. When the device uses the DTR instruction code, the address input and data output will be latched on the rising and falling edges of the serial clock.

QPI Instructions

The device supports Quad Peripheral Interface (QPI) operations when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the “Enable the QPI (38H)”. The QPI mode utilizes all four IO pins to input the command code with less serial clocks to improve system performance in an XIP environment.

Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given times. The “Enter QPI (38h)” and “Exit QPI (FFh)” instructions are applied to switch the device between these two modes.

Upon power-up or after a software reset with “Reset (99h)” instruction, the default state of the device is Standard/Dual/Quad SPI mode. The QPI commands require the non-volatile bit, QE =1. When the QPI instruction is under function, the DI and DO pins become bidirectional DQ_0 and DQ_1, and the WP# and HOLD# pins become DQ_2 and DQ_3 respectively.

3-Byte / 4-Byte Address Modes

The device provides two Address Modes that can be used to specify any byte of data in the memory array. The 3-Byte Address Mode is backward compatible to older generations of serial flash memory that only support up to 128M-bit data. To address the 256M-bit or more data in 3-Byte Address Mode, Extended Address Register must be used in addition to the 3-Byte addresses. 4-Byte Address Mode is designed to support Serial Flash Memory devices from 256M-bit to 32G-bit. The extended Address Register is not necessary when the 4-Byte Address Mode is enabled.
Upon power up, the device can operate in 3-Byte Address Mode or 4-Byte Address Mode, depending on ADP (SR3.1) bit setting. If ADP=0(default), the device will operate in 3-Byte Address Mode; if ADP=1, the device will operate in 4-Byte Address Mode. To switch between the 3-Byte or 4-Byte Address Modes, “Enter 4-Byte Mode (B7h)” or “Exit 4-Byte Mode (E9h)” instructions must be used. The current address mode is indicated by ADS (SR3.0).

This device also supports a set of basic SPI instructions which requires dedicated 4-Byte address regardless the device Address Mode setting. Please refer to Instruction Set for details.

Hold Function

The HOLD# signal is designed to give the device to suspend operation when actively selected (when CS# is low) in Standard / Dual SPI operations. The HOLD function is available when QE=0. If QE=1, The HOLD function is disabled, and the HOLD# pin acts as dedicated data I/O pin. The HOLD# signal goes low to stop any communications with the device, except the operation in progress.
The operation of HOLD needs CS# keep low, and starts on falling edge of the HOLD# signal, with CLK signal being low. The HOLD condition ends on rising edge of HOLD# signal with CLK being low. The DO is high impedance, both DI and CLK don't care during the HOLD operation. When CS# is driven high during HOLD operation, the internal logic of the device will be reset. To re-start communication with the chip, the HOLD# must be at high and then CS# must be at low.

Software Reset & Hardware RESET# pin

The software Reset sequence allows the device to reset to the initial power on state (SPI/QPI mode) which must consist of two consecutive commands: Enable Reset (66h) & Reset (99h). The device can also be configured under the hardware RESET# pin for the WSON-8 package types. The HRSW bit is set for either HOLD# pin or RESET pin function. When the HRSW=0 (default) and HRSW=1, the pin acts as the HOLD# pin and RESET# pin respectively. When the QE = 1, the HOLD# or RESET# function will be disabled and the pin will act as DQ_3.
The hardware RESET# pin has the highest priority at all of input signals.
It will take approximately t_{SR} for the device to restore if the command sequence is successfully received, and no commands will be accepted during reset. Any on-going external/internal operations will be interrupted by driving RESET# low for a minimum period of ~1us (t_{RESET}*), regardless the status of other SPI signals (CS#, CLK, IOs, WP# and/or HOLD#).

Note: While a faster RESET# pulse (as short as a few hundred nanoseconds) generally resets the device, a minimum of 1us is recommended to ensure reliable operation.

Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the device provides the following data protection mechanisms:

Write Protect Features

- Reset of the device will be triggered when V_{CC} falls below threshold
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (WP# pin) write protection using Status Registers
- Write Protection with Power-down instruction
- Lock Down write protection for Status Register until the next power-up

While V_{CC} below threshold of V_{WI}, all operations are deactivated and no instructions are acceptable. After the V_{CC} voltage exceeds V_{WI}, all program and erase related instructions are further disabled for a time delay of t_{PUW}, including Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register. The CS# must track the V_{CC} level at power-up status until the V_{CC}-min level and t_{VSL} time delay are met, and it must also keep track of the V_{CC} level at power-down status to prevent adverse command sequence as indicated in figure Power-up Timing and Voltage Levels

Note that there was an internal pull-up resistor on the CS# pin to achieve this.

After power-up, the device is automatically rendered write-disabled and the Write Enable Latch (WEL) is set to 0. Before a Page/Erase/Write Status Register instruction can be accepted, a Write Enable instruction must be issued. After the instruction finished, the Write Enable Latch (WEL) is automatically cleared to 0.

Software controlled write protection is achieved by issuing the Write Status Register instruction and setting the Status Register Protect (SRP0, SRP1) and Block Protect (CMP, BP [4:0]) bits. These settings can set parts or the entire memory array as read-only. Used together with the Write Protect (WP#) pin, changes to the Status Register can be activated or deactivated under hardware control.

The Power-down instruction provides an extra level of write protection, as all instructions are omitted except for the Release Power-down instruction.

Protected Area Sizes Sector Organization

STATUS REGISTER[1]						Memory Content			
CMP	BP4	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION
0	0	0	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	0	1	511	01FF0000h - 01FFFFFFh	64KB	Upper 1/512
0	0	0	0	1	0	510 to 511	01FE0000h - 01FFFFFFh	128KB	Upper 1/256
0	0	0	0	1	1	508 to 511	01FC0000h - 01FFFFFFh	256KB	Upper 1/128
0	0	0	1	0	0	504 to 511	01F80000h - 01FFFFFFh	512KB	Upper 1/64
0	0	0	1	0	1	496 to 511	01F00000h - 01FFFFFFh	1MB	Upper 1/32
0	0	0	1	1	0	480 to 511	01E00000h - 01FFFFFFh	2MB	Upper 1/16
0	0	0	1	1	1	448 to 511	01C00000h - 01FFFFFFh	4MB	Upper 1/8
0	0	1	0	0	0	384 to 511	01800000h - 01FFFFFFh	8MB	Upper 1/4
0	0	1	0	0	1	256 to 511	01000000h - 01FFFFFFh	16MB	Upper 1/2
0	0	1	0	1	0	0 to 511	00000000h - 01FFFFFFh	32MB	ALL
0	0	1	0	1	1	0 to 511	00000000h - 01FFFFFFh	32MB	ALL
0	0	1	1	0	0	0 to 511	00000000h - 01FFFFFFh	32MB	ALL
0	0	1	1	0	1	0 to 511	00000000h - 01FFFFFFh	32MB	ALL
0	0	1	1	1	0	0 to 511	00000000h - 01FFFFFFh	32MB	ALL
0	0	1	1	1	1	0 to 511	00000000h - 01FFFFFFh	32MB	ALL
0	1	0	0	0	0	NONE	NONE	NONE	NONE
0	1	0	0	0	1	0	00000000h - 0000FFFFh	64KB	Lower 1/512
0	1	0	0	1	0	0 to 1	00000000h - 0001FFFFh	128KB	Lower 1/256
0	1	0	0	1	1	0 to 3	00000000h - 0003FFFFh	256KB	Lower 1/128
0	1	0	1	0	0	0 to 7	00000000h - 0007FFFFh	512KB	Lower 1/64
0	1	0	1	0	1	0 to 15	00000000h - 000FFFFFh	1MB	Lower 1/32
0	1	0	1	1	0	0 to 31	00000000h - 001FFFFFh	2MB	Lower 1/16
0	1	0	1	1	1	0 to 63	00000000h - 003FFFFFh	4MB	Lower 1/8
0	1	1	0	0	0	0 to 127	00000000h - 007FFFFFh	8MB	Lower 1/4
0	1	1	0	0	1	0 to 255	00000000h - 00FFFFFFh	16MB	Lower 1/2
0	1	1	0	1	0	0 to 511	00000000h - 01FFFFFFh	32MB	ALL
0	1	1	0	1	1	0 to 511	00000000h - 01FFFFFFh	32MB	ALL
0	1	1	1	0	0	0 to 511	00000000h - 01FFFFFFh	32MB	ALL
0	1	1	1	0	1	0 to 511	00000000h - 01FFFFFFh	32MB	ALL
0	1	1	1	1	0	0 to 511	00000000h - 01FFFFFFh	32MB	ALL
0	1	1	1	1	1	0 to 511	00000000h - 01FFFFFFh	32MB	ALL
1	0	0	0	0	0	0 to 511	00000000h - 01FFFFFFh	ALL	ALL

1	0	0	0	0	1	0 to 510	00000000h - 01FEFFFFh	32,704KB	Lower 511/512
1	0	0	0	1	0	0 to 509	00000000h - 01FDFFFFh	32,640KB	Lower 255/256
1	0	0	0	1	1	0 to 507	00000000h - 01FBFFFFh	32,512KB	Lower 127/128
1	0	0	1	0	0	0 to 503	00000000h - 01F7FFFFh	32,256KB	Lower 63/64
1	0	0	1	0	1	0 to 495	00000000h - 01EFFFFFh	31MB	Lower 31/32
1	0	0	1	1	0	0 to 479	00000000h - 01DFFFFFh	30MB	Lower 15/16
1	0	0	1	1	1	0 to 447	00000000h - 01BFFFFFh	28MB	Lower 7/8
1	0	1	0	0	0	0 to 383	00000000h - 017FFFFFh	24MB	Lower 3/4
1	0	1	0	0	1	0 to 255	00000000h - 00FFFFFFh	16MB	Lower 1/2
1	0	1	0	1	0	NONE	NONE	NONE	NONE
1	0	1	0	1	1	NONE	NONE	NONE	NONE
1	0	1	1	0	0	NONE	NONE	NONE	NONE
1	0	1	1	0	1	NONE	NONE	NONE	NONE
1	0	1	1	1	0	NONE	NONE	NONE	NONE
1	0	1	1	1	1	NONE	NONE	NONE	NONE
1	1	0	0	0	0	0 to 511	00000000h - 01FFFFFFh	ALL	ALL
1	1	0	0	0	1	1 to 511	00010000h - 01FFFFFFh	32,704KB	Upper 511/512
1	1	0	0	1	0	2 to 511	00020000h - 01FFFFFFh	32,640KB	Upper 255/256
1	1	0	0	1	1	4 to 511	00040000h - 01FFFFFFh	32,512KB	Upper 127/128
1	1	0	1	0	0	8 to 511	00080000h - 01FFFFFFh	32,256KB	Upper 63/64
1	1	0	1	0	1	16 to 511	00100000h - 01FFFFFFh	31MB	Upper 31/32
1	1	0	1	1	0	32 to 511	00200000h - 01FFFFFFh	30MB	Upper 15/16
1	1	0	1	1	1	64 to 511	00400000h - 01FFFFFFh	28MB	Upper 7/8
1	1	1	0	0	0	128 to 511	00800000h - 01FFFFFFh	24MB	Upper 3/4
1	1	1	0	0	1	256 to 511	01000000h - 01FFFFFFh	16MB	Upper 1/2
1	1	1	0	1	0	NONE	NONE	NONE	NONE
1	1	1	0	1	1	NONE	NONE	NONE	NONE
1	1	1	1	0	0	NONE	NONE	NONE	NONE
1	1	1	1	0	1	NONE	NONE	NONE	NONE
1	1	1	1	1	0	NONE	NONE	NONE	NONE
1	1	1	1	1	1	NONE	NONE	NONE	NONE

Note:
1. X = don't care;
2. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

INSTRUCTIONS

SPI instructions are list in table **Instruction Set (Standard/Dual/Quad SPI Instruction)** and **Instruction Set (Standard/Dual/Quad SPI Instruction, 3-byte Address Mode)**, **Instruction Set (Standard/Dual/Quad SPI instruction, 4-byte Address Mode)**. These instructions are initiated with the falling edge of Chip Select (CS#). The first Byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock, with the most significant bit (MSB) preceding it.

QPI instruction set is in table **Instruction Set (QPI Instructions, 3-Byte Address Mode), Instruction Set (QPI Instructions, 4-byte Address Mode)**. Instructions are initiated with the falling edge of Chip Select (CS#). The first Byte of data clocked through IO [3:0] provides the instruction code. Data on all four IO pins are sampled on the rising edge of clock, with MSB first. All QPI instructions, addresses, data and dummy Bytes are using all four IO pins to transfer one byte data at two serial clocks (CLK).

The instructions vary in length from one to several Bytes and may be followed by address Bytes, data Bytes, dummy Bytes (do not care). Instructions are completed with the rising edge of edge CS#. Clock relative timing diagrams for each instruction are included in the datasheet.

All read instructions can be finished after any clocked bit. However, all Write, Program or Erase instructions must be completed on a Byte boundary (CS# is driven high after a full 8-bits clocked) or the instruction will be ignored. Additionally, when a memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register and Erase/Program Suspend instructions will be ignored until the embedded operation has completed.

Instruction Set (Standard/Dual/Quad SPI Instructions)[1]

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number	**(0-7)**	**(8-15)**	**(16-23)**	**(24-31)**	**(32-39)**	**(40-47)**	**(48-55)**
Write Enable	**06h**						
Volatile SR Write Enable	**50h**						
Write Disable	**04h**						
Read Status Register-1	**05h**	(SR7-SR0)[2]					
Write Status Register-1[4]	**01h**	(SR7-SR0)[4]	(SR2.7-SR2.0)				
Read Status Register-2	**35h**	(SR2.7-SR2.0)[2]					
Write Status Register-2	**31h**	(SR2.7-SR2.0)					
Read Status Register-3	**15h**	(SR3.7-SR3.0)[2]					
Write Status Register-3	**11h**	(SR3.7-SR3.0)					
Read Extended Addr. Reg.	**C8h**	(EA7-EA0) (2)					
Write Extended Addr. Reg.	**C5h**	(EA7-EA0)					
Chip Erase	**C7h/60h**						
Erase / Program Suspend	**75h**						
Erase / Program Resume	**7Ah**						
Power-down	**B9h**						
Release Power-down / ID	**ABh**	Dummy	Dummy	Dummy	(ID7-ID0) [2]		
Manufacturer/Device ID	**90h**	Dummy	Dummy	00h	(MF7-MF0)	(ID7-ID0)	
JEDEC ID	**9Fh**	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)			
Enter QPI Mode	**38h**						
Reset Enable	**66h**						
Reset	**99h**						
Enter 4-Byte Address Mode	**B7h**						
Exit 4-Byte Address Mode	**E9h**						

Instruction Set (Standard/Dual/Quad SPI Instructions, 3-Byte Address Mode)[1]

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number	**(0-7)**	**(8-15)**	**(16-23)**	**(24-31)**	**(32-39)**	**(40-47)**	**(48-55)**
Read Unique ID	**4Bh**	Dummy	Dummy	Dummy	Dummy	(UID7-UID0)	…
Page Program	**02h**	A23-A16	A15-A8	A7-A0	(D7-D0)[3]	…	
Page Program with 4-Byte Address	**12h**	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)[3]	…
Quad Input Page Program	**32h**	A23-A16	A15-A8	A7-A0	(D7-D0)[3][9]	…	
Sector Erase (4KB)	**20h**	A23-A16	A15-A8	A7-A0			
Sector Erase (4KB) with 4-Byte Address	**21h**	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	**52h**	A23-A16	A15-A8	A7-A0			
Block Erase (32KB) with 4-Byte Address	**5Ch**	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	**D8h**	A23-A16	A15-A8	A7-A0			
Block Erase (64KB) with 4-Byte Address	**DCh**	A31-A24	A23-A16	A15-A8	A7-A0		
Read SFDP Register	**5Ah**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	…
Erase Security Register[5]	**44h**	A23-A16	A15-A8	A7-A0			
Program Security Register[5]	**42h**	A23-A16	A15-A8	A7-A0	(D7-D0)[3]	…	
Read Security Register[5]	**48h**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	…
Read Data	**03h**	A23-A16	A15-A8	A7-A0	(D7-D0)	…	
Read Data with 4-Byte Address	**13h**	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read	**0Bh**	A23-A16	A15-A8	A7-A0	Dummy*	(D7-D0)	…
Fast Read with 4-Byte Address	**0Ch**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)…

Instruction Set (Standard/Dual/Quad SPI Instructions, 3-Byte Address Mode)[1] continued

Clock Number	(0–7)	(8–15)	(16–23)	(24–31)	(32–39)	(40–43)	
Fast Read Dual Output	**3Bh**	A23-A16	A15-A8	A7-A0	Dummy*	(D7-D0)[7]	…
Clock Number	**(0–7)**	**(8–15)**	**(16–23)**	**(24–31)**	**(32–39)**	**(40–47)**	**(48–51)**
Fast Read Dual output with 4-Byte Address	**3Ch**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)
Clock Number	**(0–7)**	**(8–15)**	**(16–23)**	**(24–31)**	**(32–39)**	**(40–41)**	
Fast Read Quad Output	**6Bh**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0) [9]	…
Clock Number	**(0–7)**	**(8–15)**	**(16–23)**	**(24–31)**	**(32–39)**	**(40–47)**	**(48–49)**
Fast Read Quad Output with 4-Byte Address	**6Ch**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)[9]…

Data Input Output	Byte 1	Byte 2[6]	Byte 3[6]	Byte 4[6]	Byte 5	Byte 6[7]	Byte 7[7]
Clock Number	**(0–7)**	**(8–11)**	**(12–15)**	**(16–19)**	**(20–23)**	**(24–27)**	**(28–31)**
Fast Read Dual I/O	**BBh**	A23-A16	A15-A8	A7-A0	Dummy*	(D7-D0)	…
Clock Number	**(0–7)**	**(8–11)**	**(12–15)**	**(16–19)**	**(20–23)**	**(24–27)**	**(28–31)**
Fast Read Dual I/O with 4-Byte Address	**BCh**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)
Mftr./Device ID Dual I/O	**92h**	A23-A16	A15-A8	A7-A0	Dummy	(MF7-MF0)	(ID7-ID0)

Data Input Output	Byte 1	Byte 2[8]	Byte3[8]	Byte4[8]	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Clock Number	**(0-7)**	**(8, 9)**	**(10, 11)**	**(12, 13)**	**(14, 15)**	**(16, 17)**	**(18,19)**	**(20, 21)**	**(22, 23)**
Set Burst with Wrap	**77h**	Dummy	Dummy	Dummy	W7-W0				
Fast Read Quad I/O	**EBh**	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	Dummy	(D7-D0)	…
Fast Read Quad I/O with 4-Byte Address	**ECh**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	Dummy	(D7-D0)
Word Read Quad I/O[9]	**E7h**	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)	(D7-D0)	…
Mftr./Device ID Quad I/O	**94h**	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	Dummy	(MF7-MF0)	(ID7-ID0)

Instruction Set (QPI Instructions, 3-Byte Address Mode)[10]

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number	**(0, 1)**	**(2, 3)**	**(4, 5)**	**(6, 7)**	**(8, 9)**	**(10, 11)**	**(12, 13)**
Write Enable	**06h**						
Volatile SR Write Enable	**50h**						
Write Disable	**04h**						
Read Status Register-1	**05h**	(SR7-SR0)[2]					
Write Status Register-1[4]	**01h**	(SR7-SR0)[4]	(SR2.7-SR2.0)				
Read Status Register-2	**35h**	(SR2.7-SR2.0)[2]					
Write Status Register-2	**31h**	(SR2.7-SR2.0)					
Read Status Register-3	**15h**	(SR3.7-SR3.0)[2]					
Write Status Register-3	**11h**	(SR3.7-SR3.0)					
Read Extended Addr. Reg.	**C8h**	(EA7-EA0) (2)					
Write Extended Addr. Reg.	**C5h**	(EA7-EA0)					
Chip Erase	**C7h/60h**						
Erase / Program Suspend	**75h**						
Erase / Program Resume	**7Ah**						
Power-down	**B9h**						
Set Read Parameters	**C0h**	P7-P0					
Release Power-down / ID	**ABh**	Dummy	Dummy	Dummy	(ID7-ID0)[2]		
Manufacturer/Device ID	**90h**	Dummy	Dummy	00h	(MF7-MF0)	(ID7-ID0)	
JEDEC ID	**9Fh**	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)			
Exit QPI Mode	**FFh**						
Enter 4-Byte Address Mode	**B7h**						
Exit 4-Byte Address Mode	**E9h**						
Reset Enable	**66h**						
Reset	**99h**						
Page Program	**02h**	A23-A16	A15-A8	A7-A0	(D7-D0)[9]	…	
Page Program with 4-Byte Address	**12h**	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)[9]	…

Sector Erase (4KB)	**20h**	A23-A16	A15-A8	A7-A0			
Block Erase (32KB)	**52h**	A23-A16	A15-A8	A7-A0			
Block Erase (64KB)	**D8h**	A23-A16	A15-A8	A7-A0			
Sector Erase (4KB) with 4-Byte Address	**21h**	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (32KB) with 4-Byte Address	**5Ch**	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (64KB) with 4-Byte Address	**DCh**	A31-A24	A23-A16	A15-A8	A7-A0		
Fast Read	**0Bh**	A23-A16	A15-A8	A7-A0	Dummy[11]	(D7-D0)	…
Burst Read with Wrap[12]	**0Ch**	A23-A16	A15-A8	A7-A0	Dummy[11]	(D7-D0)	…
Fast Read Quad I/O	**EBh**	A23-A16	A15-A8	A7-A0	M7-M0[11]	Dummy	(D7-D0)
Fast Read Quad I/O with 4-Byte Address	**ECh**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0[11]	(D7-D0)
Erase Security Register[5]	**44h**	A23-A16	A15-A8	A7-A0			
Program Security Register[5]	**42h**	A23-A16	A15-A8	A7-A0	(D7-D0)(3)		
Read Security Register[5]	**48h**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	

Instruction Set (DTR with SPI Instructions, 3-Byte Address Mode)

Number of Clock(1-1-1) Clock number	**8 (0-7)**	**4 (8-11)**	**4 (12-15)**	**4 (16-19)**	**6 (20-25)**	**4 (26-29)**	**4**
DTR Fast Read	**0Dh**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	…
Number of Clock(1-2-2) Clock Number	**8 (0-7)**	**2 (8-9)**	**2 (10-11)**	**2 (12-13)**	**6 (14-19)**	**2 (20-21)**	**2**
DTR Fast Read Dual I/O	**BDh**	A23-A16	A15-A8	A7-A0	M7-M0&Dummy	(D7-D0)	...
Number of Clock(1-4-4) Clock Number	**8 (0-7)**	**1 (8)**	**1 (9)**	**1 (10)**	**8 (11-18)**	**1 (19)**	**1 (20)**
DTR Fast Read Quad I/O	**EDh**	A23-A16	A15-A8	A7-A0	M7-M0&Dummy	(D7-D0)	(D7-D0)
Number of Clock(1-4-4) Clock Number	**8 (0-7)**	**1 (8)**	**1 (9)**	**1 (10)**	**1 (11)**	**8 (12-19)**	**1 (20)**
DTR Fast Read Quad I/O with 4-Byte Address	**EEh**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0&Dummy	(D7-D0)

Instruction Set (DTR with QPI Instructions, 3-Byte Address Mode)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock(4-4-4) Clock Number	**2 (0-1)**	**1 (2)**	**1 (3)**	**1 (4)**	**8 (5-14)**	**1 (15)**	**1**
DTR Read with Wrap[12]	**0Eh**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	...
DTR Fast Read	**0Dh**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	...
DTR Fast Read Quad I/O	**EDh**	A23-A16	A15-A8	A7-A0	M7-M0&Dummy	(D7-D0)	-
Clock Number	**2 (0-1)**	**1 (2)**	**1 (3)**	**1 (4)**	**1 (5)**	**8 (6-15)**	**1 (16)**
DTR Fast Read Quad I/O with 4-Byte Address	**EEh**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)

Instruction Set (Standard/Dual/Quad SPI Instructions, 4-Byte Address Mode)[1]

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number	**(0–7)**	**(8–15)**	**(16–23)**	**(24–31)**	**(32–39)**	**(40–47)**	**(48-55)**
Read Unique ID	**4Bh**	Dummy	Dummy	Dummy	Dummy	Dummy	(UID7-UID0)…
Page Program	**02h**	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)[3]	
Page Program with 4-Byte Address	**12h**	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)[3]	
Quad Input Page Program	**32h**	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)[3][9]	
Sector Erase (4KB)	**20h**	A31-A24	A23-A16	A15-A8	A7-A0		
Sector Erase (4KB) with 4-Byte Address	**21h**	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	**52h**	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (32KB) with 4-Byte Address	**5Ch**	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	**D8h**	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (64KB) with 4-Byte Address	**DCh**	A31-A24	A23-A16	A15-A8	A7-A0		
Read Data	**03h**	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	…
Read Data with 4-Byte Address	**13h**	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	…
Fast Read	**0Bh**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)
Fast Read with 4-Byte Address	**0Ch**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy*	(D7-D0)
Read SFDP Register	**5Ah**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	…
Erase Security Register[5]	**44h**	A31-A24	A23-A16	A15-A8	A7-A0		
Program Security Register[5]	**42h**	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)[3]	…
Read Security Register[5]	**48h**	A31-S24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)
Clock Number	**(0–7)**	**(8–15)**	**(16–23)**	**(24–31)**	**(32–39)**	**(40–47)**	**(48-51)**
Fast Read Dual Output	**3Bh**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)[7]
Fast Read Dual Output with 4-Byte Address	**3Ch**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)[7]

Clock Number	(0–7)	(8–15)	(16–23)	(24–31)	(32–39)	(40–47)	(48-49)
Fast Read Quad Output	**6Bh**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)[9]
Fast Read Quad Output with 4-byte Address	**6Ch**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)[9]

Data Input Output	Byte 1	Byte 2[6]	Byte 3[6]	Byte 4[6]	Byte 5	Byte 6[7]	Byte 7[7]
Clock Number	**(0–7)**	**(8–11)**	**(12–15)**	**(16–19)**	**(20–23)**	**(24–27)**	**(28–31)**
Fast Read Dual I/O	**BBh**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)
Fast Read Dual I/O with 4-Byte Address	**BCh**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)
Mftr./Device ID Dual I/O	**92h**	A23-A16	A15-A8	A7-A0	Dummy	(MF7-MF0)	(ID7-ID0)

Data Input Output	Byte 1	Byte 2[8]	Byte3[8]	Byte4[8]	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Clock Number	**(0–7)**	**(8, 9)**	**(10, 11)**	**(12, 13)**	**(14, 15)**	**(16, 17)**	**(18,19)**	**(20, 21)**	**(22, 23)**
Set Burst with Wrap	**77h**	Dummy	Dummy	Dummy	W7-W0				
Fast Read Quad I/O	**EBh**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	Dummy	(D7-D0)
Fast Read Quad I/O with 4-Byte Address	**ECh**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	Dummy	(D7-D0)
Word Read Quad I/O[9]	**E7h**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)	(D7-D0)
Mftr./Device ID Quad I/O	**94h**	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	Dummy	(MF7-MF0)	(ID7-ID0)

Instruction Set (QPI Instructions, 4-Byte Address Mode)[13]

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number	**(0, 1)**	**(2, 3)**	**(4, 5)**	**(6, 7)**	**(8, 9)**	**(10, 11)**	**(12, 13)**
Write Enable	**06h**						
Volatile SR Write Enable	**50h**						
Write Disable	**04h**						
Read Status Register-1	**05h**	(SR7-SR0)[2]					
Write Status Register-1[4]	**01h**	(SR7-SR0)[4]	(SR2.7-SR2.0)				
Read Status Register-2	**35h**	(SR2.7-SR2.0)[2]					
Write Status Register-2	**31h**	(SR2.7-SR2.0)					
Read Status Register-3	**15h**	(SR3.7-SR3.0)[2]					
Write Status Register-3	**11h**	(SR3.7-SR3.0)					
Read Extended Addr. Reg.	**C8h**	(EA7-EA0) (2)					
Write Extended Addr. Reg.	**C5h**	(EA7-EA0)					
Chip Erase	**C7h/60h**						
Erase / Program Suspend	**75h**						
Erase / Program Resume	**7Ah**						
Power-down	**B9h**						
Set Read Parameters	**C0h**	P7-P0					
Release Power-down /ID	**ABh**	Dummy	Dummy	Dummy	(ID7-ID0)[2]		
Manufacturer/Device ID	**90h**	Dummy	Dummy	00h	(MF7-MF0)	(ID7-ID0)	
JEDEC ID	**9Fh**	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)			
Exit QPI Mode	**FFh**						
Enter 4-Byte Address Mode	**B7h**						
Exit 4-Byte Address Mode	**E9h**						
Enable Reset	**66h**						
Reset Device	**99h**						

Instruction Set (QPI Instructions, 4-Byte Address Mode)[13] continued

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5		Byte 6	Byte 7
Clock Number	**(0, 1)**	**(2, 3)**	**(4, 5)**	**(6, 7)**	**(8, 9)**		**(10, 11)**	**(12, 13)**
Page Program	**02h**	A31-A24	A23-A16	A15-A8	A7-A0		(D7-D0)[3]	
Page Program with 4-Byte Address	**12h**	A31-A24	A23-A16	A15-A8	A7-A0		(D7-D0)[3]	
Sector Erase (4KB)	**20h**	A31-A24	A23-A16	A15-A8	A7-A0			
Half Block Erase (32KB)	**52h**	A31-A24	A23-A16	A15-A8	A7-A0			
Block Erase (64KB)	**D8h**	A31-A24	A23-A16	A15-A8	A7-A0			
Sector Erase (4KB) with 4-Byte Address	**21h**	A31-A24	A23-A16	A15-A8	A7-A0			
Half Block Erase (32KB) with 4-Byte Address	**5Ch**	A31-A24	A23-A16	A15-A8	A7-A0			
Block Erase (64KB) with 4-Byte Address	**DCh**	A31-A24	A23-A16	A15-A8	A7-A0			
Fast Read	**0Bh**	A31-A24	A23-A16	A15-A8	A7-A0		Dummy[11]	(D7-D0)
Burst Read with Wrap	**0Ch**	A31-A24	A23-A16	A15-A8	A7-A0		Dummy[11]	(D7-D0)
Erase Security Register[5]	**44h**	A31-A24	A23-A16	A15-A8	A7-A0			
Program Security Register[5]	**42h**	A31-A24	A23-A16	A15-A8	A7-A0		(D7-D0)[3]	
Read Security Register[5]	**48h**	A31-A24	A23-A16	A15-A8	A7-A0		Dummy	(D7-D0)
Number of Clock(4-4-4) Clock number	**2 (0, 1)**	**2 (2, 3)**	**2 (4, 5)**	**2 (6, 7)**	**2 (8, 9)**	**2 (10, 11)**	**2 (12, 13)**	**2 (14, 15)**
Fast Read Quad I/O	**EBh**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)
Fast Read Quad I/O with 4-Byte Address	**ECh**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)

Instruction Set (DTR with SPI Instructions, 4-Byte Address Mode)

Number of Clock(1-1-1) **Clock number**	**8** **(0-7)**	**4** **(8-11)**	**4** **(12-15)**	**4** **(16-19)**	**4** **(20-23)**	**6** **(24-29)**	**4** **(30-33)**	**4**
DTR Fast Read	**0Dh**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	…
Number of Clock(1-2-2) **Clock Number**	**8** **(0-7)**	**2** **(8-9)**	**2** **(10-11)**	**2** **(12-13)**	**2** **(14-15)**	**6** **(16-21)**	**2** **(22-23)**	**2**
DTR Fast Read Dual I/O	**BDh**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0&Dummy	(D7-D0)	...
Number of Clock(1-4-4) **Clock Number**	**8** **(0-7)**	**1** **(8)**	**1** **(9)**	**1** **(10)**	**1** **(11)**	**8** **(12-19)**	**1** **(20)**	**1**
DTR Fast Read Quad I/O	**EDh**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0&Dummy	(D7-D0)	(D7-D0)
DTR Fast Read Quad I/O with 4-Byte Address	**EEh**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0&Dummy	(D7-D0)	…

Instruction Set (DTR with QPI Instructions, 4-Byte Address Mode)

Number of Clock(4-4-4) **Clock Number**	**2** **(0-1)**	**1** **(2)**	**1** **(3)**	**1** **(4)**	**1** **(5)**	**8** **(6-15)**	**1** **(16)**	**1**
DTR Read with Wrap[12]	**0Eh**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	…
DTR Fast Read	**0Dh**	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	…
DTR Fast Read Quad I/O	**EDh**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0&Dummy	(D7-D0)	-
DTR Fast Read Quad I/O with 4-Byte Address	**EEh**	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0&Dummy	(D7-D0)	…

Note:
1. Most Significant Bit is sent first when shift data Bytes. Data in “( )” indicate data output from the device on either 1, 2 or 4 IO pins.
2. The Status Register contents and Device ID will repeat continuously until CS# pull high.
3. (1-256) Byte of data input is required for Page Program, Quad Page Program and Program Security Registers. If more than 256 Bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.
4. Write Status Register-1 (01h) can be used to write both Status Register-1&2.

5. Security Register Address:
   Security Register1: A23-A16=00H, A15-A12=1H, A11-A10 = 00b, A9-A0= Byte Address;
   Security Register2: A23-A16=00H, A15-A12=2H, A11-A10 = 00b, A9-A0= Byte Address;
   Security Register3: A23-A16=00H, A15-A12=3H, A11-A10 = 00b, A9-A0= Byte Address.

6. Dual SPI address input format:
   DQ_0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0

DQ_1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3, M1

7. Dual SPI data output format:
   DQ_0 = (D6, D4, D2, D0)
   DQ_1 = (D7, D5, D3, D1)

8. Quad SPI address and Set Burst with Wrap Input format:

Quad SPI address input format:	Set Burst with Wrap input format:
DQ_0 = A20, A16, A12, A8, A4, A0, M4, M0	DQ_0 = x, x, x, x, x, x, W4, x
DQ_1 = A21, A17, A13, A9, A5, A1, M5, M1	DQ_1 = x, x, x, x, x, x, W5, x
DQ_2 = A22, A18, A14, A10, A6, A2, M6, M2	DQ_2 = x, x, x, x, x, x, W6, x
DQ_3 = A23, A19, A15, A11, A7, A3, M7, M3	DQ_3 = x, x, x, x, x, x, x, x

9. Quad SPI data input/output, Fast Read Quad I/O data output and Word Read Quad I/O data output format:

Quad SPI data input/output format:	Fast Read Quad I/O data output format:	Word Read Quad I/O data output format:
DQ_0 = (D4, D0, ……) DQ_1 = (D5, D1, ……) DQ_2 = (D6, D2, ……) DQ_3 = (D7, D3, ……)	DQ_0 = (x, x, x, x, D4, D0, D4, D0) DQ_1 = (x, x, x, x, D5, D1, D5, D1) DQ_2 = (x, x, x, x, D6, D2, D6, D2) DQ_3 = (x, x, x, x, D7, D3, D7, D3)	DQ_0 = (x, x, D4, D0, D4, D0, D4, D0) DQ_1 = (x, x, D5, D1, D5, D1, D5, D1) DQ_2 = (x, x, D6, D2, D6, D2, D6, D2) DQ_3 = (x, x, D7, D3, D7, D3, D7, D3)

10. QPI Command with 3-Byte Address, Address, Data input/output format:

	Command		Address						Data input/output				
CLK	0	1	2	3	4	5	6	7	8	9	10	11	……
DQ_0	C4	C0	A20	A16	A12	A8	A4	A0	D4,	D0	D4	D0	……
DQ_1	C5	C1	A21	A17	A13	A9	A5	A1	D5,	D1	D5	D1	……
DQ_2	C6	C2	A22	A18	A14	A10	A6	A2	D6	D2	D6	D2	……
DQ_3	C7	C3	A23	A19	A15	A11	A7	A3	D7	D3	D7	D3	……

11. The number of dummy clocks for QPI Fast Read (0Bh), QPI Fast Read Quad I/O (EBh) & QPI Burst Read with Wrap (0Ch) is controlled by read parameter P7 - P4.
12. The wrap around length for QPI Burst Read with Wrap is controlled by read parameter P3 - P0.
13. QPI Command with 4-Byte Address, Address, Data input/output format:

	Command		Address								Data input/output				
CLK	0	1	2	3	4	5	6	7	8	9	10	11	12	13	……
DQ_0	C4	C0	A28	A24	A20	A16	A12	A8	A4	A0	D4,	D0	D4	D0	……
DQ_1	C5	C1	A29	A25	A21	A17	A13	A9	A5	A1	D5,	D1	D5	D1	……
DQ_2	C6	C2	A30	A26	A22	A18	A14	A10	A6	A2	D6	D2	D6	D2	……
DQ_3	C7	C3	A31	A27	A23	A19	A15	A11	A7	A3	D7	D3	D7	D3	……

Read Dummy setting reference

	DC1/ DC0	Dmy Clk	0B/0C	3B/3C	6B/6C	Dmy Clk	BB/BC	E7	Dmy Clk	EB/EC	Dmy Clk	0D	BD	Dmy Clk	ED/EE
			Speed				Speed			Speed		Speed			Speed
SPI	00	8	166[1]	166[1]	166[1]	4	108[1]	108[1]	6	166[1]	6	90[1]	90[1]	8	90[1]
	01	8	166	166	166	8	166	166	4	108	4	66	66	4	66
	10	8	166	166	166	4	108	108	8	166	8	90	90	6	66
	11	8	166	166	166	8	166	166	10	166	10	108	108	10	108
	C0h P[5:4]	Dmy Clk	0B	EB/EC	0C	Dmy Clk	0D	ED/EE	0E						
			Speed				Speed								
QPI	00	4	80[1]	80[1]	80[1]	10	108[1]	108[1]	108[1]						
	01	6	108	108	108	4	66	66	66						
	10	8	133	133	133	6	80	80	80						
	11	10	166	166	166	8	108	108	108						

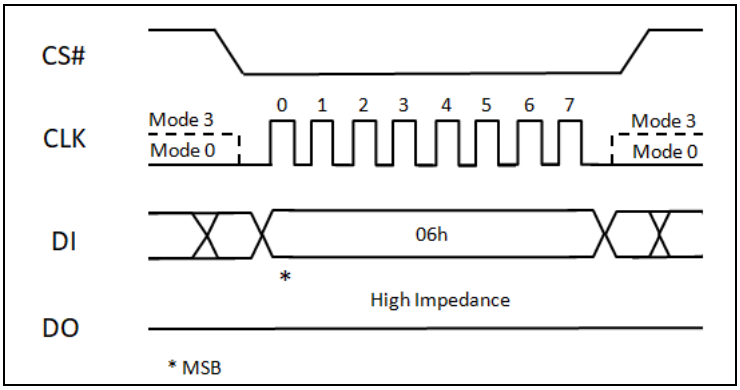
Note:
1. default

Manufacturer and Device Identification

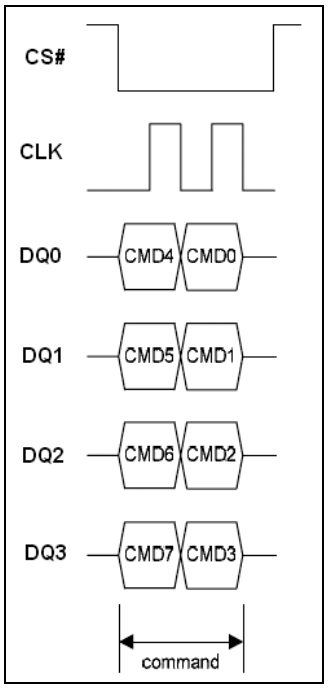
OP code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			18h
90h/92h/94h	1Ch		18h
9Fh	1Ch	4019h	

Write Enable (06h)

The Write Enable (WREN) instruction (Figure shown as below) sets the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Quad Input Page Program (QPP), Sector Erase (SE), Block Erase (HBE/BE), Chip Erase (CE) and Write Status Register (WRSR/ WRSR2/ WRSR3) instruction.
The Write Enable (WREN) instruction is entered by driving Chip Select (CS#) Low, sending the instruction code, and then driving Chip Select (CS#) High.
The instruction sequence is shown in figure Write Enable Instruction (QPI Mode) while using the Enter QPI mode (EQPI) (38h) command.



Write Enable Instruction (SPI mode)

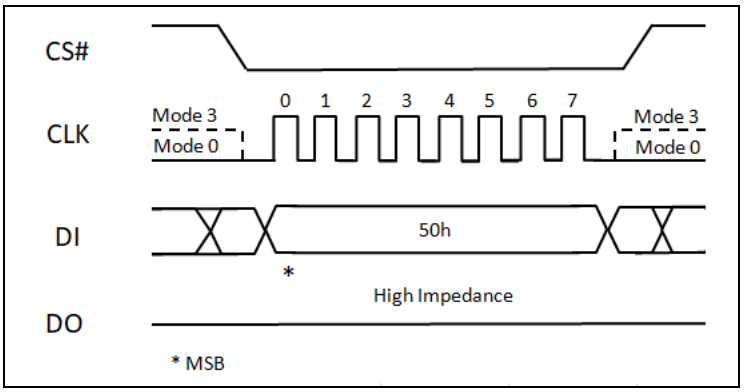


Write Enable Instruction (QPI Mode)

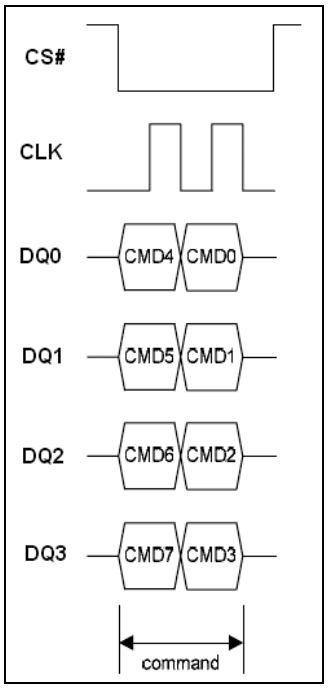
Write Enable for Volatile Status Register (50h)

This feature enables user to change memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Volatile Status Register Write Enable (50h) command won't set the Write Enable Latch (WEL) bit, it is only valid for WRSR, WRSR2 and WRSR3 commands to change the Volatile Status Register bit values.
To write to Volatile Status Register, issue the Volatile Status Register Write Enable (50h) command prior to issuing WRSR or WRSR2 or WRSR3. The Status Register bits will be refreshed to Volatile Status Register (S[7:2] or SR2[7:0]) or SR3[7:0]) within t_{SHSL2}. Upon power off or the execution of a Software/Hardware Reset, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored.
The instruction sequence is shown as below.

The instruction sequence is shown as below while using the Enter QPI mode (EQPI) (38h) command.



Write Enable for Volatile Status Register Instruction (SPI mode)

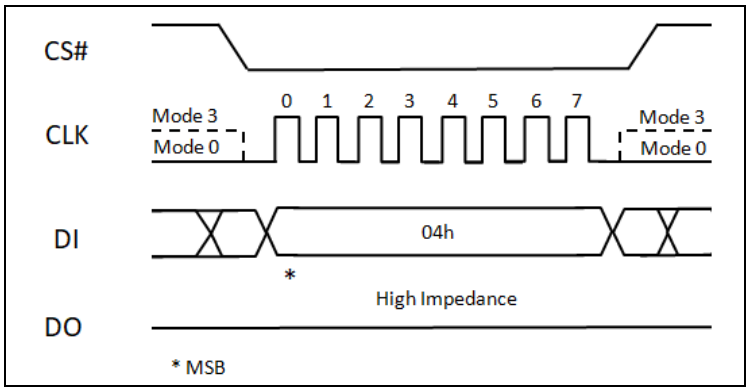


Write Enable for Volatile Status Register Instruction (QPI Mode)

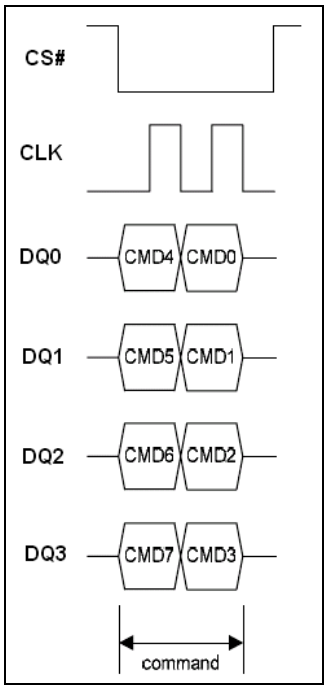
Write Disable (04h)

The Write Disable instruction resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving Chip Select (CS#) low, shifting the instruction code “04h” into the DI pin and then driving Chip Select (CS#) high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase (HBE/BE) and Chip Erase instructions.

The instruction sequence is shown as below while using the Enter QPI mode (EQPI) (38h) command.



Write Disable Instruction (SPI Mode)

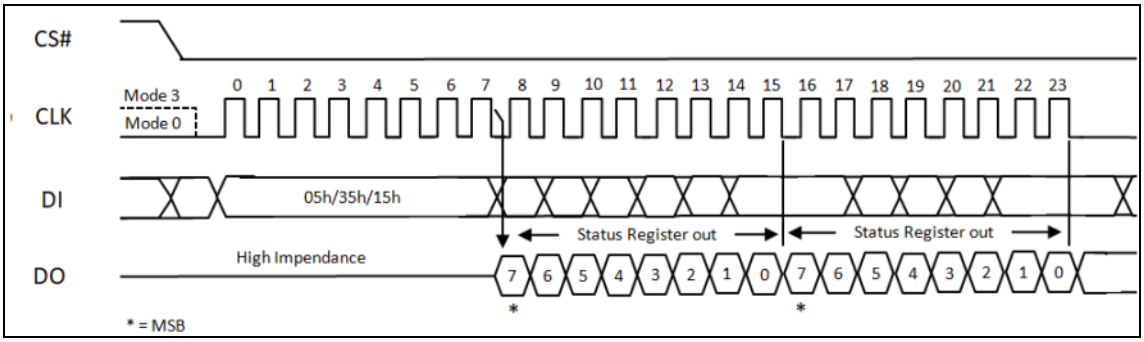


Write Disable Instruction (QPI Mode)

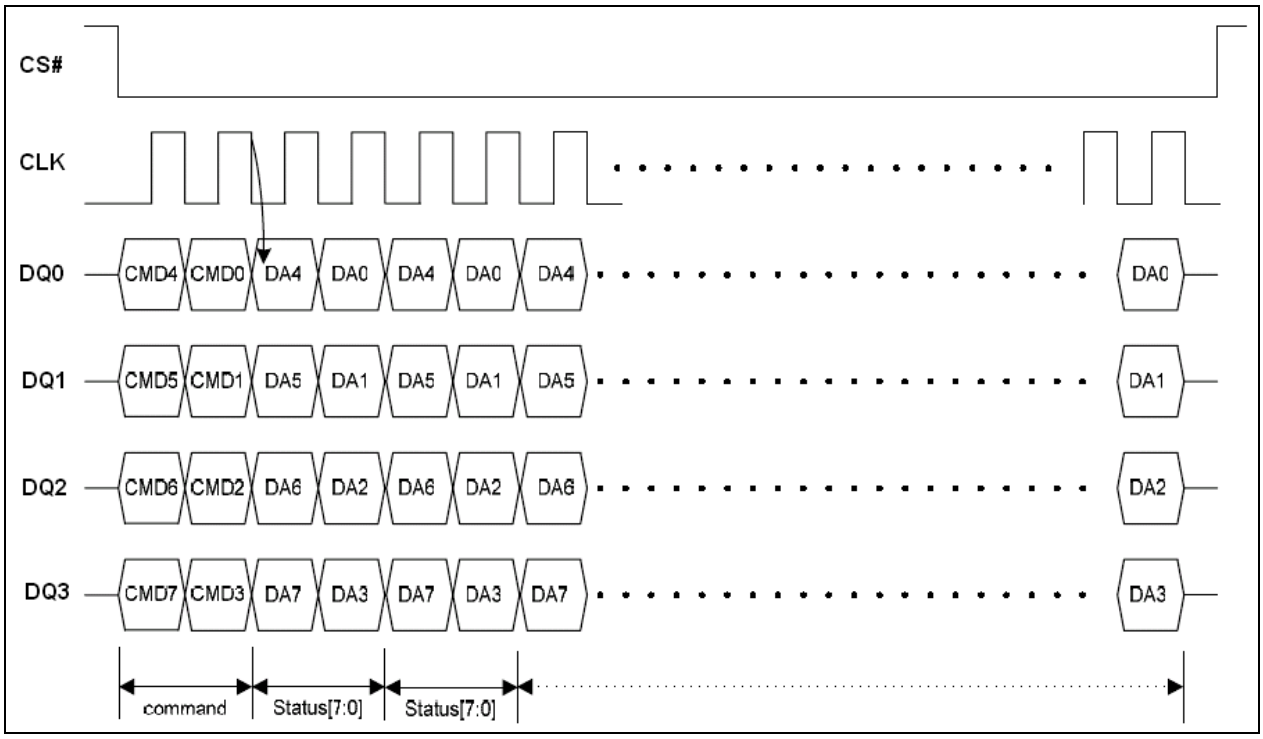
Read Status Register-1/2/3 (05h/35h/15h)

The Read Status Register-1/2/3 (RDSR, RDSR2, RDSR3) instruction allows the Status Register-1/2/3 to be read. The Status Register-1/2/3 may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously.

The instruction sequence is shown as below while using the Enter QPI mode (EQPI) (38h) command.



Read Status Register Instruction (SPI Mode)



Read Status Register Instruction (QPI Mode)

Status Register 1

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
SRP0 bit (Status Register Protect 0)	BP4 bit (Block Protected)	BP3 bit (Block Protected)	BP2 bit (Block Protected)	BP1 bit (Block Protected)	BP0 bit (Block Protected)	WEL bit (Write Enable Latch)	WIP bit (Write in Progress)
(note 2)	(note1)	(note1)	(note1)	(note1)	(note1)	1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
Volatile/ Non-Volatile bit	Volatile/ Non-Volatile bit	Volatile/ Non-Volatile bit	Volatile/ Non-Volatile bit	Volatile/ Non-Volatile bit	Volatile/ Non-Volatile bit	Read Only bit	Read Only bit

Note:
1. See the “Protected Area Size Sector Organization” table
2. See the “hardware protect” table

The status and control bits of the Status Register are as follows:

Erase/Write in Progress (WIP) – Read Only

The WIP bit will be reset to 0, while the device accepts further instructions and the instructions of program, erase or write status/security register instruction are finished.
When the device is performing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Register instruction, WIP=1. During this time, the device will ignore further instructions except the Read Status Register and Erase/Program Suspend instructions (as indicated by t_W, t_{PP}, t_{SE}, t_{BE}, and t_{CE} in AC Characteristics).

Write Enable Latch (WEL) – Read only

After the Write Enable Instruction (06h) is executed, the Write Enable Latch (WEL) =1 at SR1. The WEL status bit is cleared to 0 when the device is write disabled. At power-up or after the execution of any of the instructions (Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Register and Program Security Register), the WEL=0.

Block Protect Bits (BP4, BP3, BP2, BP1, BP0) – Volatile/Non-Volatile Writable

As indicated by t_W in AC characteristics, the Block Protect Bits (BP4, BP3, BP2, BP1 and BP0) are read/write bits in the status register (SR6, SR5, SR4, SR3, and SR2) that provide Write Protection control and status. Block Protect bits can be set with the Write Status Register Instruction. It is possible for all, none or part of a memory array to be protected from Program and Erase instructions (please refer Protected Area Sizes Sector Organization table). The factory default setting for the Block Protection Bits is 0, meaning that the device is non-protect.

Status Register Protect (SRP1, SRP0) – Volatile/Non-Volatile Writable

The Status Register Protect bits (SRP1 and SRP0) control three methods of write protection: software protection, hardware protection, power supply lock-down. And the SRP bits are read/write bits in the status register (SR2.0 and SR7).

Hardware Protect

SRP1	SRP0	WP#	Status Register	Description
0	0	X	Software Protect	WP# pin has no control. The Status Register can be written to after a Write Enable instruction, WEL=1. (default)
0	1	0	Hardware Protect	When WP# pin is low the Status Register locked and cannot be written to.
0	1	1	Hardware Unprotect	When WP# pin is high the Status register is unlocked and can be written to after a Write Enable instruction, WEL=1.
1	0	X	Power Supply Lock Down	Status Register is protected and cannot be written to again until the next power-down, power-up cycle.[1]

Note.
1. When SRP1, SRP0 = (1, 0), a power-down, power-up cycle will change SRP1, SRP0 to (0, 0) state

Status Register 2

SR2.7	SR2.6	SR2.5	SR2.4	SR2.3	SR2.2	SR2.1	SR2.0
SUS bit (suspend status bit)	CMP bit	SPL2 bit	SPL1 bit	SPL0 bit	Reserved bit	QE bit (Quad Enable bit)	SRP1 bit (Status Register Protect 1)
1 = suspend 0 = not suspend	(note 1)	1 = OTP3 sector is protected	1 = OTP2 sector is protected	1 = OTP1 sector is protected		1 = WP# and HOLD#/RESET# disable 0 = WP# and HOLD#/RESET# enable (Note 3)	(note 2)
Indicator bit	Volatile/ Non-Volatile bit	OTP bit	OTP bit	OTP bit		Volatile/ Non-Volatile bit	Volatile/ Non-Volatile bit

Note:
1. See the “Protected Area Size Sector Organization” table
2. See the “Hardware Protect” table
3. Factory default for Quad Enabled part numbers with differentiation code. (**Please refer to ORDERING INFORMATION**).

Erase/Program Suspend Status (SUS) – Indicator bit

After running Erase/Program Suspend (75h) instruction, the Suspend Status bit is a read-only bit in the status register (SR2.7) that is set to 1. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) instruction and after power-down and power-up cycles.

Complement Protect (CMP) – Volatile/Non-Volatile Writable

The Complement Protect bit (CMP) which functions work with the BP4, BP3, BP2, BP1 and BP0 bits to provide greater flexibility for array protection is a read/write bit in the status register (SR2.6). The default setting is CMP=0. Once CMP=1, the array protection previously set by BP4, BP3, BP2, BP1 and BP0 will be reversed. When CMP=0, the top 64KB block can be protected while the rest of the array is unprotected; when CMP=1, the top 64KB block will become unprotected while the rest of the array become read-only. (Refer to Protected Area Sizes Sector Organization table)

Security Register Lock Bits (SPL2, SPL1, SPL0) – OTP bit

The Security Register Lock Bits (SPL2, SPL1, SPL0) are non-volatile One Time Program (OTP) bits in the Status Register (SR2.5, SR2.4 and SR2.3) that provide the write protect control and status to the Security Registers. The default state of SPL2-0 = (0,0,0) for three Security Registers unlocked. SPL2-0 can be individually set to 1 using the Write Status Register instruction. SPL2-0 is One Time Programmable (OTP), and once it is set to 1, the corresponding 2048-Byte Security Register will become permanently read-only.

Quad Enable (QE) – Volatile/Non-Volatile Writable

The Quad Enable (QE) bit that allows Quad SPI and QPI operation is a read/write bit in the status register (SR2.1). When the QE bit is set to the state of 0, the WP# and HOLD# pin are enabled. When the QE bit is set to the state of 1, the Quad DQ_2 and DQ_3 pins are activated, and WP# and HOLD# pin functions are disabled. Factory default for Quad Enabled part numbers with differentiation code. (**Please refer to ORDERING INFORMATION**).
Before issuing an “Enter QPI (38h)” to switch the device from Standard/Dual/Quad SPI to QPI, the QE bit should be set to 1, otherwise the command will be ignored. When the device is in QPI mode, the QE bit will remain at 1. The “Write Status Register” command in QPI mode cannot change the QE bit from “1” to “0”.

Status Register 3

<table>
<tr><th>SR3.7</th><th>SR3.6</th><th>SR3.5</th><th>SR3.4</th><th>SR3.3</th><th>SR3.2</th><th>SR3.1</th><th>SR3.0</th></tr>
<tr><td>HRSW
(HOLD# / RESET# function bit)</td><td>DRV1
(Output Driver Strength bit)</td><td>DRV0
(Output Driver Strength bit)</td><td>DC1
(dummy cycle bit)</td><td>DC0
(dummy cycle bit)</td><td rowspan="3">Reserved bit</td><td>ADP
(Power Up Address Mode)</td><td>ADS
(Current Address Mode)</td></tr>
<tr><td>1 = RESET#
0 = HOLD#
(default 0)</td><td colspan="3">00 = 100%
01 = 75%
10 = 50%
11 = 25%
(default 01)</td><td>(Note 1)</td><td>1 = Power up into 4byte address mode
0 = Power up into 3byte address mode
(default 0)</td><td>1 = 4byte address mode
0 = 3byte address mode</td></tr>
<tr><td>Volatile/ Non-Volatile bit</td><td>Volatile/ Non-Volatile bit</td><td>Volatile/ Non-Volatile bit</td><td>Volatile/ Non-Volatile bit</td><td>Volatile/ Non-Volatile bit</td><td>Non-Volatile bit</td><td>Indicator bit</td></tr>
</table>

Note:
1. See description about “dummy cycle bit”

Output Driver Strength (DRV1, DRV0) – Volatile/Non-Volatile Writable

The DRV1 & DRV0 bits are applied to determine the output driver strength for Read operations.

HOLD# or RESET# Pin Function (HRSW) – Volatile/Non-Volatile Writable

Setting the HRSW bit can determine whether the HOLD# or RESET# function will be implemented on the hardware pin for 8-pin packages. When HRSW=0, that is factory default, the pin acts as HOLD#; when HRSW=1, the pin acts as RESET#; however, HOLD# or RESET# functions are only available when QE=0. If QE equals to 1, the HOLD# and RESET# functions are disabled, and the pin acts as a dedicated data I/O pin.

Dummy Cycle Bits

The Dummy Cycle Bits (DC1&DC0) are used to determine the Max Frequency for Read operations. Please refer to table **Read Dummy setting reference**

Current Address Mode (ADS) – Status Only

The Current Address Mode bit is a read only bit in the Status Register-3 that indicates which address mode the device is currently operating in. When ADS=0, the device is in the 3-Byte Address Mode, when ADS=1, the device is in the 4-Byte Address Mode.

Power-Up Address Mode (ADP) – Non-Volatile Writable

The ADP bit is a non-volatile bit that determines the initial address mode when the device is powered on or reset. This bit is only used during the power on or device reset initialization period, and it is only writable by the non-volatile Write Status sequence (06h + 11h). When ADP=0(factory default), the device will power up into 3-Byte Address Mode, the Extended Address Register must be used to access memory regions beyond 128Mb. When ADP=1, the device will power up into 4-Byte Address Mode directly.

Reserved Bits – Non Functional

There are several reserved Status Register bits that may be read out as “0” or “1” and it is recommended that the value of these bits be ignored. During the “Write Status Register” instruction, the Reserved Bits can be written as “0” without any implications.

Write Status Register-1/2/3 (01h/31h/11h)

The Write Status Register (WRSR-1/WRSR-2/WRSR-3) instructions allow new values to be written to the Status Register-1/2/3. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR1/WRSR2/WRSR3) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code and the data byte or data bytes on Serial Data Input (DI). The WRSR1 instruction also support two bytes data input to set status register-1 and status register-2.

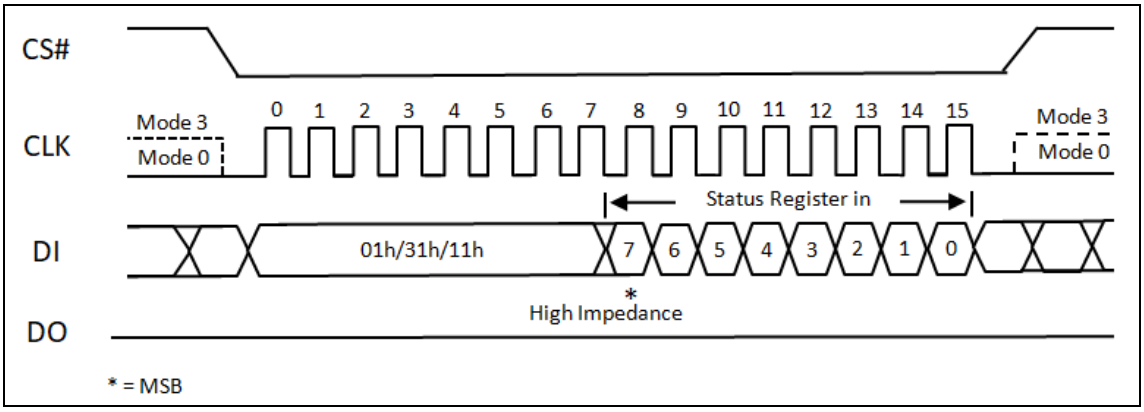
The Write Status Register (WRSR1) instruction has no effect on SR1 and SR0 of the Status Register. WRSR2 instruction has no effect on SR2.7 and SR2.2. WRSR3 instruction has no effect on SR3.2 and SR3.0. Chip Select (CS#) must be driven High after the 8th or 16th bit (16th bits only supported at WRSR1) of the data byte has been latched in. If not, the Write Status Register (WRSR1/2/3) instruction is not executed. As soon as Chip Select (CS#) is driven high, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register-1 (WRSR1) instruction allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, and Hardware protection bit (SRP0). The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Protect (SRP) bit in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode (HPM). The Write Status Register (WRSR) instruction is not executed once the Hardware Protected Mode (HPM) is entered.

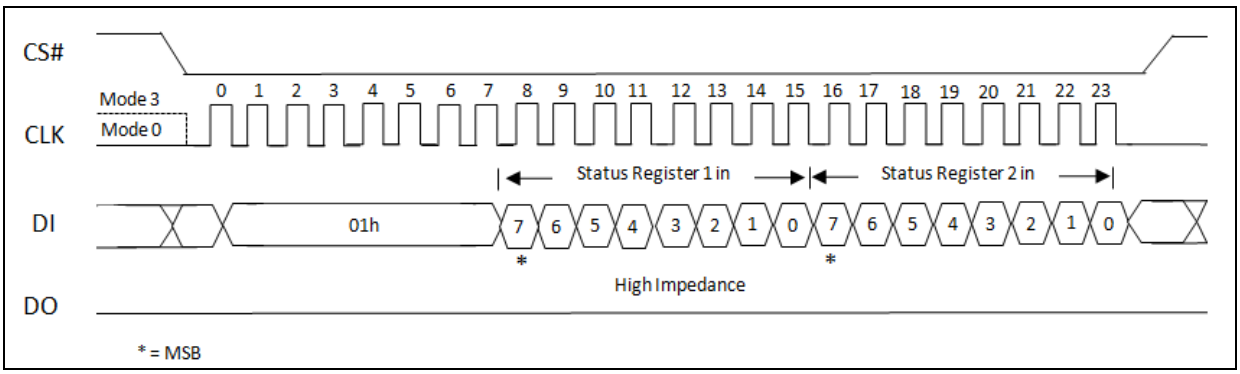
The Write Status Register-2 (WRSR2) allows set SRP1, quad enable/disable (QE), OTP security sector lock or unlock (SPL0/1/2) and CMP bit. The SRP1 can be set to use power up lock. Status Register is protected and cannot be written to again until the next power-down, power-up cycle. After power up, SRP1 and SRP0 will back to (0,0). OTP security sectors will be read only after SPL0/1/2 set to 1, and can't program or erase anymore (they are one time program bits).

QE bit cannot set to 0 while at EQPI mode. SPL2-0 cannot set from 1 to 0 because they are OTP bit.

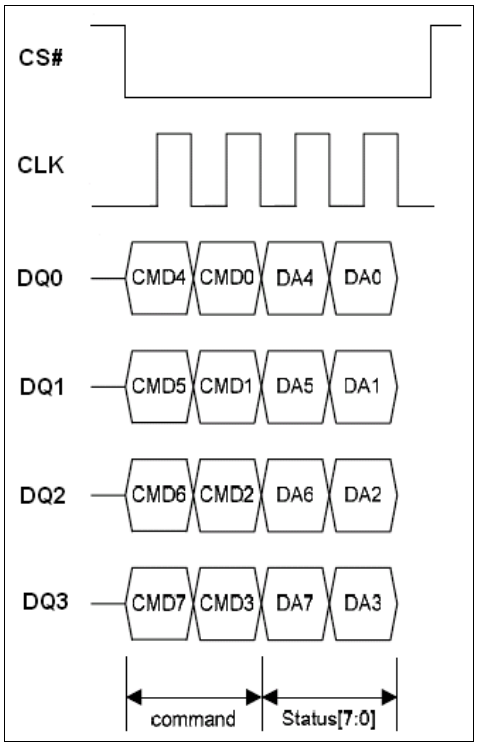
The instruction sequence is shown in as below while using the Enter QPI mode (EQPI) (38h) command.



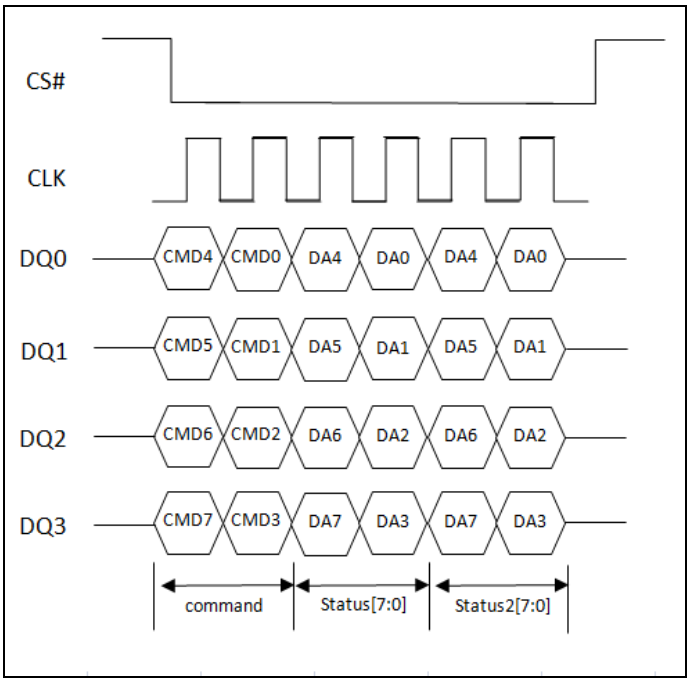
Write Status Register-1/2/3 instruction (SPI Mode)



Write Status Register-1 (Multi bytes) (SPI Mode)



Write Status Register-1/2/3 Instruction (QPI Mode)



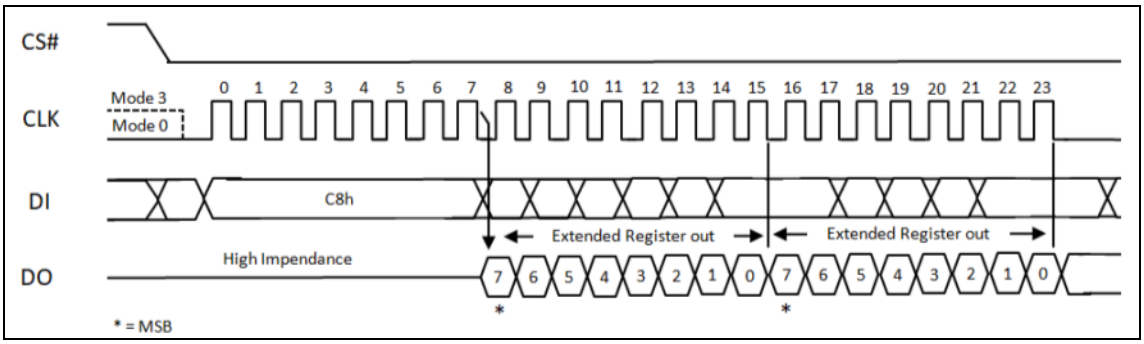
Write Status Register-1 (Multi bytes) (QPI Mode)

Read Extended Address Register (C8h)

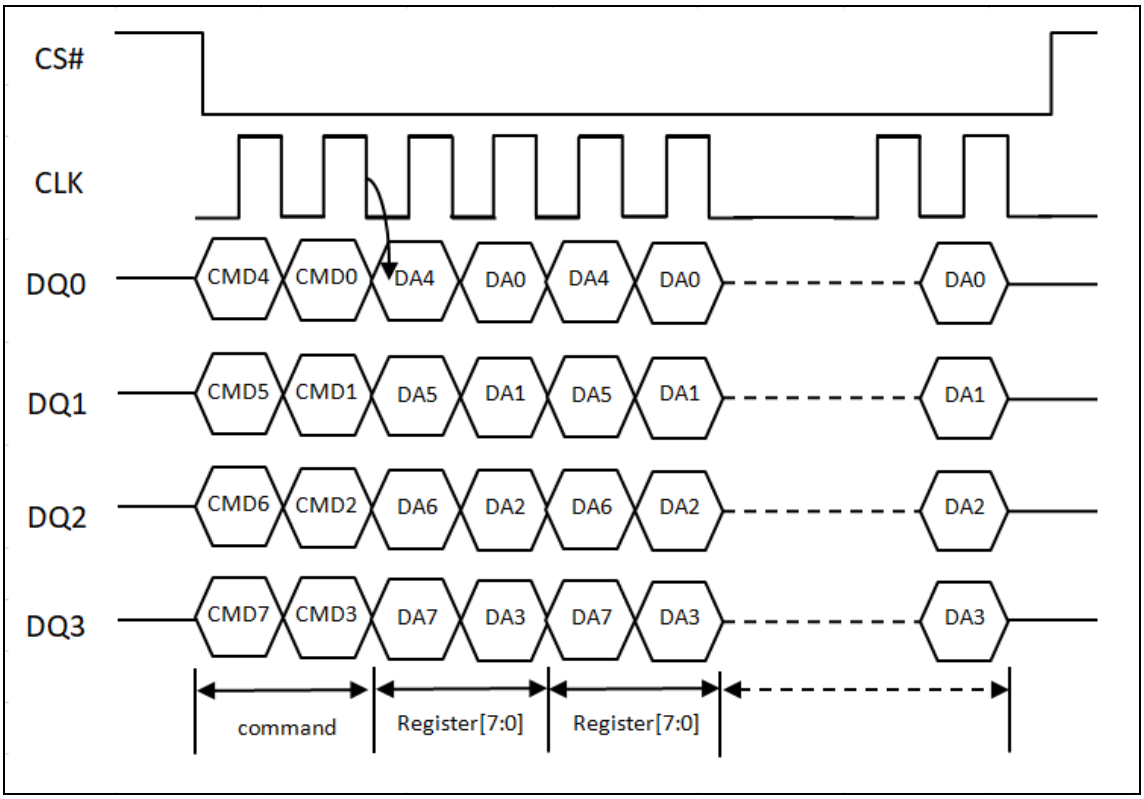
When the device is in the 3-Byte Address Mode, the Extended Address Register is used as the 4th address byte A[31:24] to access memory regions beyond 128Mb. The Read Extended Address Register instruction is entered by driving CS# low and shifting the instruction code “C8h” into the DI pin on the rising edge of CLK. The Extended Address Register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first.
When the device is in the 4-Byte Address Mode, the Extended Address Register is not used.

Extended Address Register

EA7	EA6	EA5	EA4	EA3	EA2	EA1	EA0
A31	A30	A29	A28	A27	A26	A25	A24
Volatile bit	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Volatile bit



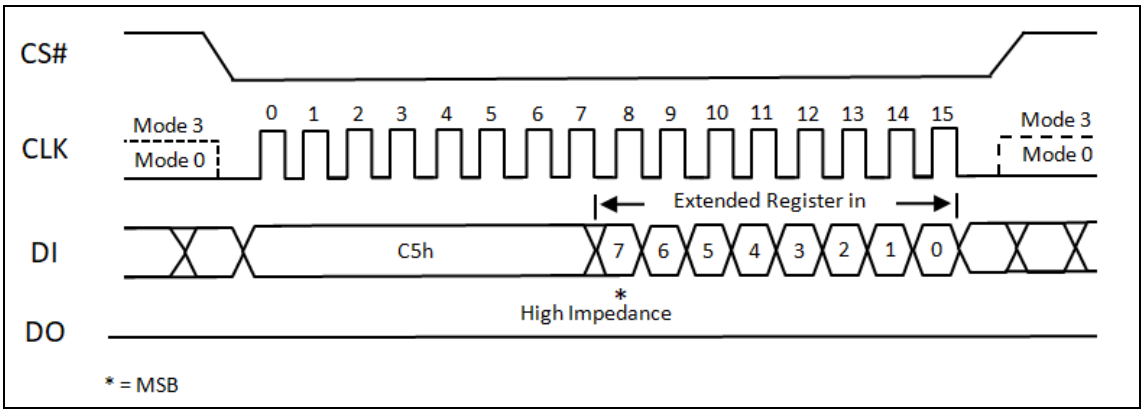
Read Extended Address Register Instruction (SPI Mode)



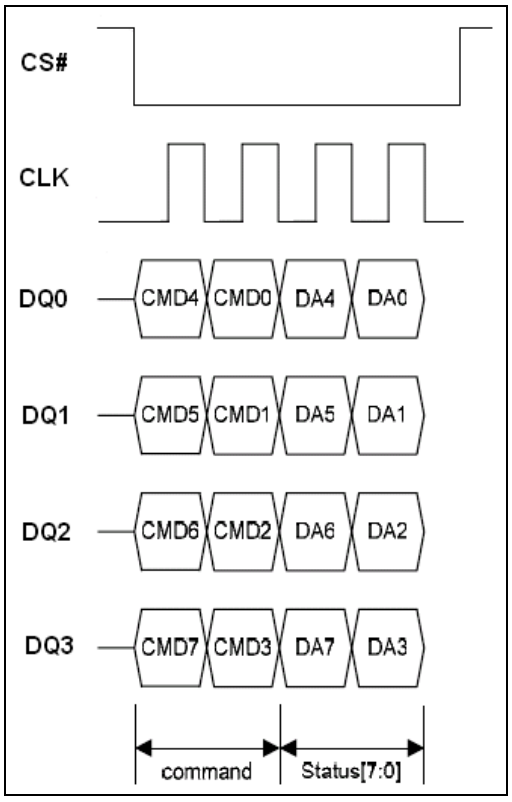
Read Extended Address Register Instruction (QPI Mode)

Write Extended Address Register (C5h)

The Extended Address Register is a volatile register that stores the 4th byte address (A31-A24) when the device is operating in the 3-Byte Address Mode (ADS=0). To write the Extended Address Register bits, a Write Enable (06h) instruction must previously have been executed for the device to accept the Write Extended Address Register instruction (WEL=1). Once write enabled, the instruction is entered by driving CS# low, sending the instruction code “C5h”, and then writing the Extended Address Register data byte.
Upon power up or the execution of a Software/Hardware Reset, the Extended Address Register bit values will be cleared to 0.
The Extended Address Register is only effective when the device is in the 3-Byte Address Mode. When the device operates in the 4-Byte Address Mode (ADS=1), any command with address input of A31-A24 will replace the Extended Address Register values. It is recommended to check and update the Extended Address Register if necessary when the device is switched from 4-Byte to 3-Byte Address Mode.



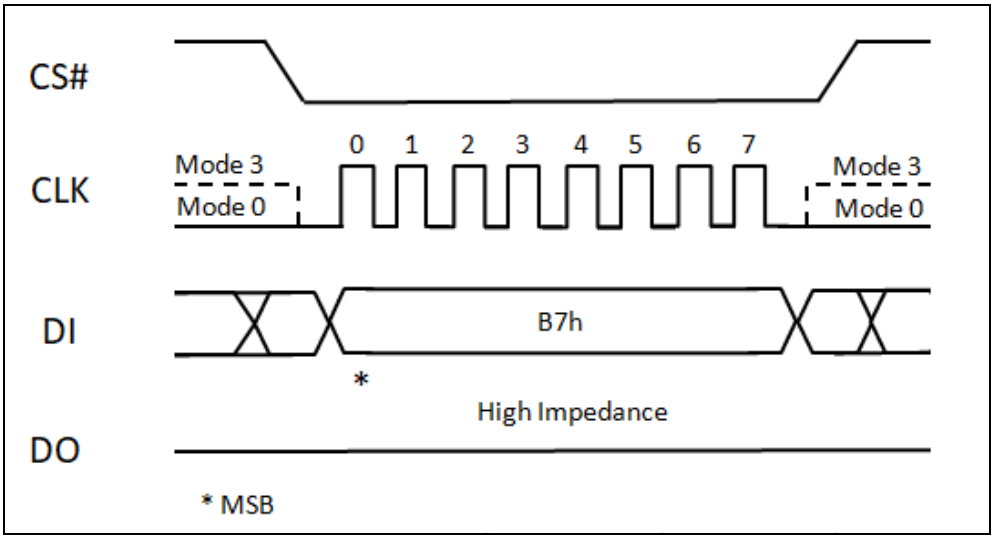
Write Extended Address Register Instruction (SPI Mode)



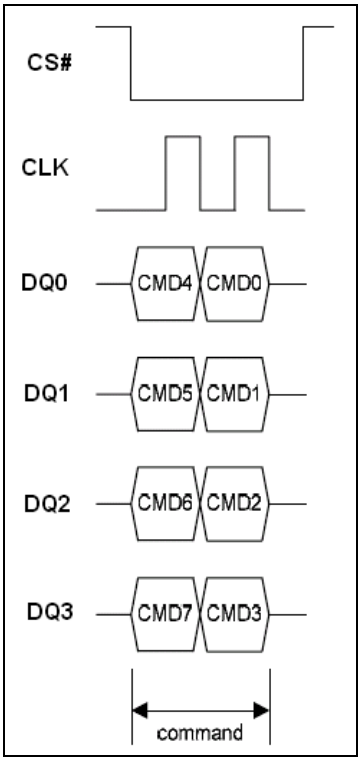
Write Extended Address Register Instruction (QPI Mode)

Enter 4-Byte Address Mode (B7h)

The enter 4byte address mode instruction enables accessing the address length of 32-bit for the memory area of higher density (larger than 128Mb). The device default is in 24-bit address mode; after sending out the enter 4byte address mode instruction, the 4byte bit (ADS) of Status Register 3 will be automatically set to "1" to indicate the 4-byte address mode has been enabled. Once the 4-byte address mode is enabled, the address length becomes 32-bit instead of the default 24-bit. There is a method to exit the 4-byte mode: writing exit 4-byte mode instruction. All instructions are accepted normally, and just the address bit is changed from 24-bit to 32-bit. The sequence of issuing enter 4byte address mode instruction is: CS# goes low → sending enter 4byte address mode instruction to enter 4-byte mode (automatically set 4byte bit as "1") → CS# goes high. (Enter 4byte address mode Instruction Sequence Diagram figure for SPI mode and EQPI mode)



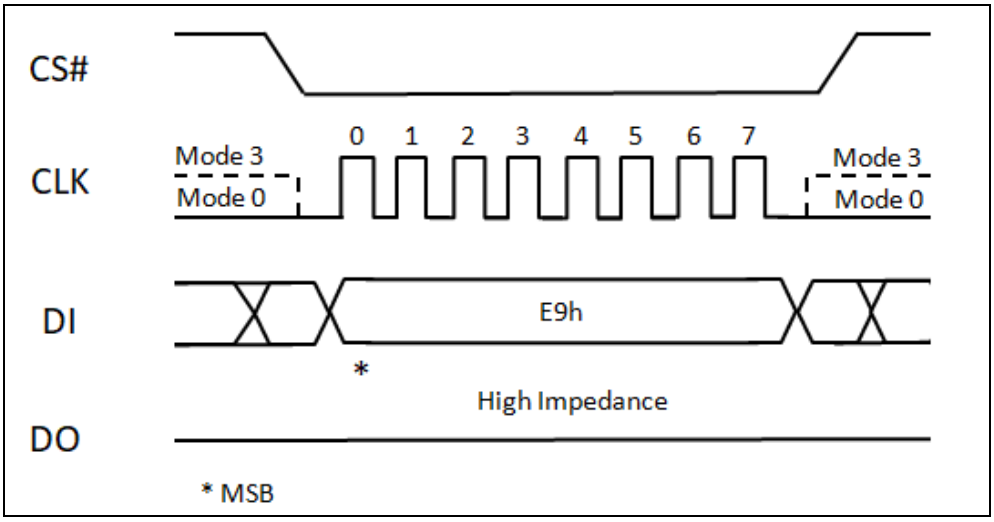
Enter 4-Byte Address Mode instruction (SPI Mode)



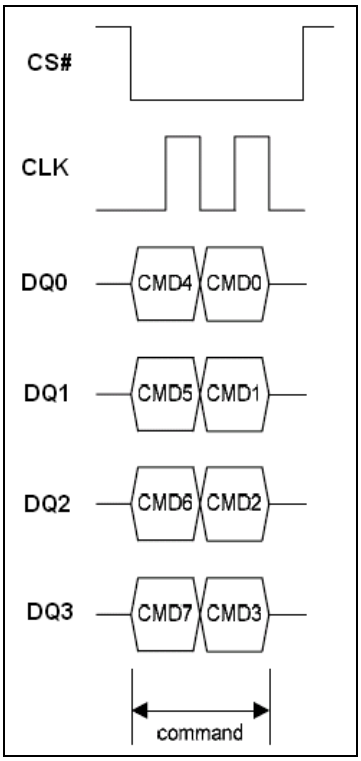
Enter 4-Byte Address Mode instruction (QPI Mode)

Exit 4-Byte Address Mode (E9h)

The Exit 4byte address mode instruction is executed to exit the 4-byte address mode and return to the default 3-bytes address mode. After sending out the exit 4byte address mode instruction, the 4byte (ADS) bit of Status Register 3 will be cleared to be "0" to indicate the exit of the 4-byte address mode. Once exiting the 4-byte address mode, the address length will return to 24-bit.
The sequence of issuing Exit 4-Byte Address Modes instruction is: CS# goes low → sending exit 4byte address mode instruction to exit 4-byte mode (automatically clear the ADS bit to be "0") → CS# goes high. (Exit 4byte address mode Instruction Sequence Diagram figure for SPI mode, and for EQPI mode).



Exit 4-Byte Address Mode instruction (SPI Mode)



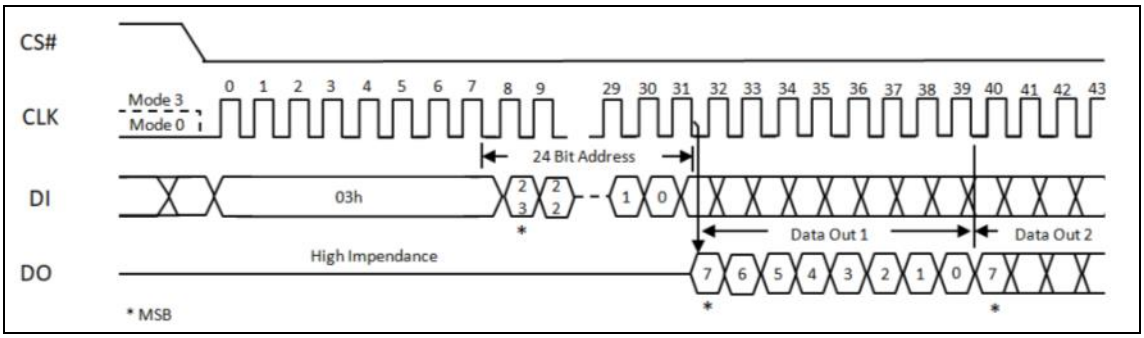
Exit 4-Byte Address Mode instruction (QPI Mode)

Read Data (03h)

The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read Data Bytes (READ) instruction is followed by a 3-byte address (A23-A0) or 4-byte address (A31-A0) (depending on mode state), each bit being latched-in during the rising edge of Serial Clock (CLK). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency f_R, during the falling edge of Serial Clock (CLK).

The first byte addressed can be at any location. To access higher address (larger than 128Mb) in 3 byte address mode, user can issue Write Extended Register (C5h) operation before Read Data Bytes (03h). The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data (READ) instruction.

The Read Data Bytes (READ) instruction is terminated by driving Chip Select (CS#) high. Chip Select (CS#) can be driven high at any time during data output. Any Read Data Bytes (READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

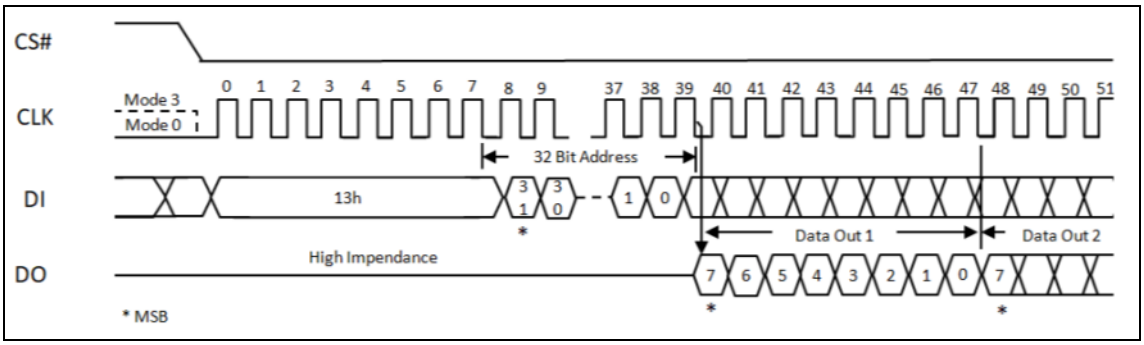


Note: The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Read Data Instruction (SPI Mode only)

Read Data with 4-Byte Address (13h)

The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read Data Bytes with 4bytes address instruction is followed by a 4-byte address (A31-A0), each bit being latched-in during the rising edge of Serial Clock (CLK). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency f_R, during the falling edge of Serial Clock (CLK).
The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes with 4byte address instruction. The Read Data Bytes with 4 byte address instruction is terminated by driving Chip Select (CS#) high. Chip Select (CS#) can be driven high at any time during data output. Any Read Data Bytes with 4byte address instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.



Note: This instruction is workable while in 4byte address mode.

The Read Data with 4-Byte Address instruction (SPI mode only)

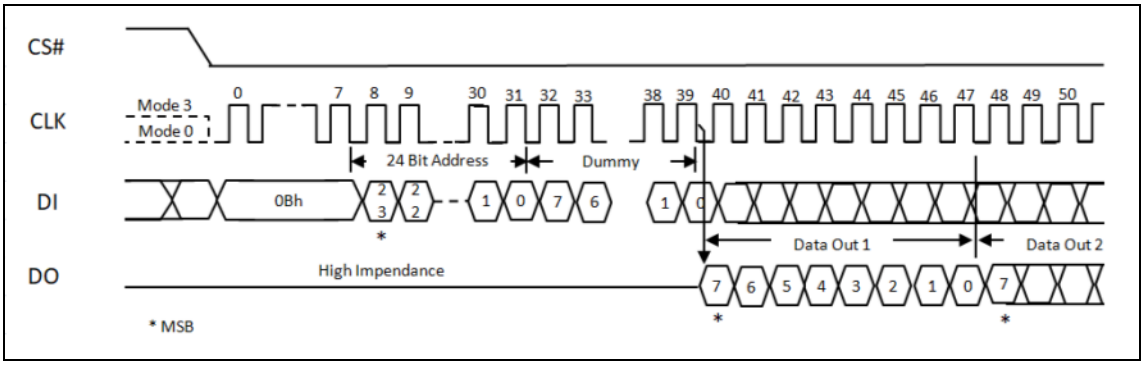
Fast Read (0Bh)

The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Fast Read instruction is followed by a 3-byte address (A23-A0) or 4-byte address (A31-A0) (depending on address mode state) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (CLK). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency F_R, during the falling edge of Serial Clock (CLK).

The first byte addressed can be at any location. To access higher address (larger than 128Mb) in 3 byte address mode, user can issue Write Extended Register (C5h) operation before Fast Read (0Bh). The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Fast Read instruction.

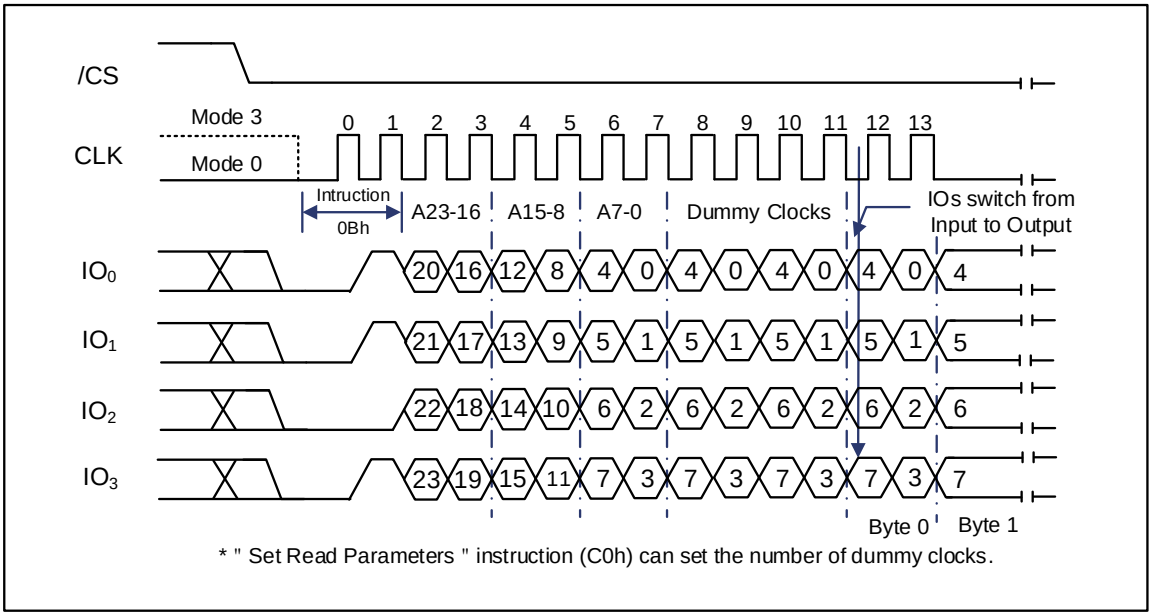
The Fast Read instruction is terminated by driving Chip Select (CS#) high. Chip Select (CS#) can be driven high at any time during data output. Any Fast Read instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

The instruction sequence is shown in Fast Read Instruction in QPI Mode figure while using the Enter QPI mode (EQPI) (38h) command.



Note: The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased

Fast Read Instruction (SPI Mode)



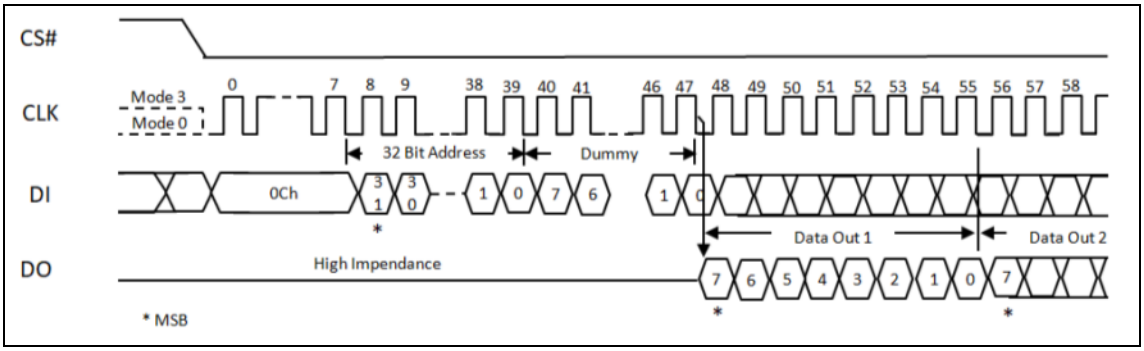
Note:

1. The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.
2. The dummy clock can be set by Set Parameter command (C0h)

Fast Read Instruction (QPI Mode)

Fast Read with 4-Byte Address (0Ch)

The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Fast Read with 4-byte address instruction is followed by a 4-byte address (A31-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (CLK). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency F_R, during the falling edge of Serial Clock (CLK).
The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Fast Read with 4-byte address instruction.
The Fast Read with 4-byte address instruction is terminated by driving Chip Select (CS#) high. Chip Select (CS#) can be driven high at any time during data output. Any Fast Read with 4-byte address instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.
This command (0Ch) is changed to “Burst Read with Wrap” while at EQPI mode.

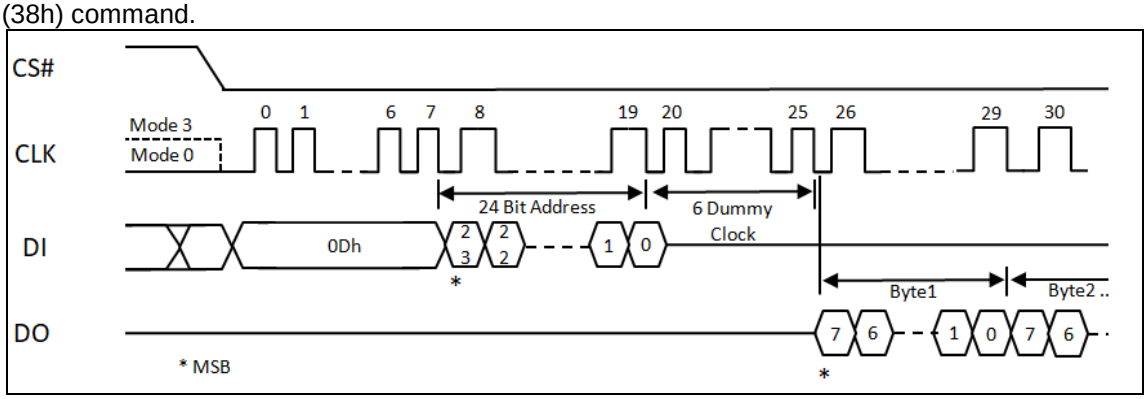


Note: This instruction is workable while in 4byte address mode

Fast Read with 4-Byte Address Instruction (SPI mode only)

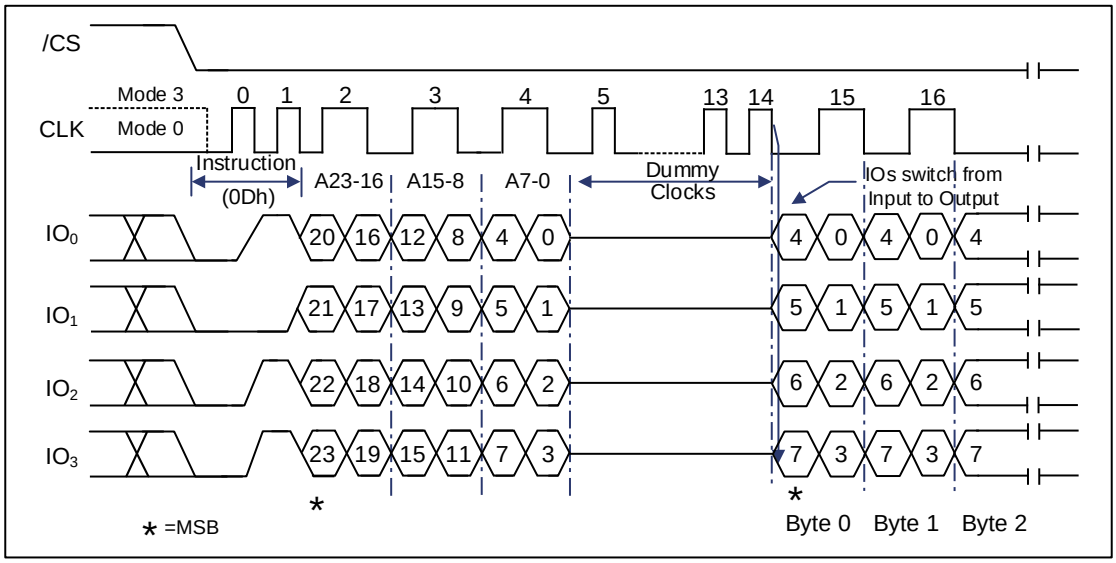
DTR Fast Read (0Dh)

The DDR Fast Read instruction is for doubling reading data out, signals are triggered on both rising and falling edge of clock. The address is latched on both rising and falling edge of CLK, and data of each bit shifts out on both rising and falling edge of CLK at a maximum frequency F_R. The 2-bit address can be latched-in at one clock, and 2-bit data can be read out at one clock, which means one bit at rising edge of clock, the other bit at falling edge of clock. The first address byte can be at any location.
The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DDR Fast Read instruction.
The sequence of issuing DDR Fast Read instruction is: CS# goes low -> sending DDR Fast Read instruction code (1 bit per clock) -> 3-byte address (or 4-byte address, depends on address mode state) on DI (2-bit per clock) -> 6 dummy clocks (default) on DI -> data out on DO (2-bit per clock) -> to end DDR Fast Read operation can use CS# to high at any time during data out.
While Program/ Erase/ Write Status Register cycle is in progress, DDR Fast Read instruction is rejected without any impact on the Program/ Erase/ Write Status Register current cycle.
The instruction sequence is shown in DDR Fast Read Instruction in QPI Mode figure using the Enter QPI mode (EQPI) (38h) command.



Note:
1. The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.
2. The dummy clock number can be set by SR3.4 and SR3.3

DTR Fast Read Instruction (SPI Mode)

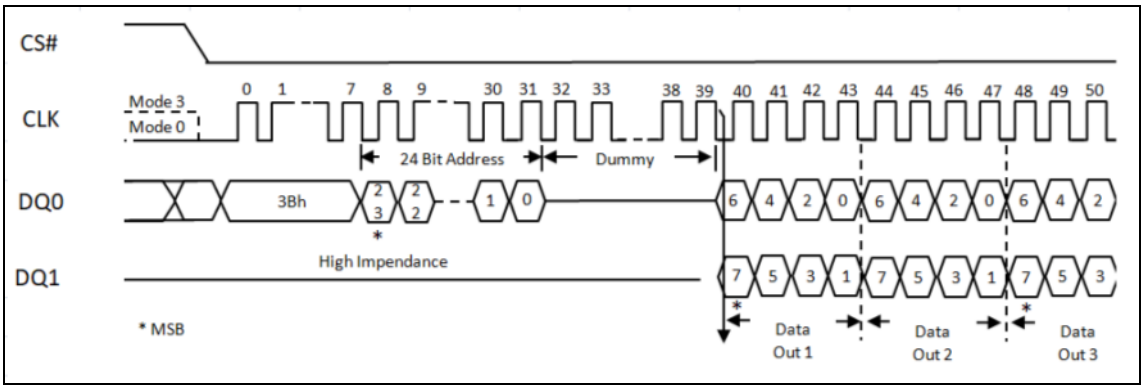


Note:
1. The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.
2. The dummy clock can be set by Set Parameter command(C0h)

DTR Fast Read Instruction (QPI Mode)

Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins, DQ_0 and DQ_1, instead of just DQ_1. This allows data to be transferred from the device at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from to RAM upon power-up or for applications that cache code-segments to RAM for execution.
Similar to the Fast Read instruction, the Fast Read Dual Output instructions can operation at the highest possible frequency of F_R (see **AC Electrical Characteristics**). This is accomplished by adding eight "dummy clocks after the 24-bit address (or 32-bit address depends on address mode state) as shown in Fast Read Dual Output Instruction figure.
The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clock is "don't care". However, the DI pin should be high-impedance prior to the falling edge of the first data out clock.



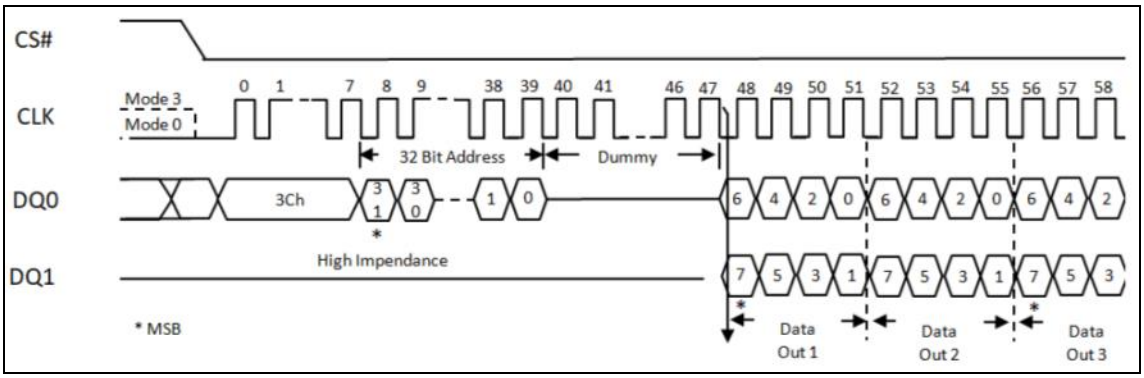
Note: The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Fast Read Dual Output Instruction (SPI Mode only)

Fast Read Dual Output with 4-Byte Address (3Ch)

The Fast Read Dual Output with 4-byte address (3Ch) is similar to the standard Fast Read with 4-byte address (0Ch) instruction except that data is output on two pins, DQ_0 and DQ_1, instead of just DQ_1. This allows data to be transferred from the device at twice the rate of standard SPI device's. The Fast Read Dual Output with 4-byte address instruction is ideal for quickly downloading code from to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read with 4-byte address instruction, the Fast Read Dual Output with 4-byte address instruction can operation at the highest possible frequency of F_R (see **AC Electrical Characteristics**). This is accomplished by adding eight dummy clocks after the 32-bit address as shown in Fast Read Dual Output with 4-byte address Instruction figure. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clock is "don't care". However, the DI pin should be high-impedance prior to the falling edge of the first data out clock.

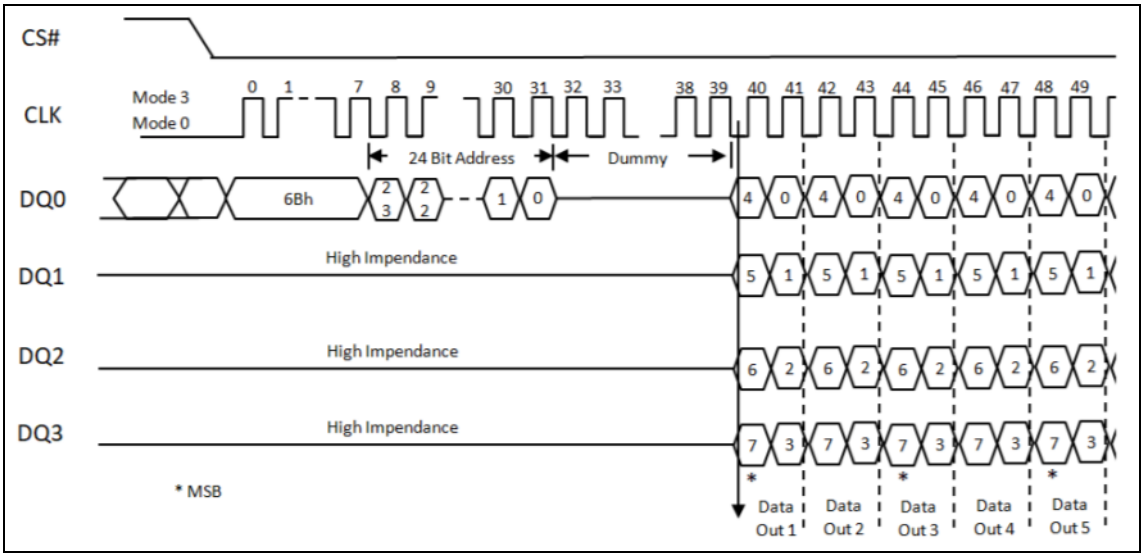


Note: This instruction is workable while in 4byte address mode.

Fast Read Dual Output with 4-Byte Address Instruction (SPI Mode only)

Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output through four pins, DQ_0, DQ_1, DQ_2 and DQ_3 and eight dummy clocks(default) are required prior to the data output.
The Fast Read Quad Output (6Bh) address is latching on rising edge of CLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of CLK at a maximum frequency F_R.
The first address can be any location. To access higher address (larger than 128Mb) in 3 byte address mode, user can issue Write Extended Register (C5h) operation before Fast Read Quad Output (6Bh). The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single Fast Read Quad Output instruction.
The sequence of issuing Fast Read Quad Output (6Bh) instruction is: CS# goes low -> sending Fast Read Quad Output (6Bh) instruction -> 24-bit address/32-bit address on DQ_0 (depends on address mode state) -> 8 dummy clocks -> data out interleave on DQ_3, DQ_2, DQ_1 and DQ_0 -> to end Fast Read Quad Output (6Bh) operation can use CS# to high at any time during data out. The QE bit must set to 1 before issue Fast Read Quad Output command and DQ pins should be high impendence until the falling edge of first data out.

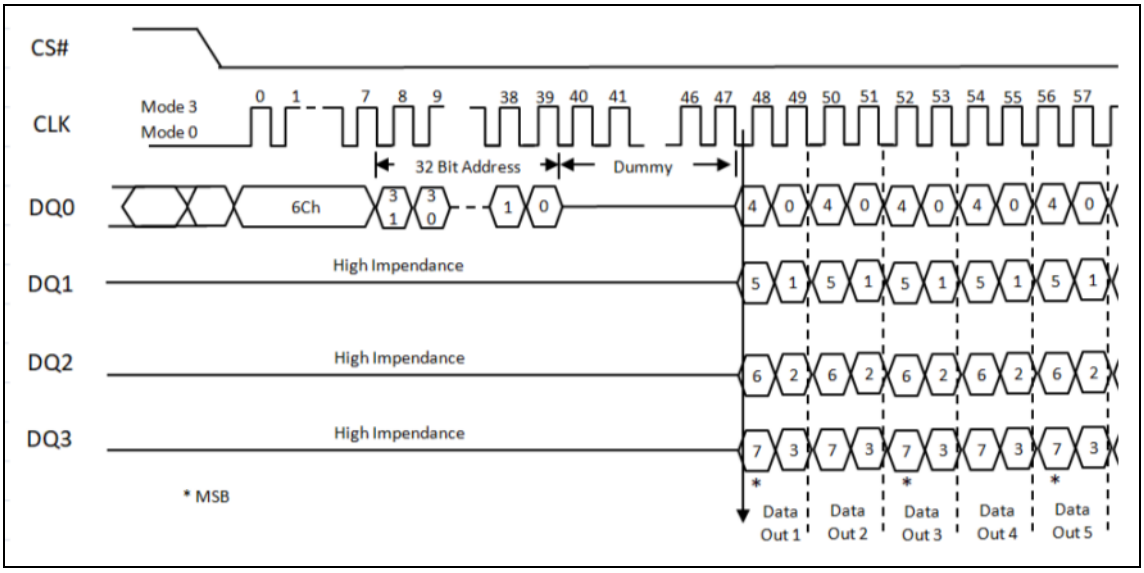


Note: The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Fast Read Quad Output Instruction (SPI Mode only)

Fast Read Quad Output with 4-Byte Address (6Ch)

The Fast Read Quad Output with 4-byte address (6Ch) instruction is similar to the Fast Read Dual Output with 4-byte address(3Ch) instruction except that data is output through four pins, DQ_0, DQ_1, DQ_2 and DQ_3 and eight dummy clocks are required prior to the data output.
The Fast Read Quad Output with 4-byte address(6Ch) address is latching on rising edge of CLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of CLK at a maximum frequency F_R. The first address can be any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single Quad Output Fast Read with 4byte address instruction.
The sequence of issuing Fast Read Quad Output with 4-byte address (6Ch) instruction is: CS# goes low -> sending Fast Read Quad Output with 4-byte address (6Ch) instruction -> 32-bit address on DQ_0 -> 8 dummy clocks -> data out interleave on DQ_3, DQ_2, DQ_1 and DQ_0 -> to end Fast Read Quad Output with 4-byte address (6Ch) operation can use CS# to high at any time during data out. The QE bit must set to 1 before issue Fast Read Quad Output command and DQ pins should be high impendence until the falling edge of first data out.

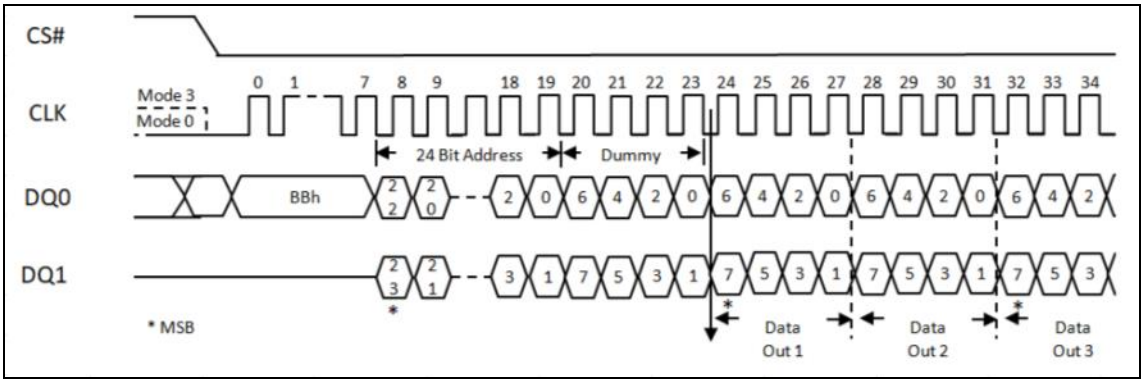


Note: This instruction is workable while in 4byte address mode.

Fast Read Quad Output with 4-Byte Address Instruction (SPI mode)

Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, DQ_0 and DQ_1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23-A0 or A31-A0, depends on address mode) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.
The Fast Read Dual I/O instruction enables double throughput of Serial Flash in read mode. The address is latched on rising edge of CLK, and data of every two bits (interleave 2 I/O pins) shift out on the falling edge of CLK at a maximum frequency. The first address can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single Fast Read Dual I/O instruction. Once writing Fast Read Dual I/O instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.



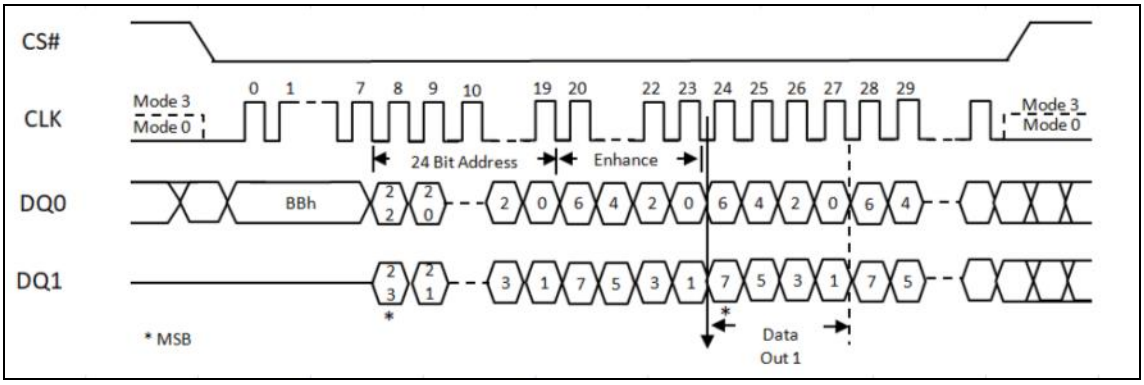
Note:

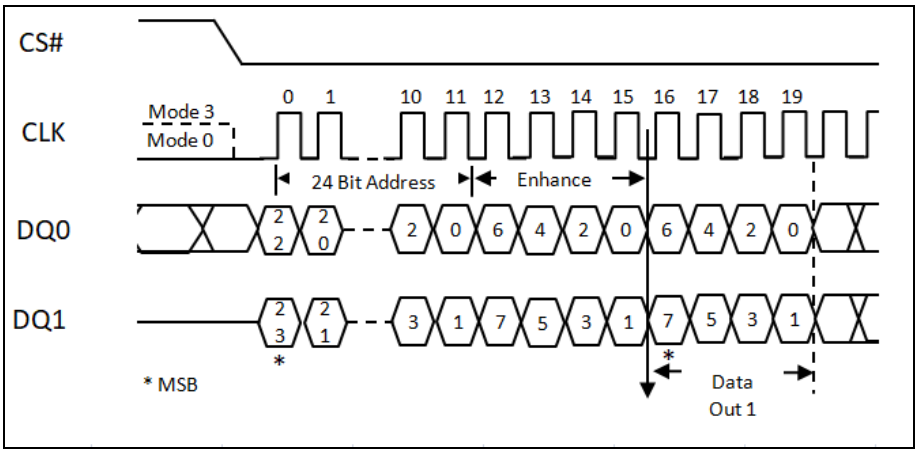
1. The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.
2. Set dummy clock by SR3.3, SR3.4

Fast Read Dual I/O Instruction (SPI Mode only)

Another sequence of issuing Fast Read Dual I/O (BBh) instruction especially useful in random access is: CS# goes low -> sending Fast Read Dual I/O (BBh) instruction -> 24-bit address (or 32-bit address, depends on address mode) interleave on DQ_1 and DQ_0 -> performance enhance byte, P[5:4]=10b -> data out interleave on DQ_1 and DQ_0 till CS# goes high -> CS# goes low (reduce Fast Read Dual I/O (BBh) instruction) -> 24-bit random access address.

In the performance – enhancing mode, P[5:4]=10b, can make this mode continue and reduce the next Fast Read Dual I/O (BBh) instruction. Once P[5:4] is no longer equal to 10b. These commands will reset the performance enhance mode. And afterwards CS# is raised or issuing FFFFh (16 clocks at DI) instead of P[4]=1, the system then will escape from performance enhance mode and return to normal operation.
While Program/ Erase/ Write Status Register is in progress, Fast Read Dual I/O (BBh) instruction is rejected without impact on the Program/ Erase/ Write Status Register current cycle.





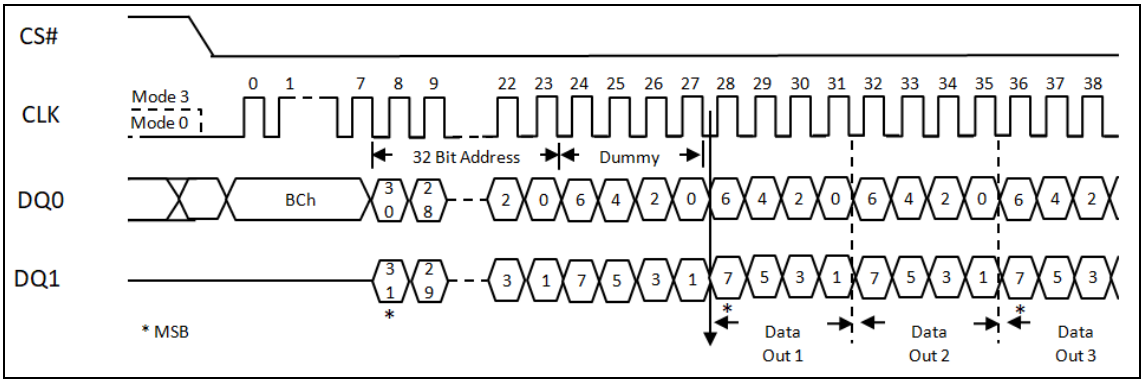
Note:

1. The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.
2. Set Dummy clock by SR3.3, SR3.4

Fast Read Dual I/O Instruction (Previous instruction set P5-4 = 10, SPI Mode only)

Fast Read Dual I/O with 4-Byte Address (BCh)

The Fast Read Dual I/O with 4-byte address (BCh) instruction allows for improved random access while maintaining two IO pins, DQ_0 and DQ_1. It is similar to the Fast Read Dual Output with 4-byte address (3Ch) instruction but with the capability to input the Address bits (A31-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.
The Fast Read Dual I/O with 4-byte address instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of CLK, and data of every two bits (interleave 2 I/O pins) shift out on the falling edge of CLK at a maximum frequency. The first address can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single Fast Read Dual I/O with 4byte address instruction. Once writing Fast Read Dual I/O with 4-byte address instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

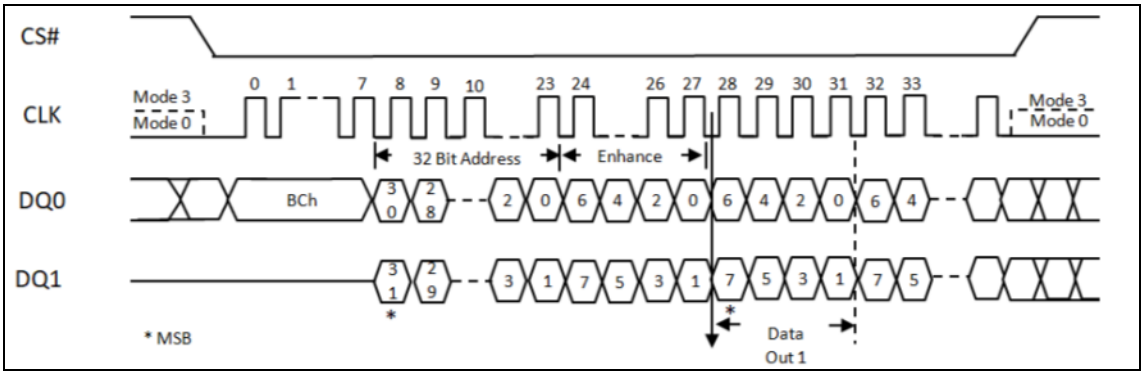


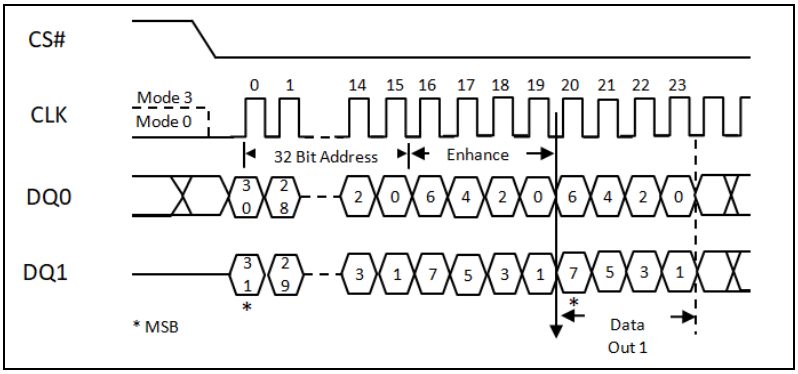
Note

1. This instruction is workable while in 4byte address mode.
2. Set Dummy clock by SR3.3, SR3.4

Fast Read Dual I/O with 4-Byte Address Instruction (SPI Mode only)

Another sequence of issuing Fast Read Dual I/O with 4-byte address (BCh) instruction especially useful in random access is: CS# goes low -> sending Fast Read Dual I/O with 4-byte address(BCh) instruction -> 32-bit address interleave on DQ_1 and DQ_0 -> performance enhance byte, P[5:4]=10b -> data out interleave on DQ_1 and DQ_0 till CS# goes high -> CS# goes low (reduce Fast Read Dual I/O with 4-byte address(BCh) instruction) -> 32-bit random access address.
In the performance – enhancing mode, P[5:4]=10b, can make this mode continue and reduce the next Fast Read Dual I/O with 4-byte address(BCh) instruction. Once P[5:4] is no longer equal to 10b. These commands will reset the performance enhance mode. And afterwards CS# is raised or issuing FFFFFh (20 clocks at DI) instead of P[4]=1, the system then will escape from performance enhance mode and return to normal operation. While Program/ Erase/ Write Status Register is in progress, Fast Read Dual I/O with 4-byte address (BCh) instruction is rejected without impact on the Program/ Erase/ Write Status Register current cycle.





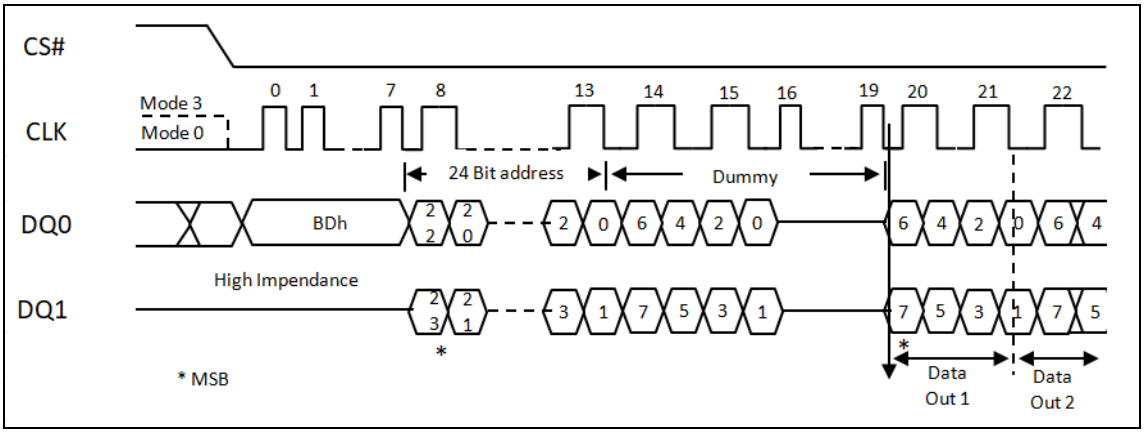
Note:

1. This instruction is workable while in 4byte address mode.
2. Set Dummy clock by SR3.3, SR3.4

Fast Read Dual I/O with 4-Byte Address Instruction with Enhance mode (Previous instruction set M5-4 =10, SPI Mode only)

DTR Fast Read Dual I/O (BDh)

The DTR Fast Read Dual I/ O (BDh) instruction enables Double Data Rate throughput on dual I/O of Serial Flash in read mode. The address (interleave on dual I/O pins) is latched on both rising and falling edge of CLK, and data (interleave on dual I/O pins) shift out on both rising and falling edge on CLK at a maximum frequency F_R. The 4-bit address can be latched-in at one clock, and 4-bit data can be read out at one clock, which means two bits at rising edge of clock, the other two bits at falling edge of clock. The first address byte can be at any location.
The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DTR Fast Read Dual I/O (BDh) instruction. Once writing DDR Fast read Dual I/O (BDh) instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.
The sequence of issuing DDR Fast Read Dual I/O (BDh) instruction is: CS# goes low -> sending DDR Fast Read Dual I/O (BDh) instruction (1-bit per clock) -> 24-bit bit address (or 32-bit address, depends on address mode state) interleave on DQ_1 and DQ_0 (4-bit per clock) -> 3 dummy byte (6 clocks) -> data out interleave on DQ_1 and DQ_0 (4-bit per clock) -> to end DDR Fast Read Dual I/O (BDh) operation can use CS# to high at any time during data out.



Note.

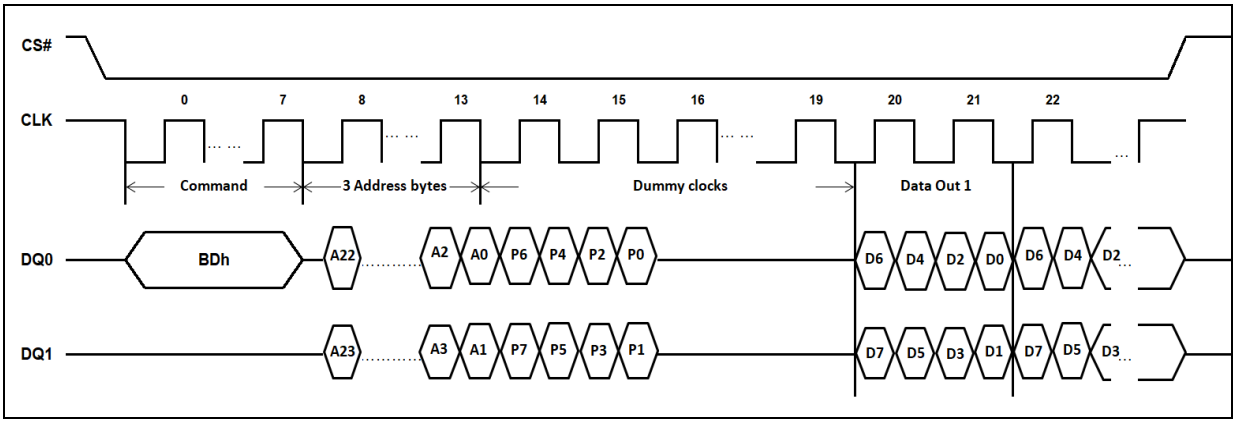
1. The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.
2. Set Dummy clock by SR3.3, SR3.4

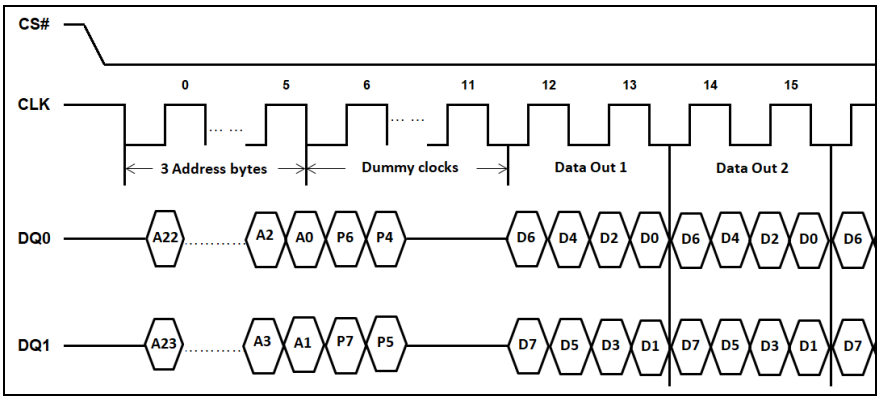
DDR Fast Read Dual I/O Instruction (SPI mode only)

Another sequence of issuing DDR Fast Read Dual I/O (BDh) instruction especially useful in random access is: CS# goes low -> sending DDR Fast Read Dual I/O (BDh) instruction -> 24-bit address (or 32-bit address, depends on address mode state) interleave on DQ_1 and DQ_0 -> performance enhance bits, P[5:4]=10b and 2byte dummy-> data out interleave on DQ_1 and DQ_0 till CS# goes high -> CS# goes low (reduce DDR Fast Read Dual I/O (BDh) instruction) -> 24-bit (or 32-bit address, depends on address mode state) random access address.

In the performance – enhancing mode, P[5:4]=10b, can make this mode continue and reduce the next DDR Fast Read Dual I/O (BDh) instruction. Once P[5:4] is no longer equal to 10b. These commands will reset the performance enhance mode. And afterwards CS# is raised or issuing FFFFh/FFFFFh command (CS# goes high -> CS# goes low -> sending FFFFh/FFFFFh at DQ_0 (16/20 clocks)-> CS# goes high) instead of P[4] not equals to 0b, the system then will escape from performance enhance mode and return to normal operation.

While Program/ Erase/ Write Status Register is in progress, DDR Fast Read Dual I/O (BDh) instruction is rejected without impact on the Program/ Erase/ Write Status Register current cycle.





Note. The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

DTR Fast Read Dual I/O with enhance mode (SPI mode only)

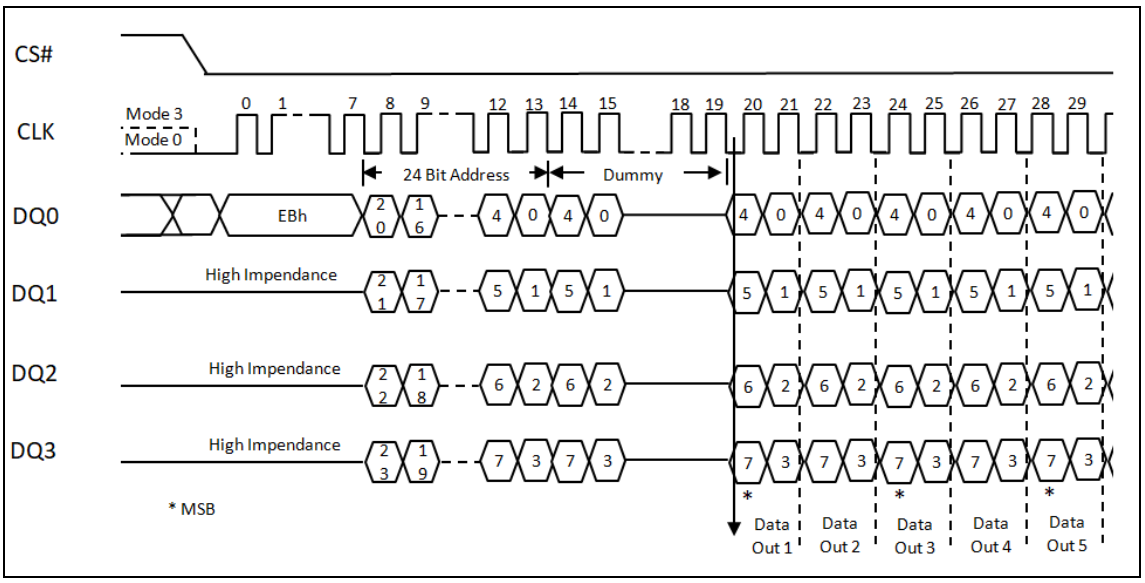
Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins, DQ_0, DQ_1, DQ_2 and DQ_3 and six dummy clocks are required prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI.

The Fast Read Quad I/O (EBh) instruction enable quad throughput of Serial Flash in read mode. The address is latching on rising edge of CLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of CLK at a maximum frequency F_R. The first address can be any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single Fast Read Quad I/O instruction. Once writing Fast Read Quad I/O instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing Fast Read Quad I/O (EBh) instruction is: CS# goes low -> sending Fast Read Quad I/O (EBh) instruction -> 24-bit address (or 32-bit address depends on address mode) interleave on DQ_3, DQ_2, DQ_1 and DQ_0 -> 6 dummy clocks -> data out interleave on DQ_3, DQ_2, DQ_1 and DQ_0 -> to end Fast Read Quad I/O (EBh) operation can use CS# to high at any time during data out. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction

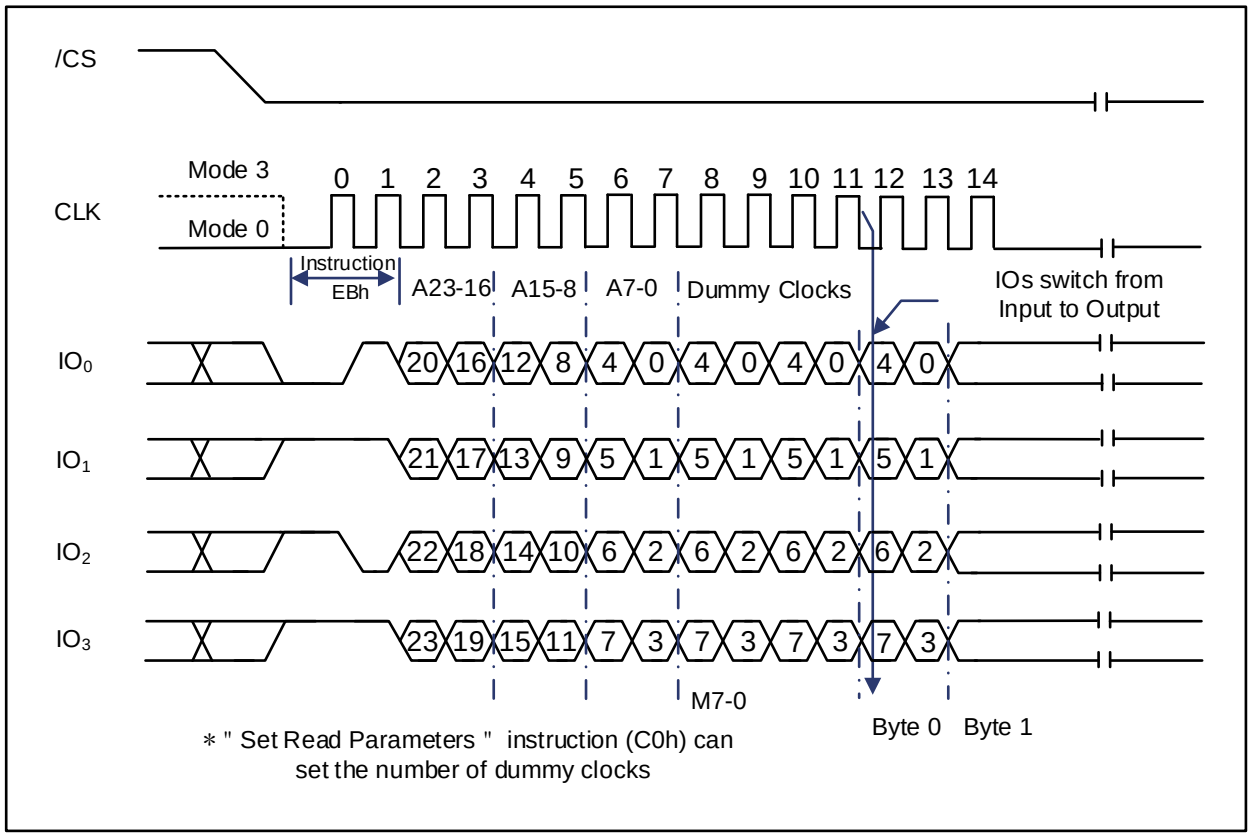
The instruction is also workable while using the Enter QPI mode (EQPI) (38h) command.



Note.

1. The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.
2. The dummy clock can be set by SR3.3, SR3.4

Fast Read Quad I/O Instruction (SPI mode)



Note.

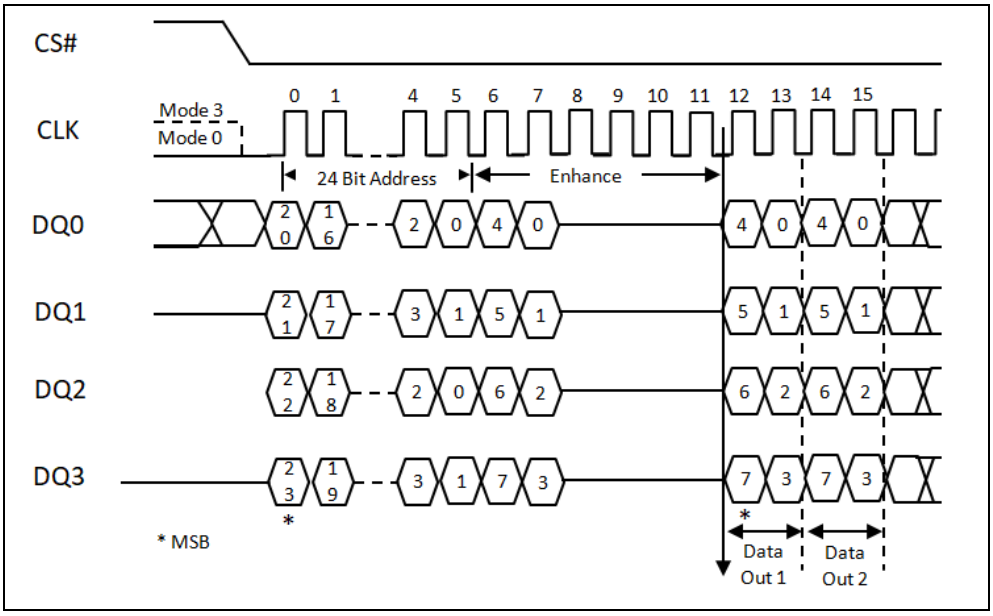
1. The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.
2. The dummy clock can be changed by Set Parameter(C0h)

Fast Read Quad I/O Instruction (QPI mode)

Another sequence of issuing Fast Read Quad I/O (EBh) instruction especially useful in random access is: CS# goes low -> sending Fast Read Quad I/O (EBh) instruction -> 24-bit (or 32-bit, depends on address mode state) address interleave on DQ_3, DQ_2, DQ_1 and DQ_0 -> one performance enhance byte P[5:4]=(1,0) and 4 dummy clocks -> data out interleave on DQ_3, DQ_2, DQ_1 and DQ_0 till CS# goes high -> CS# goes low (reduce Fast Read Quad I/O (EBh) instruction) -> 24-bit (or 32-bit, depends on address mode state) random access address.

In the performance – enhancing mode, P[5:4] must be equals to (1,0) and make this mode continue and reduce the next Fast Read Quad I/O (EBh) instruction. Once P[5:4] is no longer equals to (1, 0). These commands will reset the performance enhance mode. And afterwards CS# is raised or issuing FFh command (CS# goes high -> CS# goes low -> sending FFh (8 clock) at DQ_0 -> CS# goes high) instead of P4=1, the system then will escape from performance enhance mode and return to normal operation.

While Program/ Erase/ Write Status Register is in progress, Fast Read Quad I/O (EBh) instruction is rejected without impact on the Program/ Erase/ Write Status Register current cycle.
The performance-enhancing mode is also supported using the Enter QPI mode (EQPI) (38h) command.



Note.

1. The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.
2. The dummy clock can be set by SR3.3, SR3.4 (SPI mode) or Set Parameter(C0h)

Fast Read Quad I/O with Performance-enhance mode (SPI mode and QPI mode)

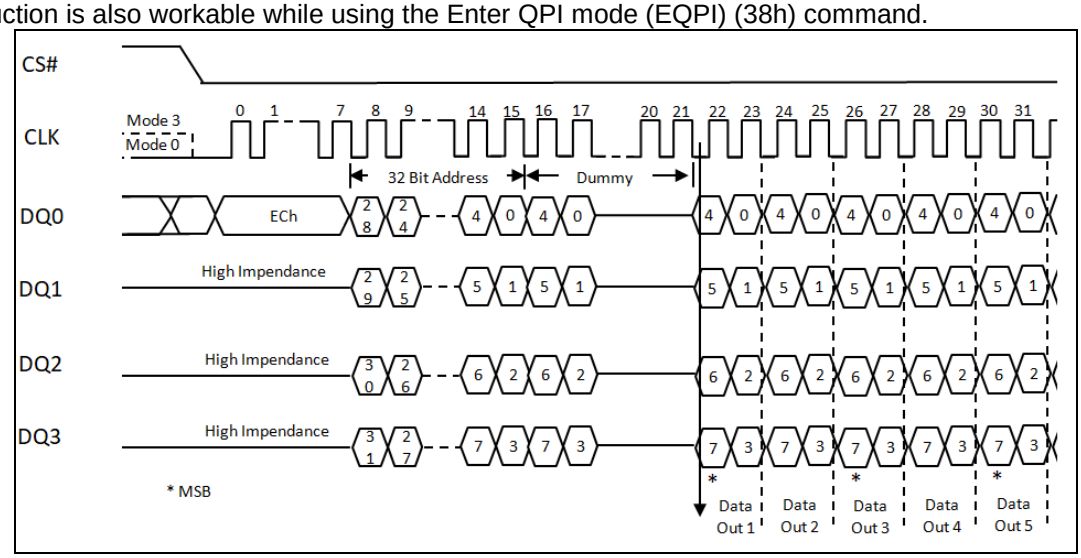
Quad Input/Output Fast Read with "8/16/32/64 byte Wrap Around"

The Fast Read Quad I/O command can be used to access a specific portion within a page by issuing "Set Burst with Wrap" (77h) commands prior to EBh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following EBh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.
The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The "Set Burst with Wrap" command allows three "Wrap Bits" W6-W4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-W5 is used to specify the length of the wrap around section within a page.

"Wrap Around" feature is not available in QPI mode for Fast Read Quad I/O Fast Read instruction. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated "Burst Read with Wrap" (0Ch) instruction must be used.

Fast Read Quad I/O with 4-Byte Address (ECh)

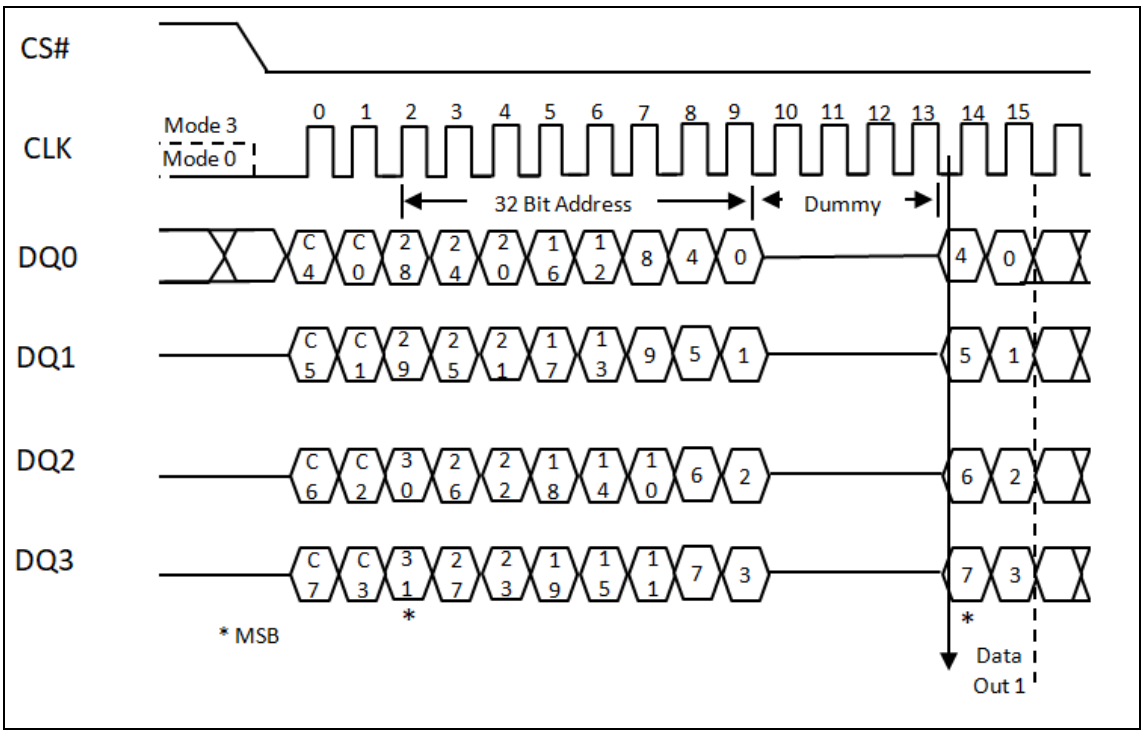
The Fast Read Quad I/O with 4byte address(ECh) instruction is similar to the Dual I/O Fast Read with 4byte address(BCh) instruction except that address and data bits are input and output through four pins, DQ_0, DQ_1, DQ_2 and DQ_3 and six dummy clocks are required prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI.
The Fast Read Quad I/O with 4byte address (ECh) instruction enable quad throughput of Serial Flash in read mode. The address is latching on rising edge of CLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of CLK at a maximum frequency F_R. The first address can be any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single Fast Read Quad I/O with 4byte address instruction. Once writing Fast Read Quad I/O with 4byte address instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.
The sequence of issuing Fast Read Quad I/O with 4byte address (ECh) instruction is: CS# goes low -> sending Fast Read Quad I/O with 4byte address (ECh) instruction -> 32-bit address interleave on DQ_3, DQ_2, DQ_1 and DQ_0 -> 6 dummy clocks -> data out interleave on DQ_3, DQ_2, DQ_1 and DQ_0 -> to end Fast Read Quad I/O with 4byte address (ECh) operation can use CS# to high at any time during data out.
The instruction is also workable while using the Enter QPI mode (EQPI) (38h) command.



Note:

1. This instruction is workable while in 4byte address mode.
2. Set Dummy clock by SR3.3, SR3.4

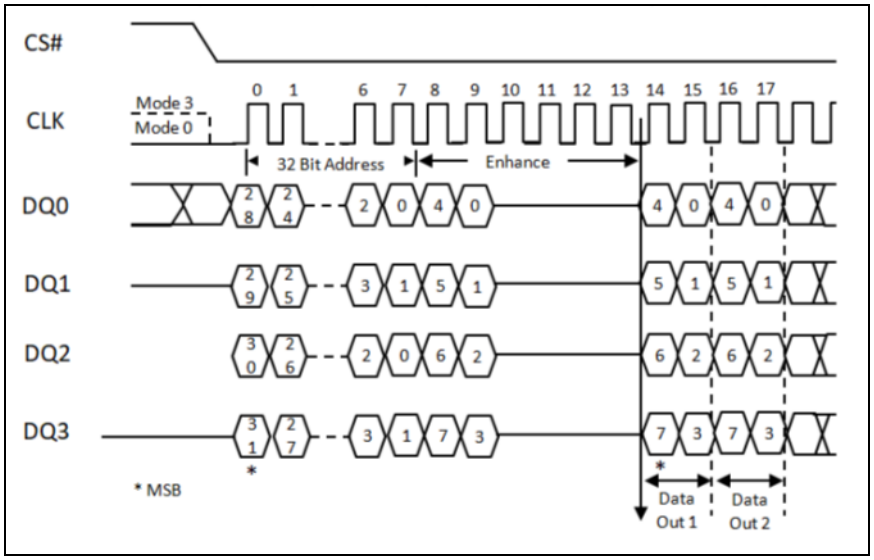
Fast Read Quad I/O with 4-Byte Address Instruction (SPI Mode)



Note:

1. This instruction is workable while in 4byte address mode.
2. Set Dummy clock by C0h

Fast Read Quad I/O with 4-Byte Address Instruction (QPI Mode)



Note:

1. This instruction is workable while in 4byte address mode.
2. The dummy clock counts can be changed by SPI or QPI mode

Fast Read Quad I/O with 4-byte address Instruction with Enhance mode (previous M[5:4]=(1,0))(SPI and QPI mode)

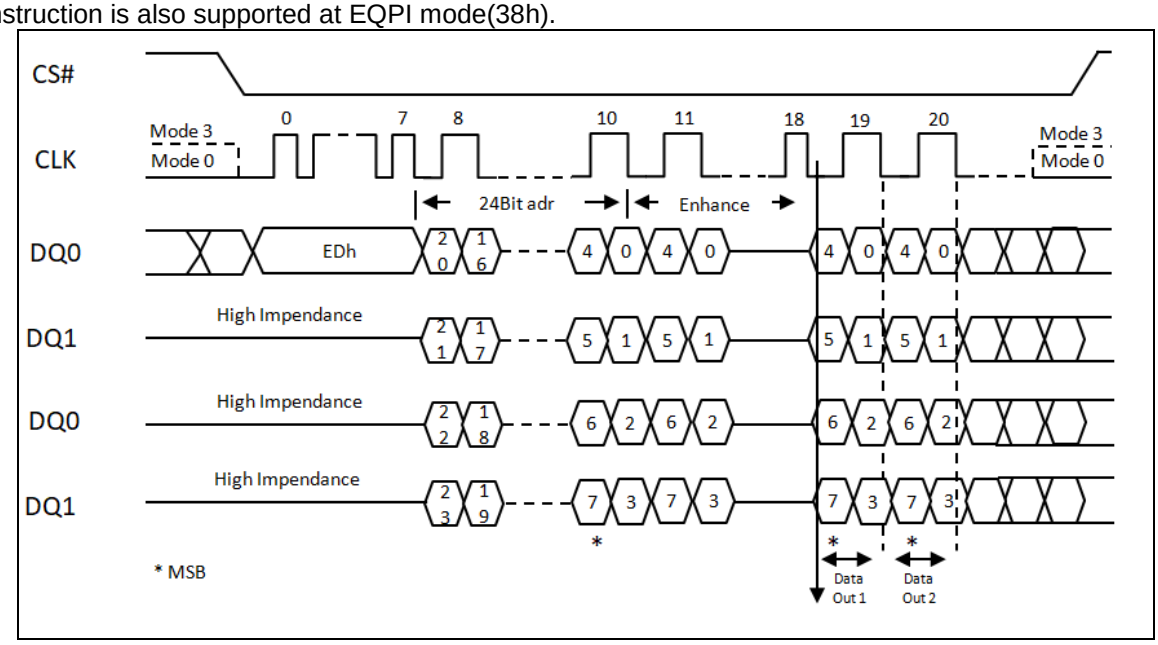
DTR Fast Read Quad I/O (EDh)

The DTR Fast Read Quad I/O (EDh) instruction enable Double Data Rate throughput on quad I/O of Serial Flash in read mode. The address (interleave on 4 I/O pins) is latched on both rising and falling edge of CLK, and data (interleave on 4 I/O pins) shift out on both rising and falling edge on CLK at a maximum frequency F_R. The 8-bit address can be latched-in at one clock, and 8-bit data can be read out at one clock, which means four bits at rising edge of clock, the other four bits at falling edge of clock. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DTR Fast Read Quad I/O (EDh) instruction. Once writing DTR Fast Read Quad I/O (EDh) instruction, the following address/dummy/data out will perform as 8-bit instead of previous 1-bit.

The sequence of issuing DTR Fast Read Quad I/O (EDh) instruction is: CS# goes low -> sending DTR Fast Read Quad I/O (EDh) instruction (1-bit per clock) -> 24-bit address (or 32 bit address depends on address mode state) interleave on DQ_3, DQ_2, DQ_1 and DQ_0 (8-bit per clock) -> 8 dummy byte (8 clocks) -> data out interleave on DQ_3, DQ_2, DQ_1 and DQ_0 (8-bit per clock) -> to end DTR Fast Read Quad I/O (EDh) operation can use CS# to high at any time during data out.

The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

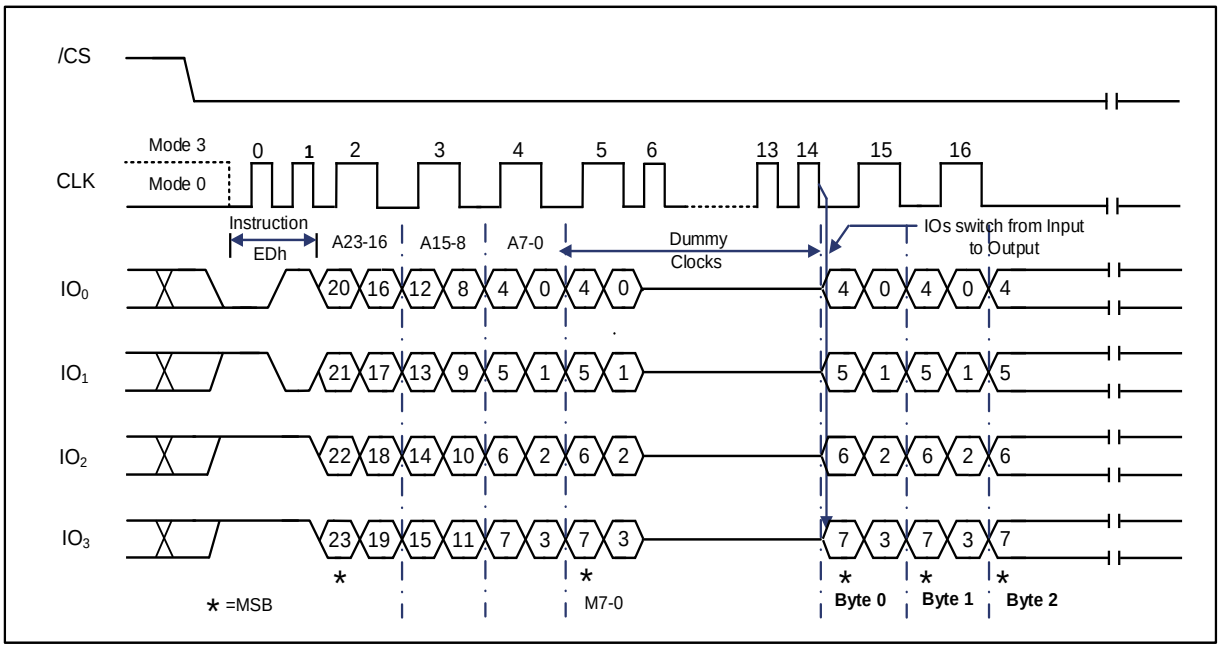
This instruction is also supported at EQPI mode(38h).



Note:

1. The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.
2. The dummy clocks can be set by SR3.4, SR.3

DTR Fast Read Quad I/O Instruction (SPI mode)



Note:

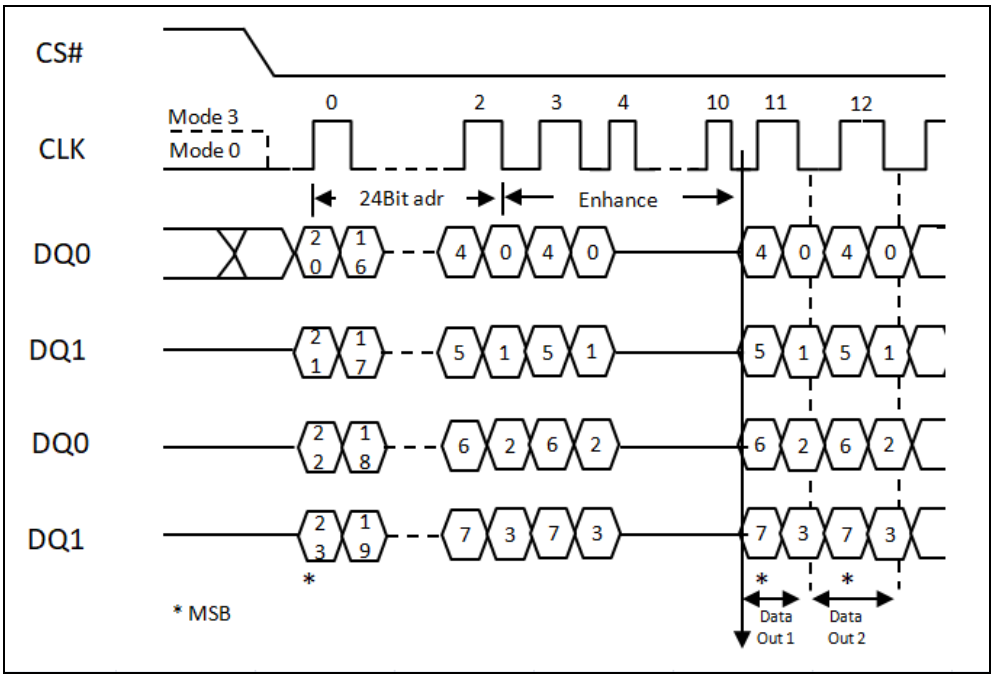
1. The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.
2. The dummy clock can be set by Set Parameter(C0h)

DTR Fast Read Quad I/O Instruction (QPI mode)

Another sequence of issuing enhanced mode of DTR Fast Read Quad I/O (EDh) instruction especially useful in random access is: CS# goes low -> sending DTR Fast Read Quad I/O (EDh) instruction (1-bit per clock) -> 24-bit address (or 32 bit address depends on address mode state) interleave on DQ_3, DQ_2, DQ_1 and DQ_0 (8-bit per clock) -> one performance enhance byte, P[5:4]=(1,0) -> 7 dummy byte (7 clocks) -> data out (8-bit per clock) still CS# goes high -> CS# goes low (eliminate DTR Fast Read Quad I/O) -> 24-bit random access address (or 32 bit address depends on address mode).

In the performance – enhancing mode, P[5:4] must be equals to (1,0) and make this mode continue and reduce the next DTR Fast Read Quad I/O (EDh) instruction. Once P[5:4] is no longer equals to (1, 0). These commands will reset the performance enhance mode. And afterwards CS# is raised or issuing FFh/3FFh (CS# goes high -> CS# goes low -> sending FFh/3FFh (8 clock/10 clock) at DQ0 -> CS# goes high) instead of P4=1, the system then will escape from performance enhance mode and return to normal operation.

While Program/ Erase/ Write Status Register cycle is in progress, DTR Fast Read Quad I/O (EDh) instruction is rejected without any impact on the Program/ Erase/ Write Status Register current cycle.



Note:

1. The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.
2. The dummy clocks can be set by SR3.4, SR.3(SPI mode) or Set Parameter(C0h)(QPI mode)

DTR Fast Read Quad I/O Instruction with Enhance mode (SPI mode and QPI mode)

DTR Fast Read Quad I/O with "8/16/32/64 byte Wrap Around"

The DTR Fast Read Quad I/O command can be used to access a specific portion within a page by issuing "Set Burst with Wrap" (77h) commands prior to EDh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following EDh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

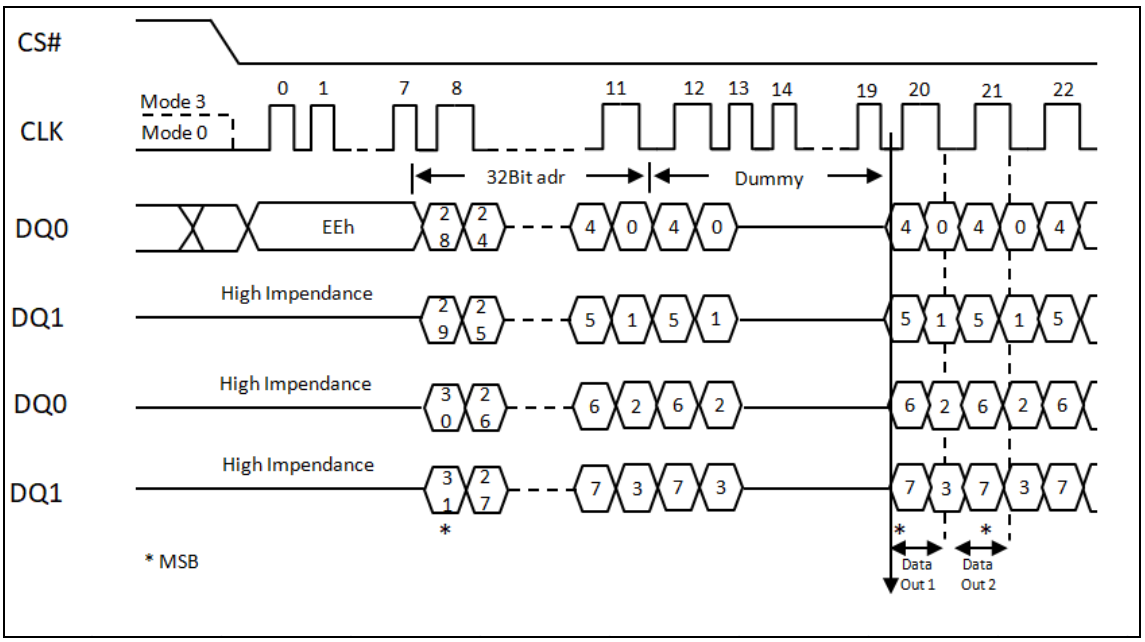
The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The "Set Burst with Wrap" command allows three "Wrap Bits" W6-W4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-W5 is used to specify the length of the wrap around section within a page.

"Wrap Around" feature is not available in QPI mode for DTR Fast Read Quad I/O instruction. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated "Burst Read with Wrap" (0Ch) instruction must be used.

In QPI mode, the "Wrap Around" feature is not available for DTR Fast Read Quad I/O instruction. To perform a wrap-around read operation with a fixed data length in QPI mode, a dedicated "DTR Burst Read with Wrap" (0Eh) instruction must be adopted.

DTR Fast Read Quad I/O with 4-Byte Address (EEh)

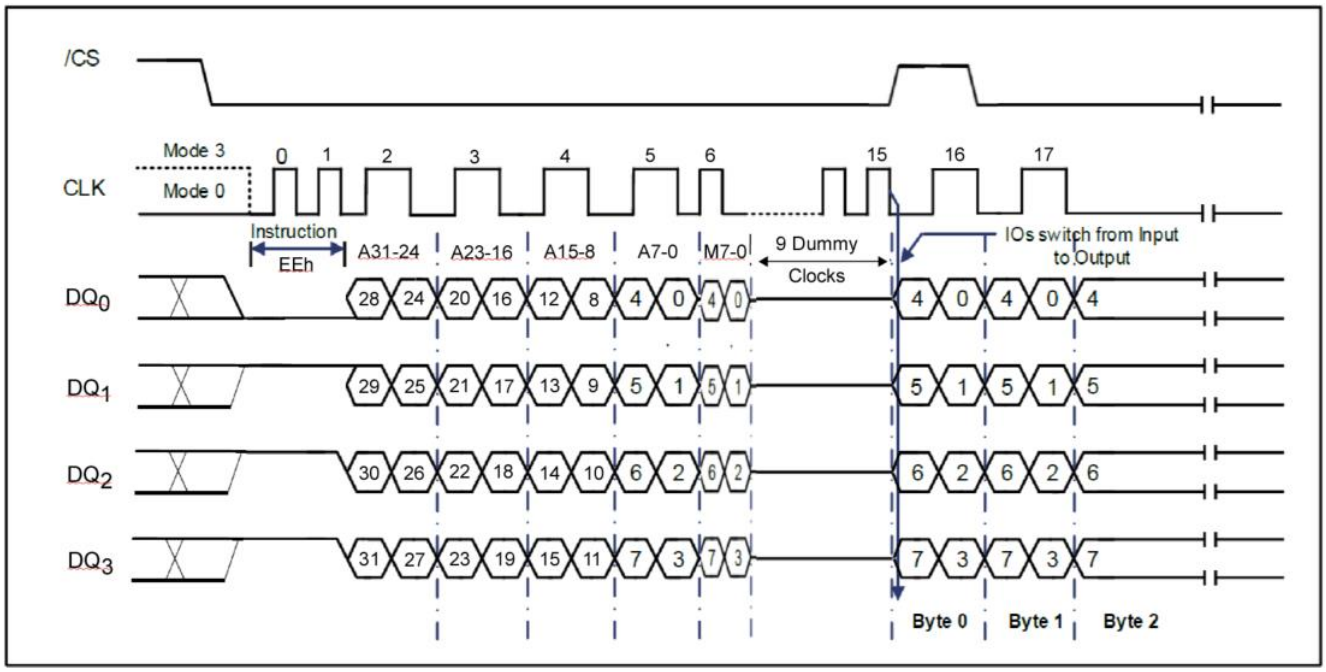
The DTR Fast Read Quad I/O with 4-byte address (EEh) instruction enable Double Data Rate throughput on quad I/O of Serial Flash in read mode. The address (interleave on 4 I/O pins) is latched on both rising and falling edge of CLK, and data (interleave on 4 I/O pins) shift out on both rising and falling edge on CLK at a maximum frequency F_R. The 8-bit address can be latched-in at one clock, and 8-bit data can be read out at one clock, which means four bits at rising edge of clock, the other four bits at falling edge of clock. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DTR Fast Read Quad I/O with 4-byte address (EEh) instruction. Once writing DTR Fast Read Quad I/O with 4-byte address (EEh) instruction, the following address/dummy/data out will perform as 8-bit instead of previous 1-bit.
The sequence of issuing DTR Fast Read Quad I/O with 4-byte address (EEh) instruction is: CS# goes low -> sending DTR Fast Read Quad I/O with 4-byte address (EEh) instruction (1-bit per clock) -> 32-bit address interleave on DQ_3, DQ_2, DQ_1 and DQ_0 (8-bit per clock) -> 8 dummy byte (8 clocks) -> data out interleave on DQ_3, DQ_2, DQ_1 and DQ_0 (8-bit per clock) -> to end DTR Fast Read Quad I/O with 4-byte address (EEh) operation can use CS# to high at any time during data out.
The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.
This instruction is also supported at EQPI mode (38h).



Note:

1. This instruction is workable at 4-byte address mode.
2. Set dummy by SR3.3, SR3.4

DTR Fast Read Quad I/O with 4-byte address Instruction (SPI mode)



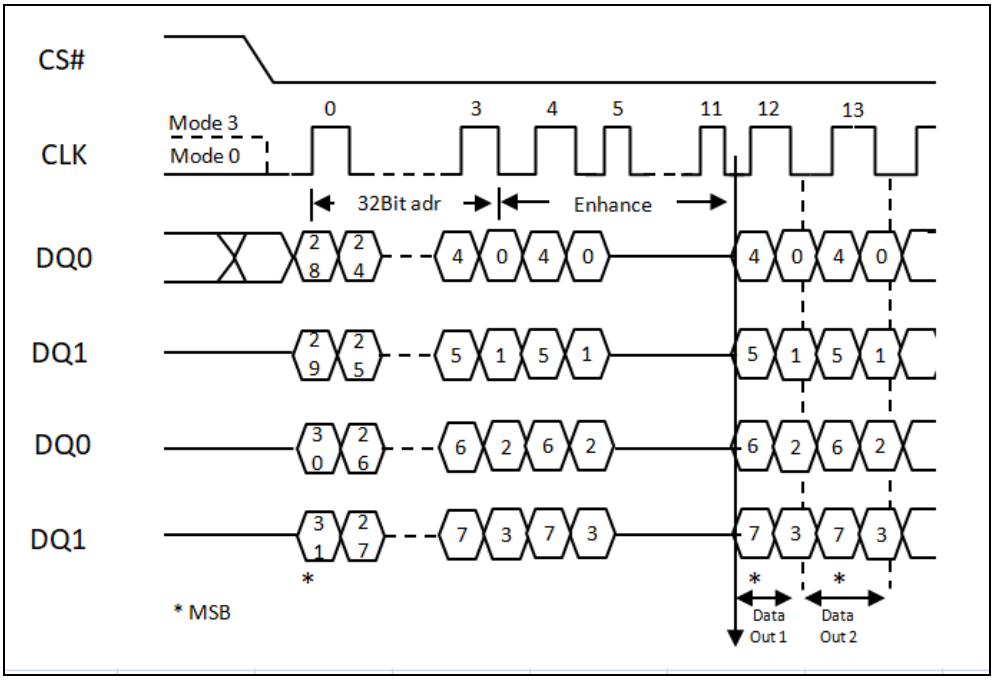
Note.

1. This instruction is workable at 4-byte address mode.
2. The dummy clock can be set by Set Parameter (C0h)

DTR Fast Read Quad I/O with 4-byte address Instruction (QPI mode)

Another sequence of issuing enhanced mode of DTR Fast Read Quad I/O with 4-byte address (EEh) instruction especially useful in random access is: CS# goes low -> sending DTR Fast Read Quad I/O with 4-byte address (EEh) instruction (1-bit per clock) -> 32-bit address interleave on DQ_3, DQ_2, DQ_1 and DQ_0 (8-bit per clock) -> one performance enhance byte, P[5:4]=(1,0) -> 7 dummy byte (7 clocks) -> data out (8-bit per clock) still CS# goes high -> CS# goes low (eliminate DTR Fast Read Quad I/O with 4-byte address) -> 32-bit random access address.
In the performance – enhancing mode, P[5:4] must be equals to (1,0) and make this mode continue and reduce the next DTR Fast Read Quad I/O with 4-byte address (EEh) instruction. Once P[5:4] is no longer equals to (1, 0). These commands will reset the performance enhance mode. And afterwards CS# is raised or issuing FFh/3FFh (CS# goes high -> CS# goes low -> sending FFh/3FFh (8 clock/10 clock) at DQ_0 -> CS# goes high) instead of P4=1, the system then will escape from performance enhance mode and return to normal operation.

While Program/ Erase/ Write Status Register cycle is in progress, DTR Fast Read Quad I/O with 4-byte address (EEh) instruction is rejected without any impact on the Program/ Erase/ Write Status Register current cycle.



Note:

1. This instruction is workable at 4-byte address mode.
2. The dummy clocks can be set by SR3.4, SR.3(SPI mode) or Set Parameter(C0h)(QPI mode)

DTR Fast Read Quad I/O with 4-byte address Instruction with enhance mode(SPI mode and QPI mode)

DTR Fast Read Quad I/O with 4-byte address with "8/16/32/64 byte Wrap Around"

The DTR Fast Read Quad I/O with 4-byte address command can be used to access a specific portion within a page by issuing "Set Burst with Wrap" (77h) commands prior to EEh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following EEh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.
The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The "Set Burst with Wrap" command allows three "Wrap Bits" W6-W4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-W5 is used to specify the length of the wrap around section within a page.

"Wrap Around" feature is not available in QPI mode for DTR Fast Read Quad I/O with 4-byte address instruction. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated "Burst Read with Wrap" (0Ch) instruction must be used.

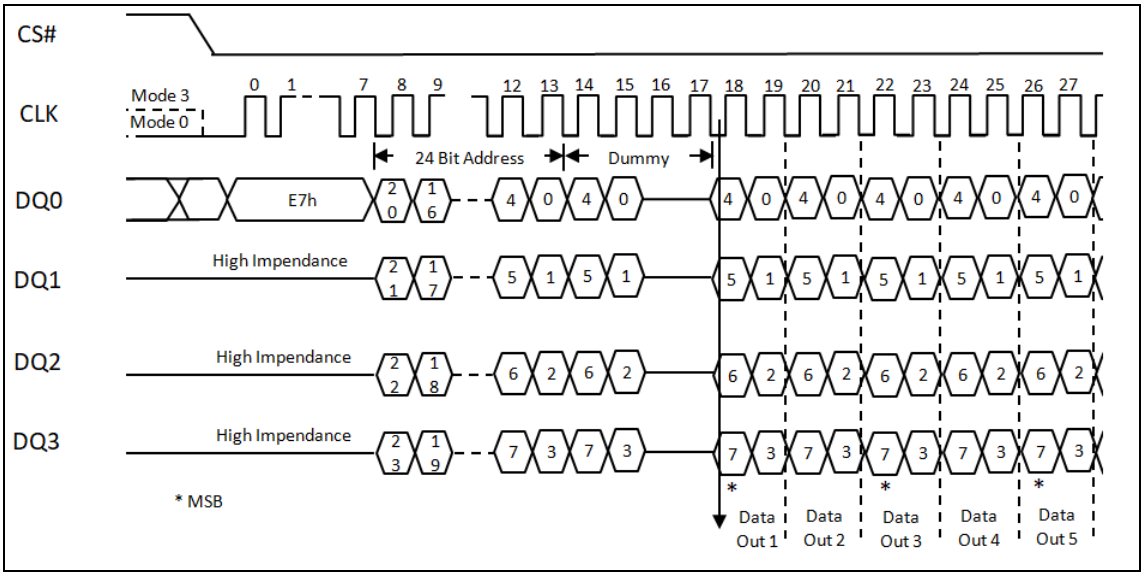
In QPI mode, the "Wrap Around" feature is not available for DTR Fast Read Quad I/O with 4-byte address instruction. To perform a wrap-around read operation with a fixed data length in QPI mode, a dedicated "DTR Burst Read with Wrap" (0Eh) instruction must be adopted.

Word Read Quad I/O (E7h)

The Word Quad I/O (E7h) instruction is similar to the Fast Read Qual I/O (EBh) instruction except that **LSB address A0=0** and four dummy clocks are required prior to the data output. The Word Quad I/O (E7h) instruction enable quad throughput of Serial Flash in read mode. The address is latching on rising edge of CLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of CLK at a maximum frequency F_R. The first address can only be **A0=0**. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single Word Quad I/O instruction. Once writing Word Quad I/O instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing Word Quad I/O (E7h) instruction is: CS# goes low -> sending Quad I/O (E7h) instruction -> 24-bit address (or 32-bit address depends on address mode state) interleave on DQ_3, DQ_2, DQ_1 and DQ_0 -> **four dummy clocks** -> data out interleave on DQ_3, DQ_2, DQ_1 and DQ_0 -> to end Word Quad I/O (E7h) operation can use CS# to high at any time during data out.

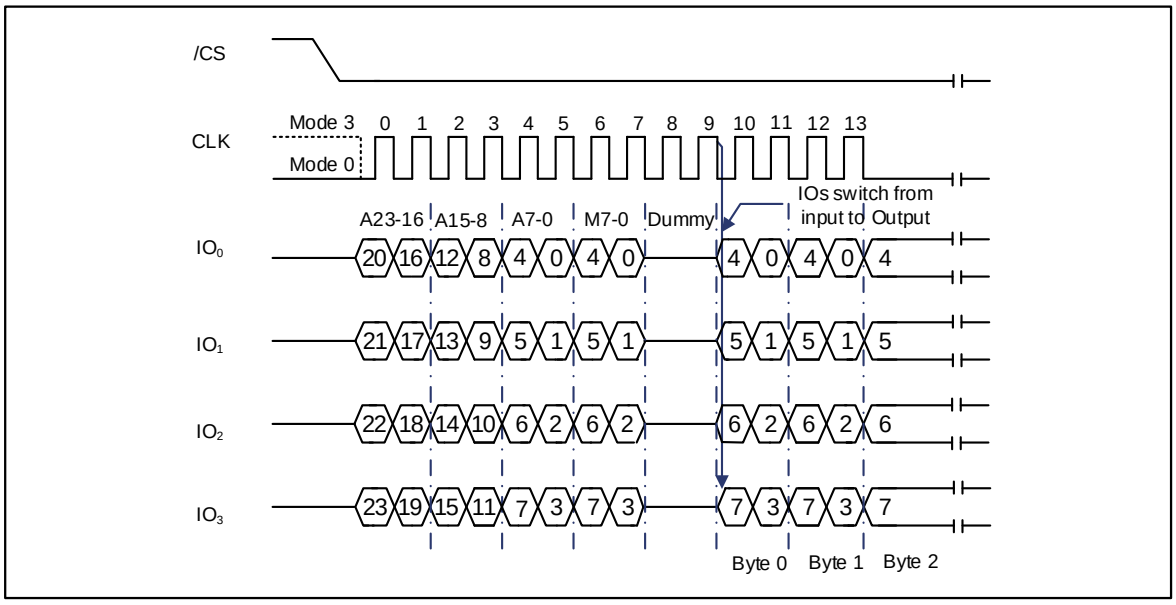
The Quad Enable bit (QE) of Status Register-2 must be set to enable the Word Read Quad I/O Instruction.



Note.

1. The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.
2. Set dummy clock by SR3.3, SR3.4

Word Read Quad I/O Instruction (Initial instruction or previous M5-4≠10, SPI Mode only)

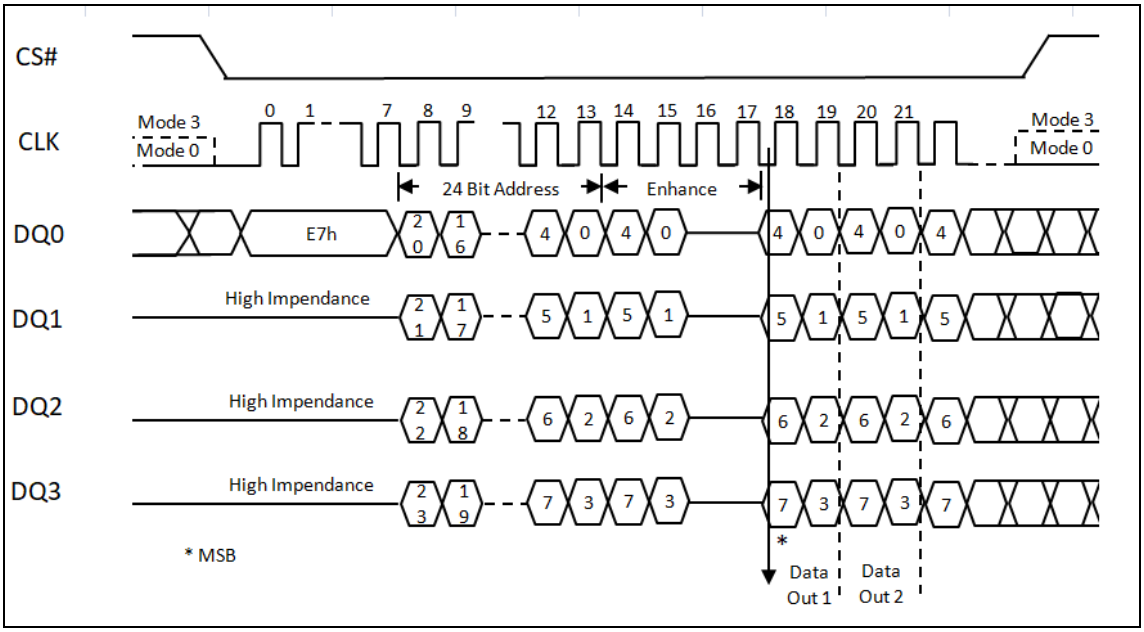


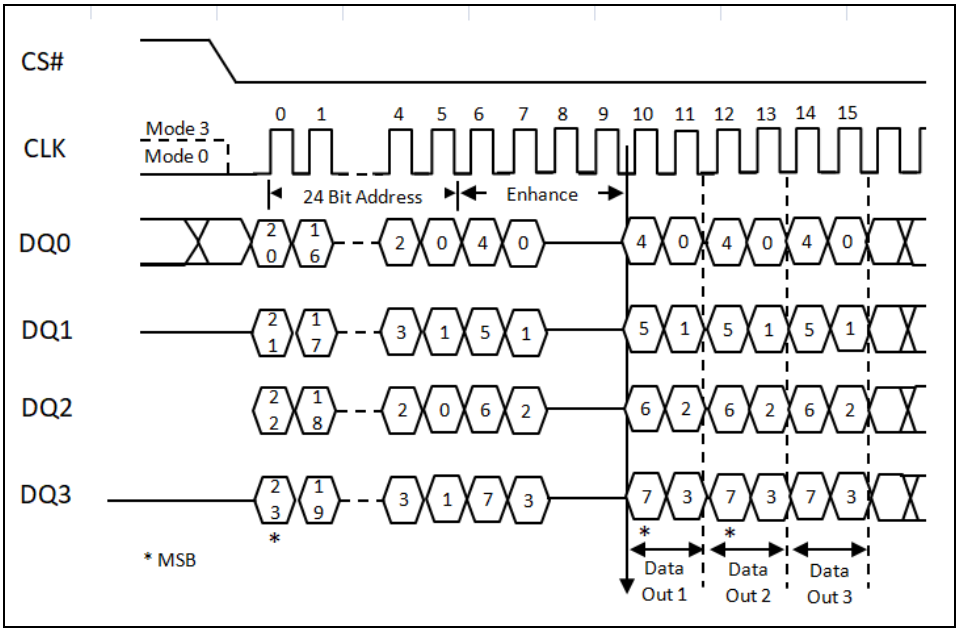
Word Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode only)

Another sequence of issuing Word Quad I/O (E7h) instruction especially useful in random access is: CS# goes low -> sending Word Quad I/O (E7h) instruction -> 24-bit address (or 32-bit address depends on address mode state) interleave on DQ_3, DQ_2, DQ_1 and DQ_0 ->one performance enhance byte, P[5:4]=10b -> two dummy clocks -> data out interleave on DQ_3, DQ_2, DQ_1 and DQ_0 till CS# goes high -> CS# goes low (reduce Word Quad I/O (E7h) instruction) -> 24-bit random access address (or 32-bit address depends on address mode state).

In the performance – enhancing mode, P[5:4]=10b, can make this mode continue and reduce the next Word Quad I/O (E7h) instruction. Once P[5:4] no longer equals to 10b. These commands will reset the performance enhance mode. And afterwards CS# is raised or issuing FFh command at DQ_0 (CS# goes high -> CS# goes low -> sending FFh at DQ_0-> CS# goes high) instead of P[4]=1, the system then will escape from performance enhance mode and return to normal operation.

While Program/ Erase/ Write Status Register is in progress, Word Quad I/O(E7h) instruction is rejected without impact on the Program/ Erase/ Write Status Register current cycle.





Note.

1. The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.
2. The dummy clock can be set by SR3.3, SR3.4

Word Quad I/O Instruction with performance enhance mode (SPI mode only)

Word Quad Input / Output Fast Read with "8/16/32/64 byte Wrap Around"

The Word Quad I/O command can be used to access a specific portion within a page by issuing "Set Burst with Wrap" (77h) commands prior to E7h. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following E7h commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The "Set Burst with Wrap" command allows three "Wrap Bits" W6-W4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-W5 is used to specify the length of the wrap around section within a page.

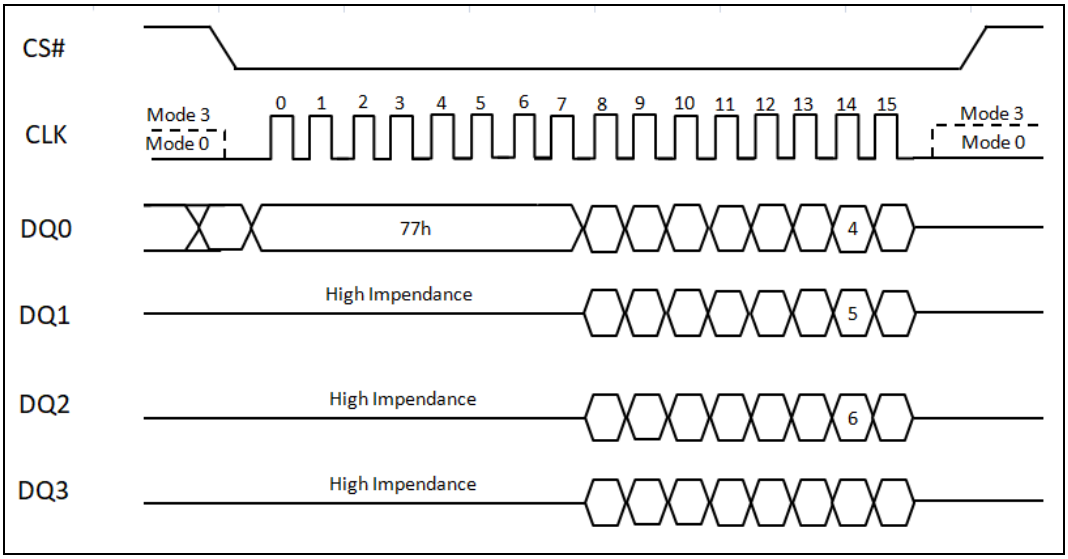
"Wrap Around" feature is not available in QPI mode for Word Quad I/O instruction. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated "Burst Read with Wrap" (0Ch) instruction must be used.

Set Burst with Wrap (77h)

This command only support SPI mode.
The Set Burst with Wrap command is used in conjunction with "Fast Read Quad I/O (EBh/E7h/EDh)" command to access a fixed length of 8/16/32/64-byte section within a 256-byte page, in standard SPI mode.
The Set Burst with Wrap command sequence: CS# goes low -> Send Set Burst with Wrap command (77h)-> 24 dummy bits (or 32dummy bits depends on address mode state) -> 8 bits "Wrap bits" ->CS# goes high.

W6, W5	W4=0		W4=1 (default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0, 0	Yes	8 byte	No	-
0, 1	Yes	16 byte	No	-
1, 0	Yes	32 byte	No	-
1, 1	Yes	64 byte	No	-

If the W6-W4 bits are set by the Set Burst with Wrap (77h) command, all the following "Quad I/O Fast Read (EBh/E7h/EDh)" command will use the W6-W4 setting to access the 8/16/32/64-byte section within any page. To exit the "Wrap Around" function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4=1. The default value of W4 is 1 at power on or after a software/hardware reset.



Note: The dummy clock counts will be increased according to address mode state

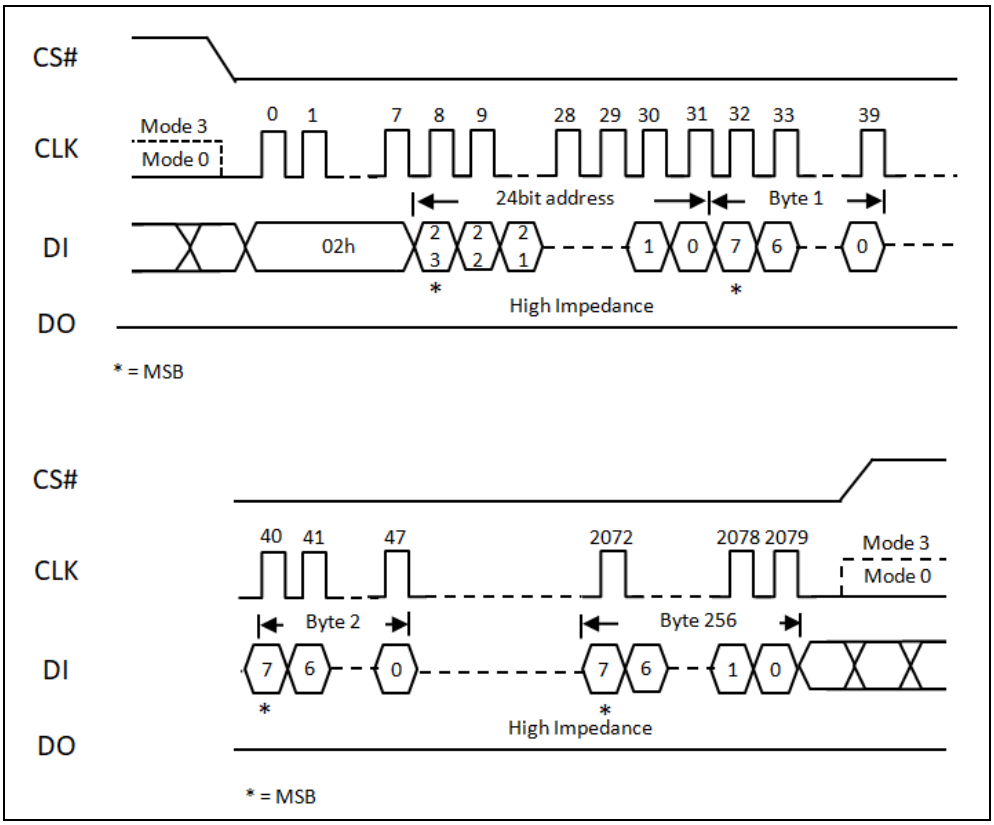
Set Burst with Wrap Instruction (SPI Mode only)

Page Program (02h)

The Page Program (PP) instruction allows bytes to be programmed in the memory. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).
The Page Program (PP) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, three address bytes (or four address bytes depends on address mode state) and at least one data byte on Serial Data Input (DI). If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). Chip Select (CS#) must be driven Low for the entire duration of the sequence.
If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 Data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

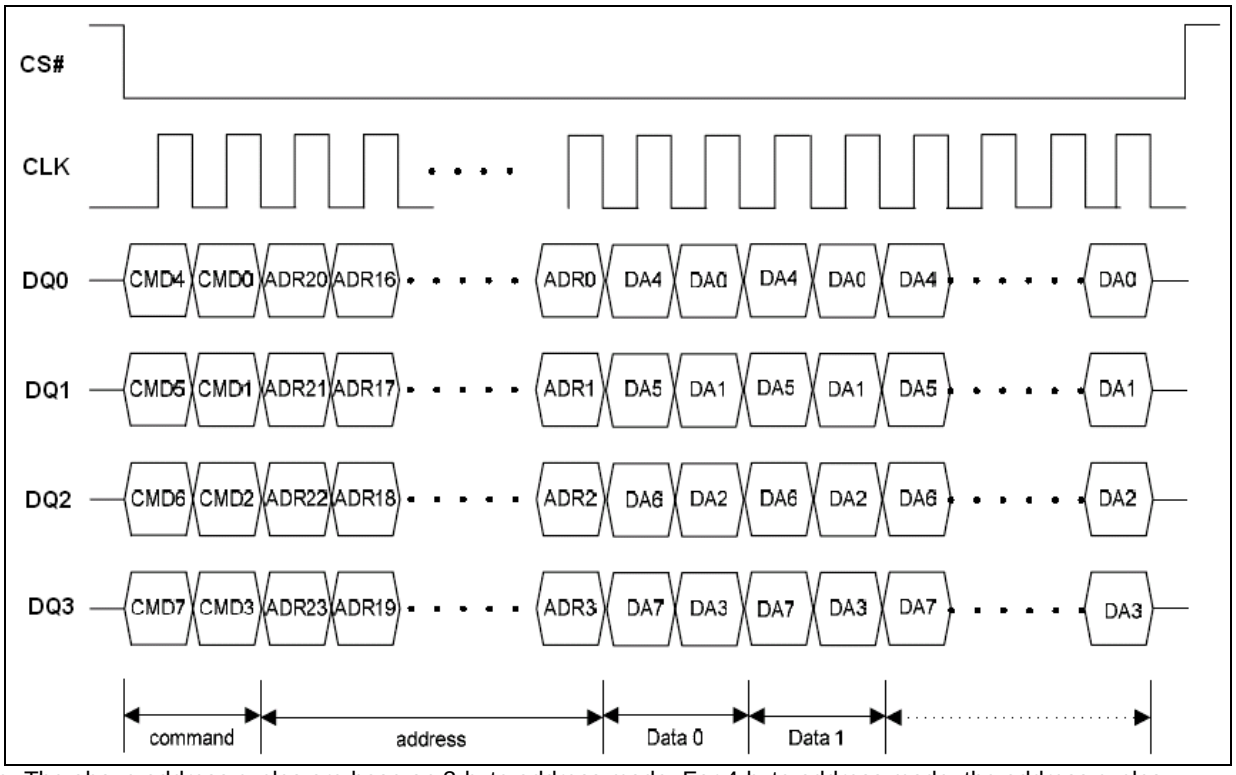
Chip Select (CS#) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Page Program (PP) instruction is not executed.
As soon as Chip Select (CS#) is driven high, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.
A Page Program (PP) instruction applied to a page which is protected by the Block Protect (CMP, BP4, BP3, BP2, BP1, BP0) bits is not executed.

The instruction is workable while using the Enter QPI mode (EQPI) (38h) command.



Note: The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Page Program Instruction (SPI Mode)

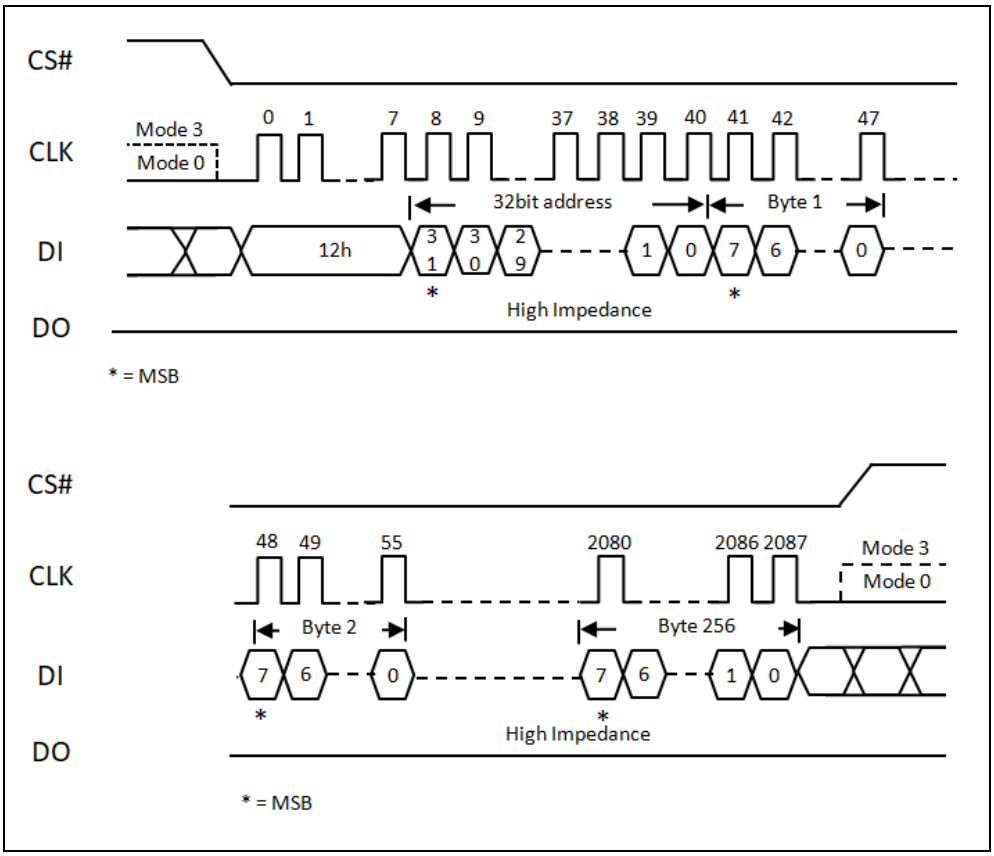


Note: The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Page Program Instruction (QPI Mode)

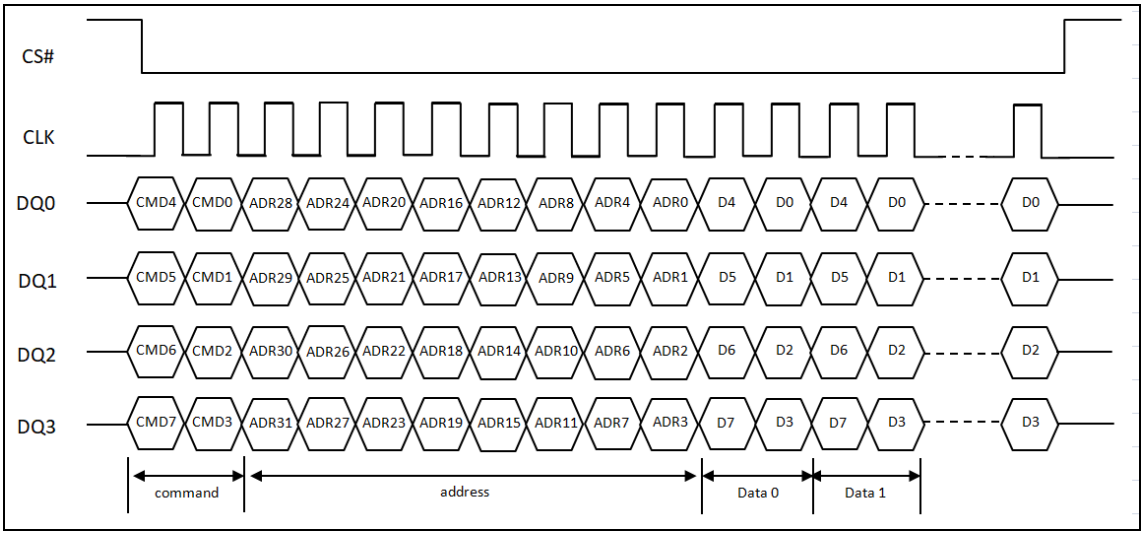
Page Program with 4-Byte Address (12h)

The Page Program with 4-byte address instruction allows bytes to be programmed in the memory. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).
The Page Program with 4-byte address instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, four address bytes and at least one data byte on Serial Data Input (DI). If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). Chip Select (CS#) must be driven Low for the entire duration of the sequence.
If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 Data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.
Chip Select (CS#) must be driven high after the eighth bit of the last data byte has been latched in, otherwise the Page Program with 4byte address instruction is not executed.
As soon as Chip Select (CS#) is driven high, the self-timed Page Program with 4-byte address cycle (whose duration is t_{PP}) is initiated. While the Page Program with 4-byte address cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Page Program with 4-byte address cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.
A Page Program with 4-byte address instruction applied to a page which is protected by the Block Protect (CMP, BP4, BP3, BP2, BP1, BP0) bits is not executed.
The instruction is workable while using the Enter QPI mode (EQPI) (38h) command.



Note: This instruction is workable while in 4byte address mode.

Page Program with 4-Byte Address (SPI Mode)



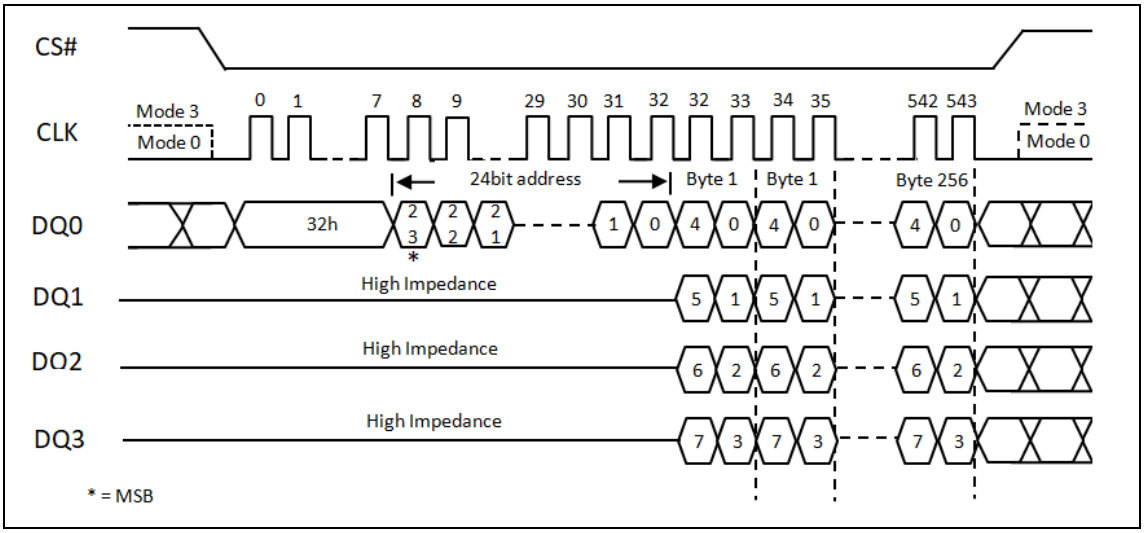
Note: This instruction is workable while in 4byte address mode.

Page Program with 4-Byte Address (QPI Mode)

Quad Input Page Program (32h)

The Quad Input Page Program (32h) instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: DQ_0, DQ_1, DQ_2 and DQ_3. The Quad Input Page Program can improve performance for PROM Programmer and applications that have slow clock speeds < 5MHz. Systems with faster clock speed will not realize much benefit for the Quad Input Page Program instruction since the inherent page program time is much greater than the time it take to clock- in the data. To access higher address (larger than 128Mb) in 3 byte address mode, user can issue Write Extended Register (C5h) operation before Quad Input Page Program (32h) or change to 4byte address mode before issue Quad Input Page Program command and use 4byte address input.

The Quad Enable (QE) bit in Status Register-2 must be set to 1 to use Quad Input Page Program. A Write Enable instruction must be executed before the device will accept the Quad Input Page Program instruction (SR.1, WEL=1). The instruction is initiated by driving the CS# pin low then shifting the instruction code “32h” followed by a 24-bit address (A23-A0) (or 32-bit address (A31-0), depends on address mode state) and at least one data byte, into the IO pins. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Input Page Program are identical to standard Page Program.

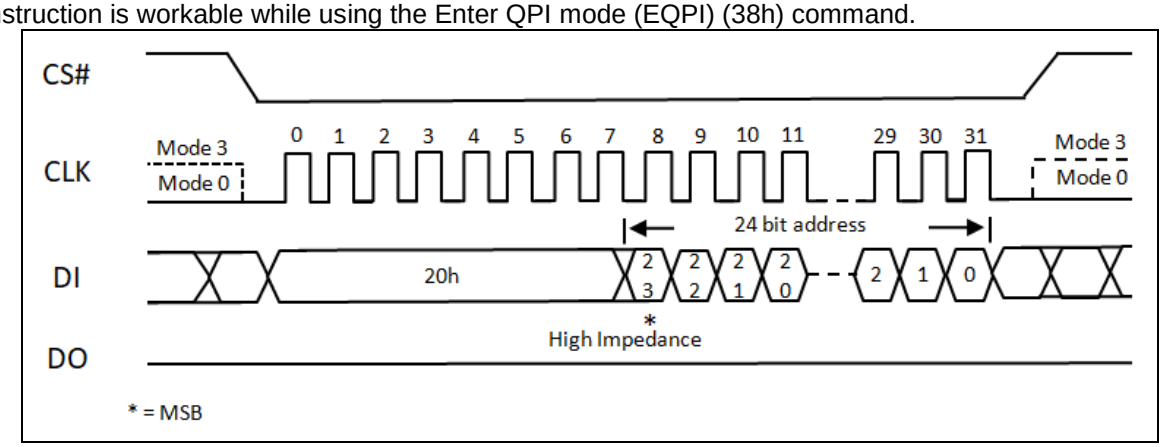


Note: The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Quad Input Page Program Instruction (SPI Mode only)

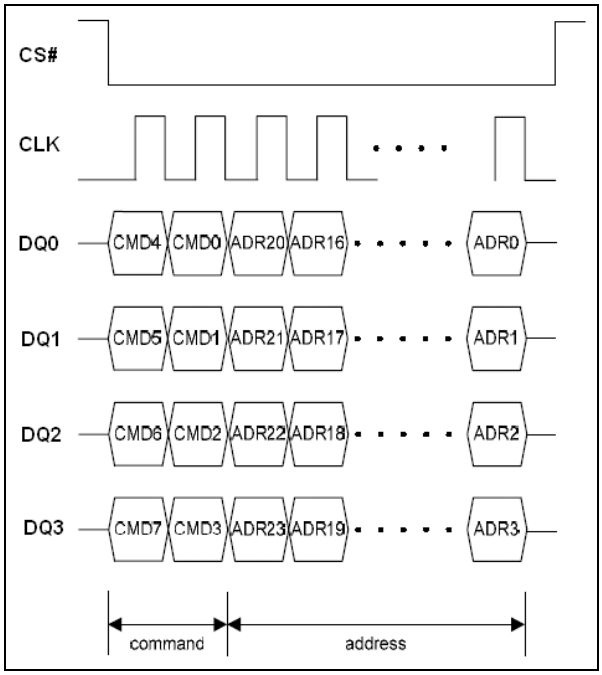
Sector Erase (20h)

The Sector Erase (SE) instruction sets to 1 (FFh) all bits inside the chosen sector. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).
The Sector Erase (SE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and three (or four depends on address mode state) address bytes on Serial Data Input (DI). Any address inside the Sector (see Uniform Block Sector Architecture table) is a valid address for the Sector Erase (SE) instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence. To access higher address (larger than 128Mb) in 3 byte address mode, user can issue Write Extended Register (C5h) operation before Sector Erase (20h).
Chip Select (CS#) must be driven high after the eighth bit of the last address byte has been latched in, otherwise the Sector Erase (SE) instruction is not executed. As soon as Chip Select (CS#) is driven high, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.
A Sector Erase (SE) instruction applied to a sector which is protected by the Block Protect (CMP, BP4, BP3, BP2, BP1, BP0) bits will be ignored.
The instruction is workable while using the Enter QPI mode (EQPI) (38h) command.



Note: The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Sector Erase Instruction (SPI Mode)

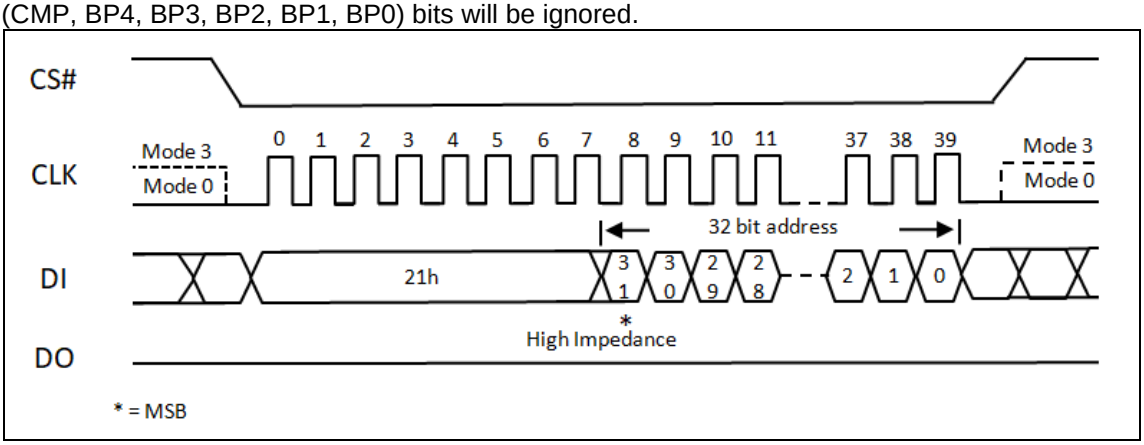


Note: The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Sector Erase Instruction (QPI Mode)

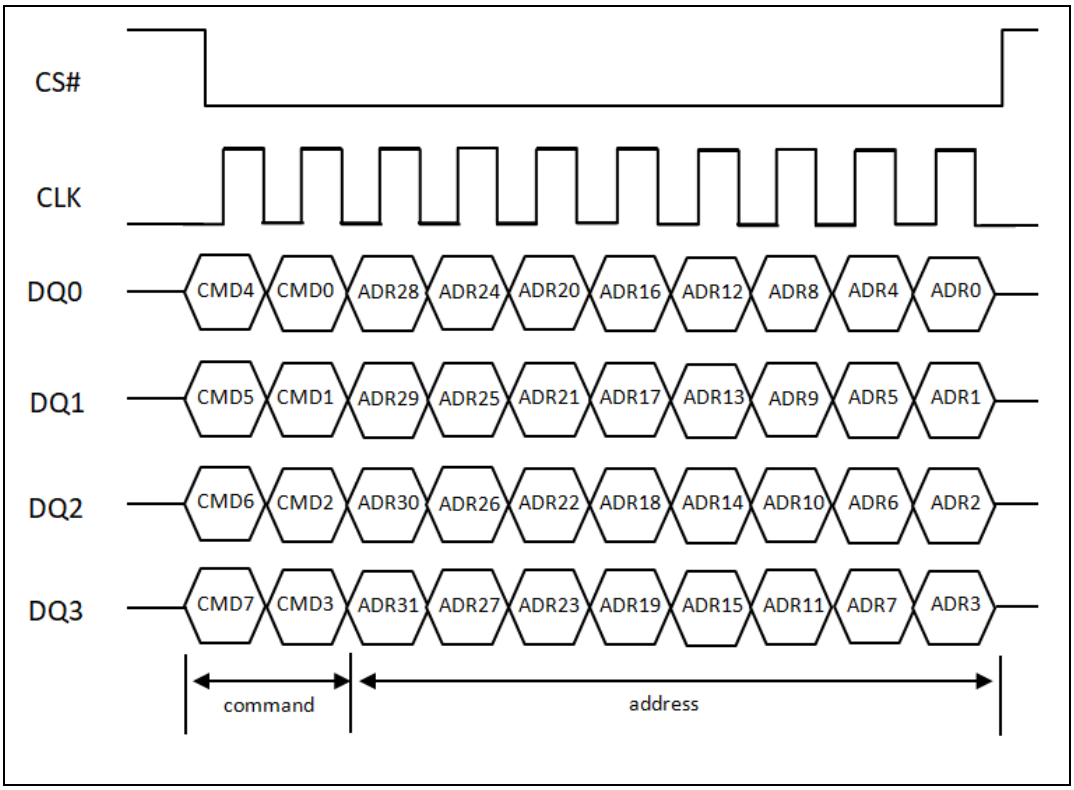
Sector Erase with 4-Byte Address (21h)

The Sector Erase with 4-byte address (21h) instruction sets to 1 (FFh) all bits inside the chosen sector. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).
The Sector Erase with 4-byte address instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and four address bytes on Serial Data Input (DI). Any address inside the Sector (see Uniform Block Sector Architecture table) is a valid address for the Sector Erase with 4-byte address instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence.
Chip Select (CS#) must be driven high after the eighth bit of the last address byte has been latched in, otherwise the Sector Erase with 4-byte address instruction is not executed. As soon as Chip Select (CS#) is driven high, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.
A Sector Erase with 4-byte address (SE4B) instruction applied to a sector which is protected by the Block Protect (CMP, BP4, BP3, BP2, BP1, BP0) bits will be ignored.



Note: This instruction is workable while in 4byte address mode.

Sector Erase with 4-Byte Address Instruction (SPI Mode)

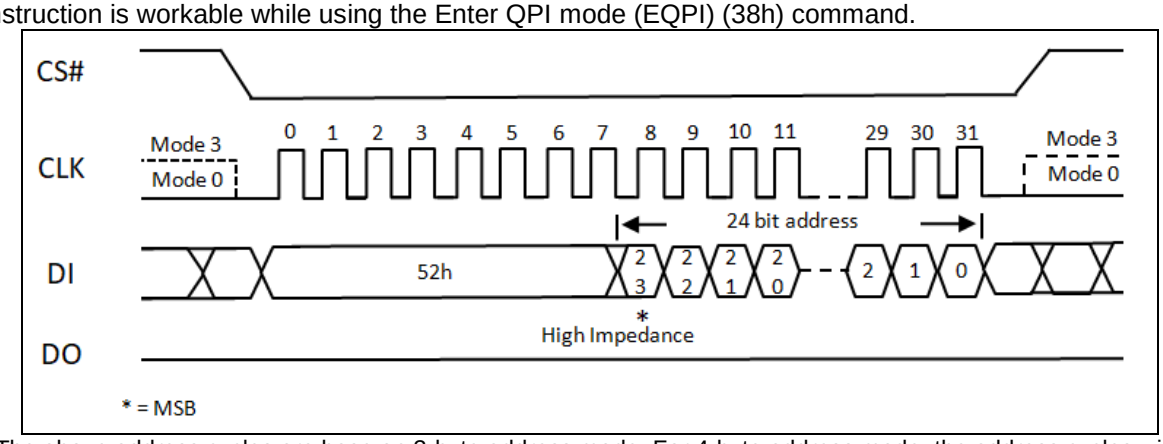


Note: This instruction is workable while in 4byte address mode.

Sector Erase with 4-Byte Address Instruction (QPI Mode)

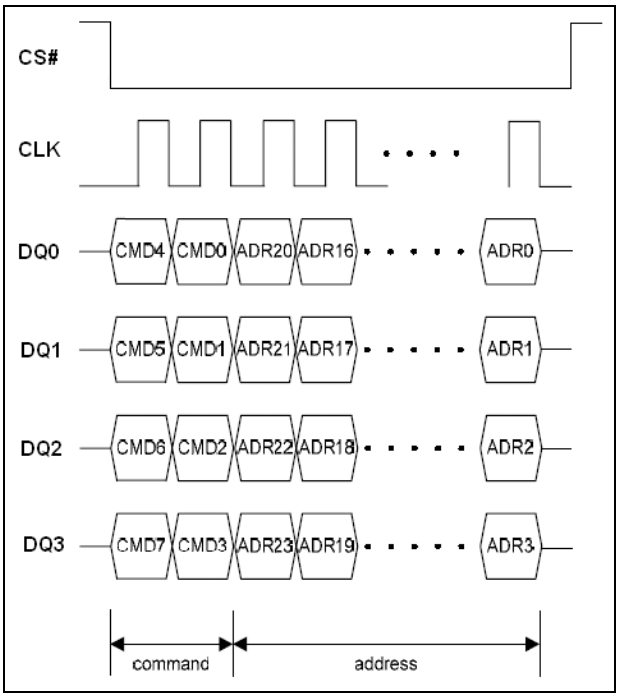
32KB Block Erase (52h)

The 32KB Block Erase (52h) instruction sets to 1 (FFh) all bits inside the chosen block. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).
The 32KB Block Erase instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and three (or four depends on address mode state) address bytes on Serial Data Input (DI). Any address inside the Block (see Uniform Block Sector Architecture table) is a valid address for the 32KB Block Erase instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence. To access higher address (larger than 128Mb) in 3 byte address mode, user can issue Write Extended Register (C5h) operation before 32KB Half Block Erase (52h).
The instruction sequence is shown in 32KB Half Block Erase Instruction Sequence Diagram figure. Chip Select (CS#) must be driven high after the eighth bit of the last address byte has been latched in, otherwise the 32KB Block Erase instruction is not executed. As soon as Chip Select (CS#) is driven high, the self-timed 32KB Block Erase cycle (whose duration is t_{HBE}) is initiated. While the 32KB Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed 32KB Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.
A 32KB Block Erase instruction applied to a block which is protected by the Block Protect (CMP, BP4, BP3, BP2, BP1, BP0) bits will be ignored.
The instruction is workable while using the Enter QPI mode (EQPI) (38h) command.



Note. The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

32KB Block Erase Instruction (SPI Mode)

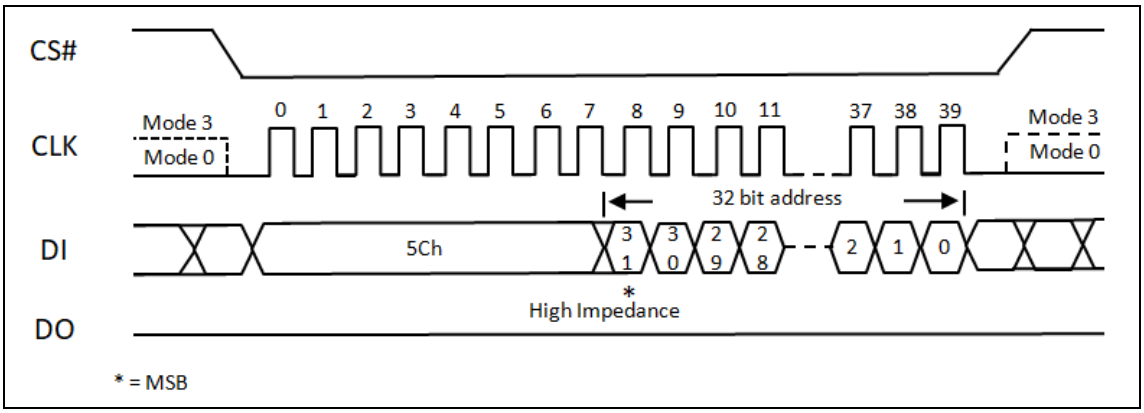


Note. The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

32KB Block Erase Instruction (QPI Mode)

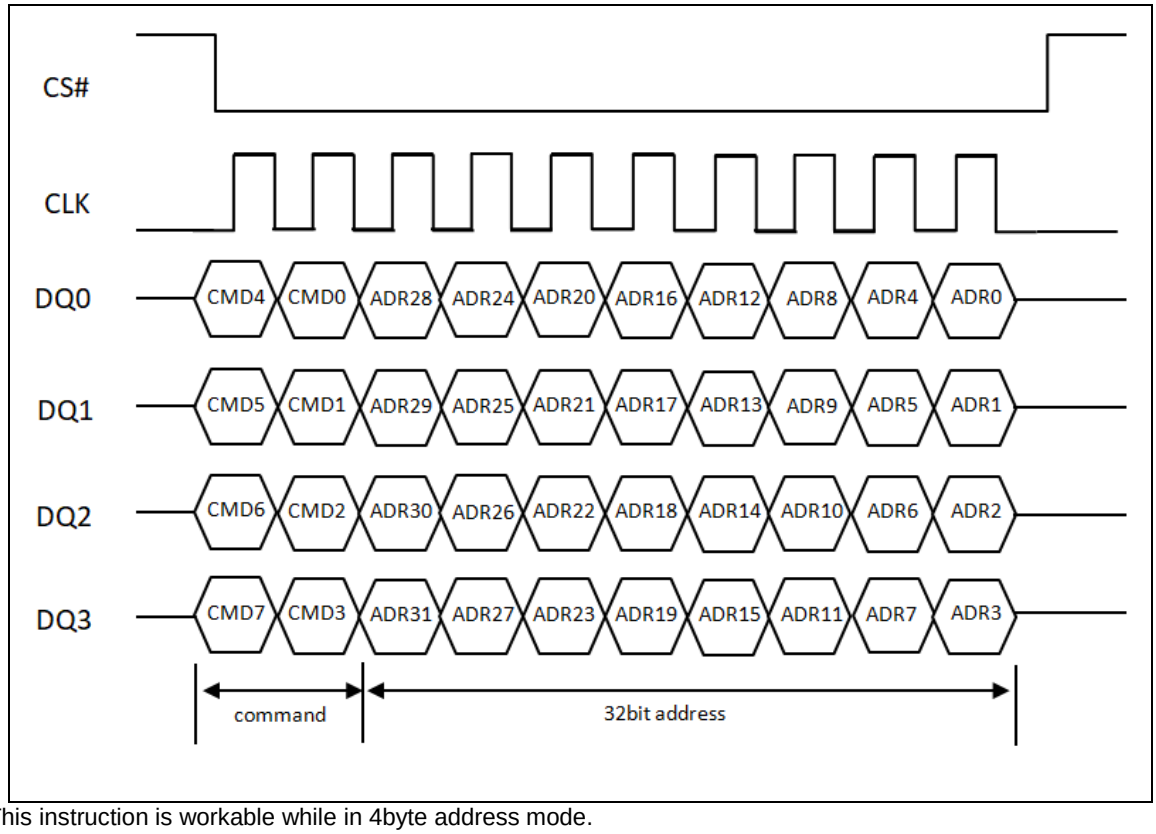
32KB Block Erase with 4-Byte Address (5Ch)

The 32KB Block Erase with 4-byte address instruction sets to 1 (FFh) all bits inside the chosen block. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).
The 32KB Block Erase with 4-byte address instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and four address bytes on Serial Data Input (DI). Any address inside the Block (see Uniform Block Sector Architecture table) is a valid address for the 32KB Block Erase with 4-byte address instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence.
Chip Select (CS#) must be driven high after the eighth bit of the last address byte has been latched in, otherwise the 32KB Block Erase with 4-byte address instruction is not executed. As soon as Chip Select (CS#) is driven high, the self-timed 32KB Block Erase cycle (whose duration is t_{HBE}) is initiated. While the 32KB Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed 32KB Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.
A 32KB Block Erase with 4-byte address instruction applied to a block which is protected by the Block Protect (CMP, BP4, BP3, BP2, BP1, BP0) bits will be ignored.
The instruction is workable while using the Enter QPI mode (EQPI) (38h) command.



Note: This instruction is workable while in 4byte address mode.

32KB Block Erase with 4-Byte Address Instruction (SPI Mode)

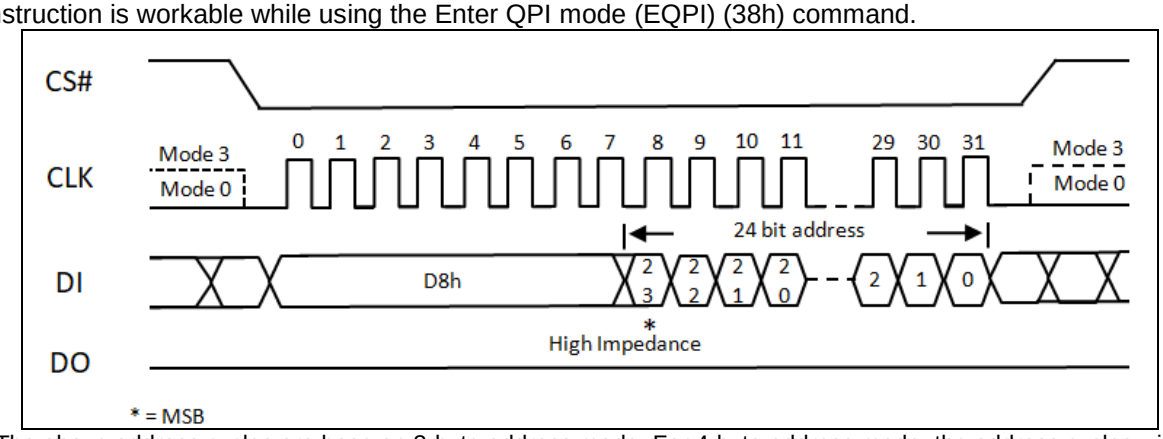


Note: This instruction is workable while in 4byte address mode.

32KB Block Erase with 4-Byte Address Instruction (QPI Mode)

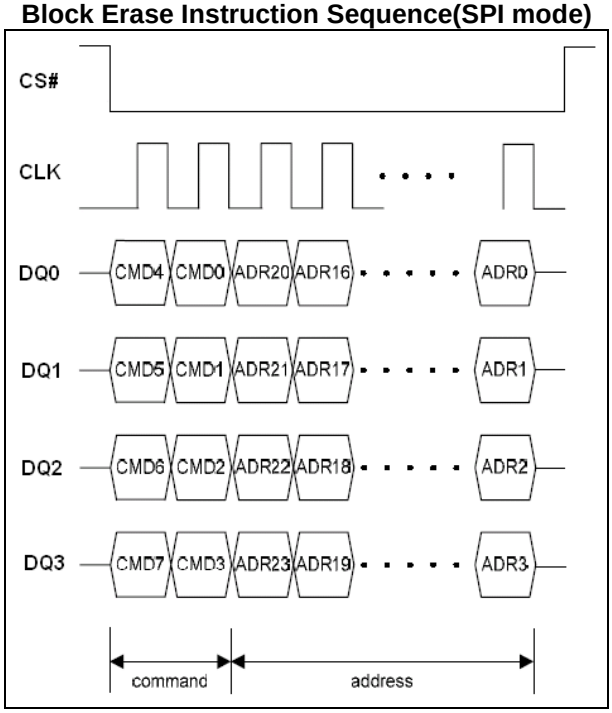
64KB Block Erase (D8h)

The 64KB Block Erase (BE) instruction sets to 1 (FFh) all bits inside the chosen block. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).
The 64KB Block Erase instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and three (or four depends on address mode state) address bytes on Serial Data Input (DI). Any address inside the Block (see Uniform Block Sector Architecture table) is a valid address for the 64KB Block Erase (BE) instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence. To access higher address (larger than 128Mb) in 3 byte address mode, user can issue Write Extended Register (C5h) operation before 64KB Block Erase.
Chip Select (CS#) must be driven high after the eighth bit of the last address byte has been latched in, otherwise the 64KB Block Erase instruction is not executed. As soon as Chip Select (CS#) is driven high, the self-timed Block Erase cycle (whose duration is t_{BE}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.
A 64KB Block Erase instruction applied to a block which is protected by the Block Protect (CMP, BP4, BP3, BP2, BP1, BP0) bits is not executed.
The instruction is workable while using the Enter QPI mode (EQPI) (38h) command.



Note. The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Block Erase Instruction Sequence(SPI mode)

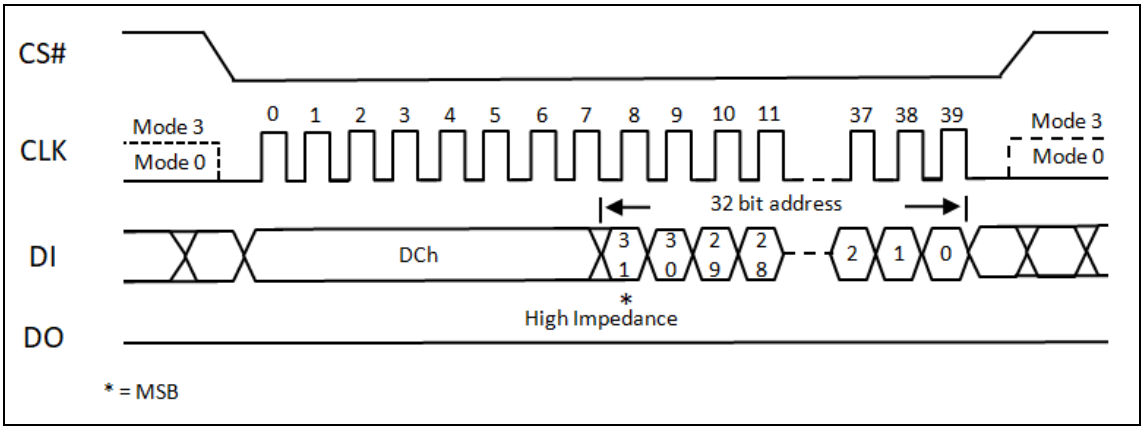


Note. The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

64KB Block Erase Instruction (QPI Mode)

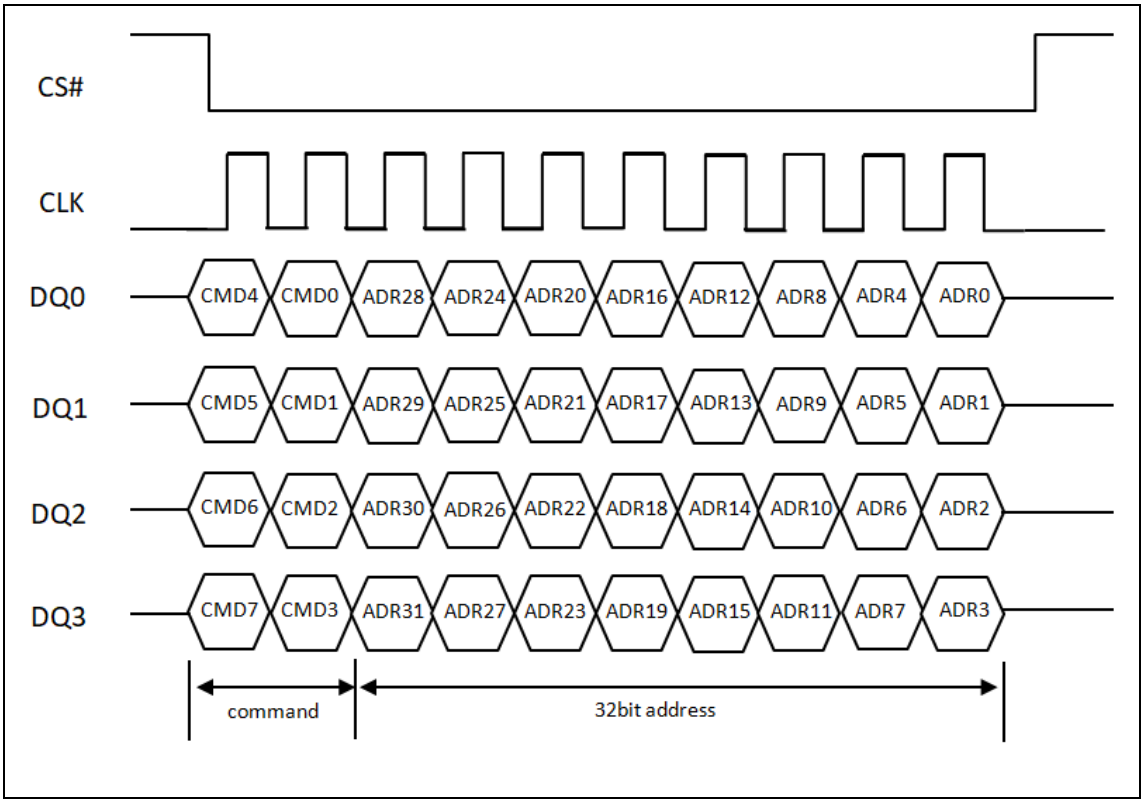
64KB Block Erase with 4-Byte Address (DCh)

The 64KB Block Erase with 4-byte address (DCh) instruction sets to 1 (FFh) all bits inside the chosen block. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).
The 64KB Block Erase with 4-byte address instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and four address bytes on Serial Data Input (DI). Any address inside the Block (see **Uniform Block Sector Architecture** table) is a valid address for the 64KB Block Erase with 4-byte address instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence.
Chip Select (CS#) must be driven high after the eighth bit of the last address byte has been latched in, otherwise the 64KB Block Erase with 4-byte address instruction is not executed. As soon as Chip Select (CS#) is driven high, the self-timed Block Erase cycle (whose duration is t_{BE}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.
A 64KB Block Erase with 4-byte address instruction applied to a block which is protected by the Block Protect (CMP, BP4, BP3, BP2, BP1, BP0) bits is not executed.
The instruction is workable while using the Enter QPI mode (EQPI) command.



Note: This instruction is workable while in 4byte address mode.

64KB Block Erase with 4-byte address Instruction (SPI Mode)

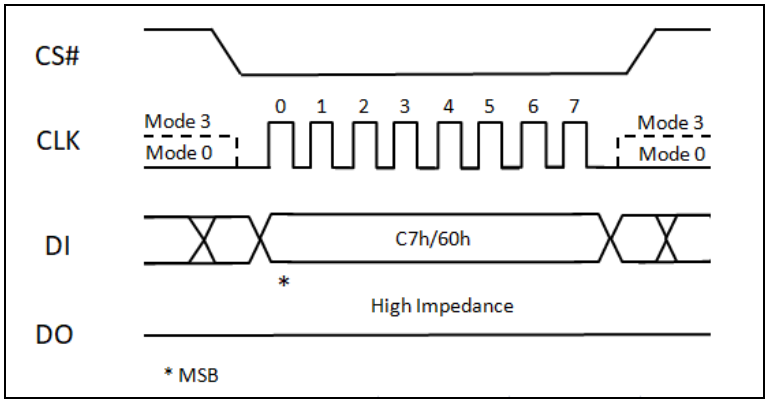


Note: This instruction is workable while in 4byte address mode.

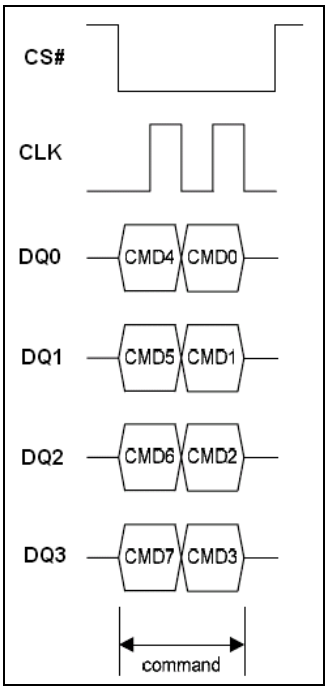
64KB Block Erase with 4-byte address Instruction (QPI Mode)

Chip Erase (C7h / 60h)

The Chip Erase (CE) instruction sets all bits to 1 (FFh). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).
The Chip Erase (CE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code on Serial Data Input (DI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.
Chip Select (CS#) must be driven high after the eighth bit of the instruction code has been latched in, otherwise the Chip Erase instruction is not executed. As soon as Chip Select (CS#) is driven high, the self-timed Chip Erase cycle (whose duration is t_{CE}) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.
The Chip Erase (CE) instruction is ignored if one or more blocks are protected.
The instruction is workable while using the Enter QPI mode (EQPI) command.



Chip Erase Instruction (SPI Mode)



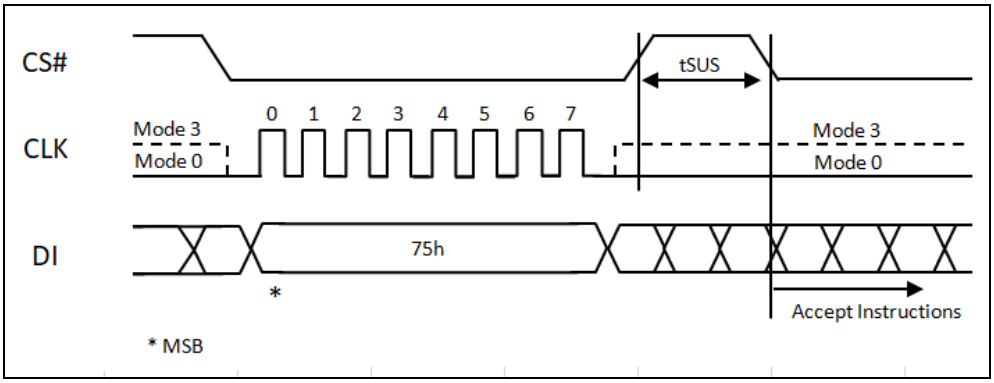
Chip Erase Instruction (QPI Mode)

Erase / Program Suspend (75h)

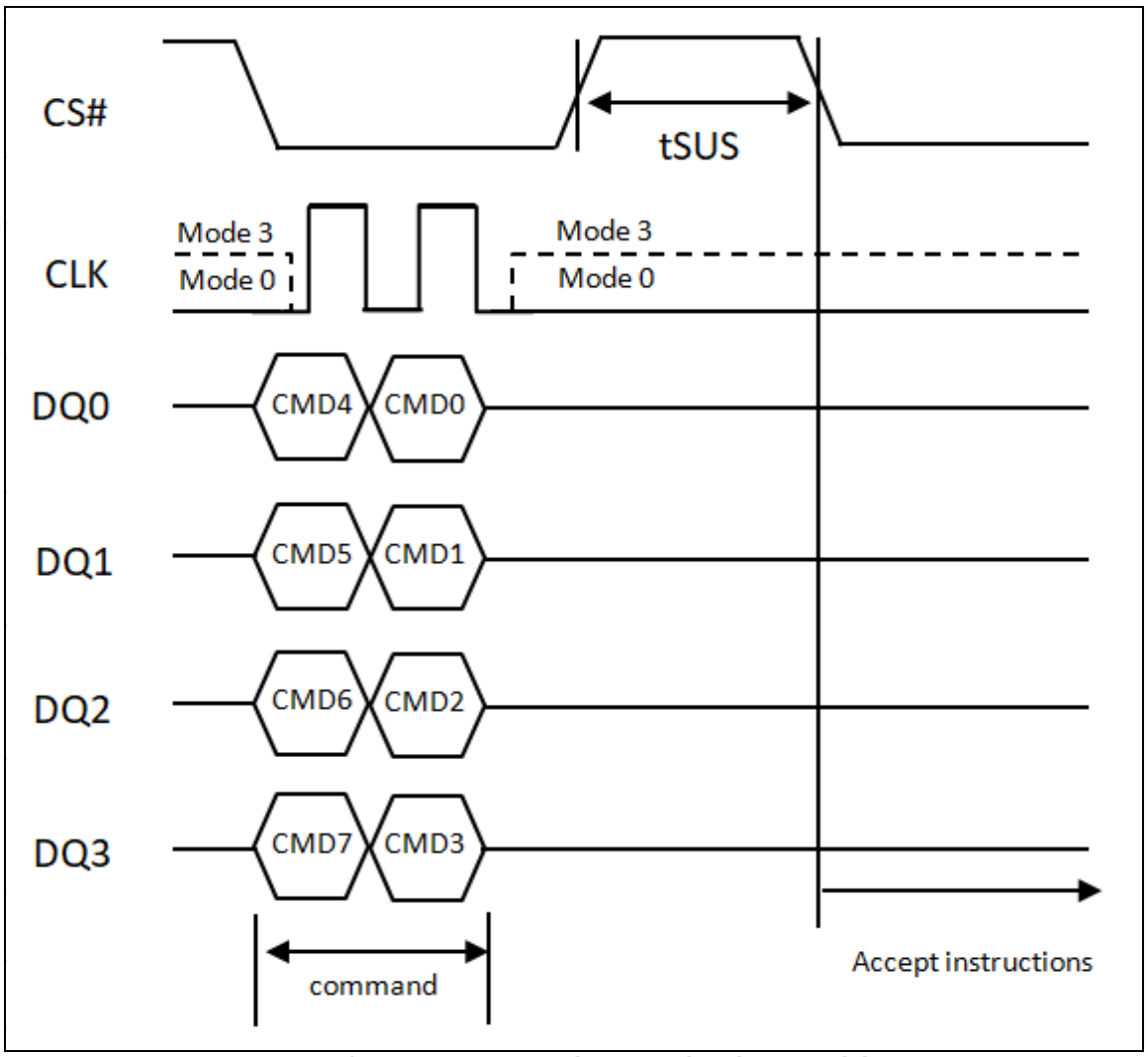
Erase/Program suspend allows the interruption of Sector Erase, Block Erase or Page Program operations in order to read data in another sector or block. The Write Status Register (01h) and erase Instructions (20h/21h/52h/5Ch/D8h/DCh/44h) are ignored while Erase Suspend. The Write status Register (01h/31h/11h), program (02h/12h/32h/42h) and erase (20h/21h/52h/5Ch/D8h/DCh/44h) instructions are ignored during Program Suspend. The original operation can be continued with Write Resume command.
The device will only accept the Erase/Program Suspend instruction "75h" if the SUS bit in the Status Register equals 0 and the WIP bit equals 1 while a Sector or Block Erase or Page Program operation is in progress. If the SUS bit is equal to 1 or the WIP bit is equal to 0, the Suspend instruction will be ignored by the device. A maximum time of "t_{SUS}" (as indicated by the Characteristics of AC) is required to suspend the Erase or Program operation. The WIP bit in the Status Register will be cleared from 1 to 0 within "t_{SUS}" and the SUS bit in the Status Register will be set from 0 to 1 immediately after Erase/Program Suspend. For a previously resumed Erase/Program operation, it is also required that the Suspend instruction "75h" can't be issued earlier than a minimum of time of "t_{SUS}" following the preceding Resume instruction "7Ah".

Unexpected power off during the Erase/Program suspend state will reset the device and release the suspend state. The SUS bit in the Status Register will also be reset to 0. Data within the page, sector or block being suspended may become corrupted. To prevent unexpected power interruptions and to maintain data integrity during Erase/Program Suspend state, system design techniques are advised to use.

Only one Erase/Program operation can be suspended at a time; if an operation is already suspended, the device will ignore the Erase/Program Suspend command. Erase/Program Suspend during Chip Erase is ignored; Chip Erase is not a valid command while a write is suspended.
The instruction is workable while using the Enter QPI mode (EQPI) command.



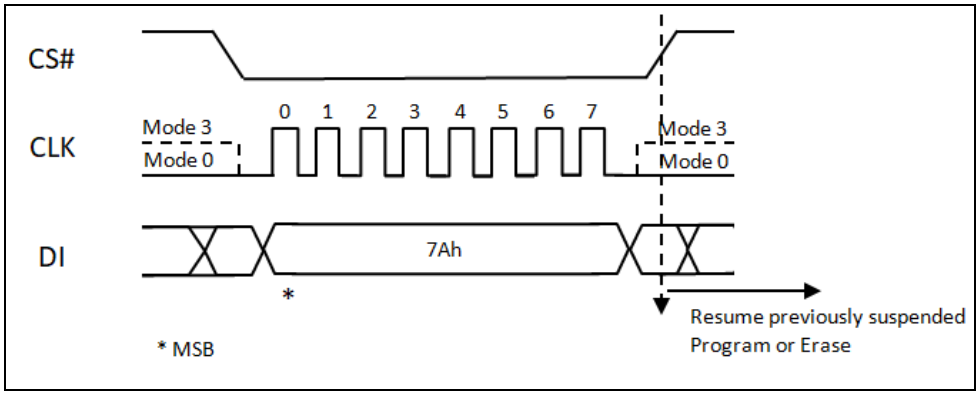
Erase/Program Suspend Instruction (SPI Mode)



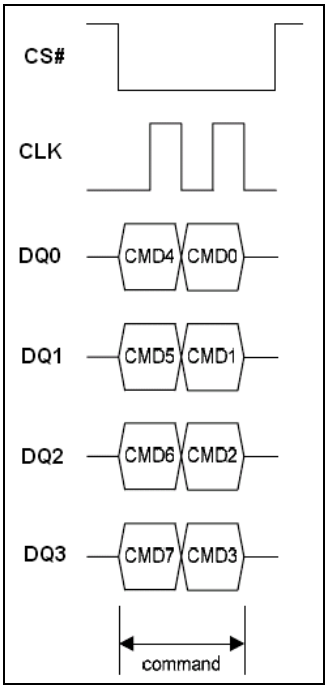
Erase/Program Suspend Instruction (QPI Mode)

Erase / Program Resume (7Ah)

Erase/Program Resume restarts Erase/Program command that was suspended, and changes the suspend status bit in the Status register 2 (SUS) back to “0”.
To execute an Erase/Program Resume operation, the host drives CS# low, sends the Erase/Program Resume command cycle (7Ah), then drives CS# high. A cycle is two nibbles long, most significant nibble first. To determine if the internal, self-timed Write operation completed, poll the WIP bit in the Status register. The total write time before suspend and after resume will not exceed the uninterrupted write times t_{SE}, t_{HBE}, t_{BE} or t_{PP}.
Resume to another suspend operation requires latency time of 200ns.
When the previous Erase/Program Suspend operation is interrupted by an unexpected power failure, the Resume instruction is ignored. It is also required that no subsequent Erase/Program Suspend instruction is issued within the minimum time of “t_{ERS}” after the previous Resume instruction.
The instruction is workable while using the Enter QPI mode (EQPI) (38h) command.



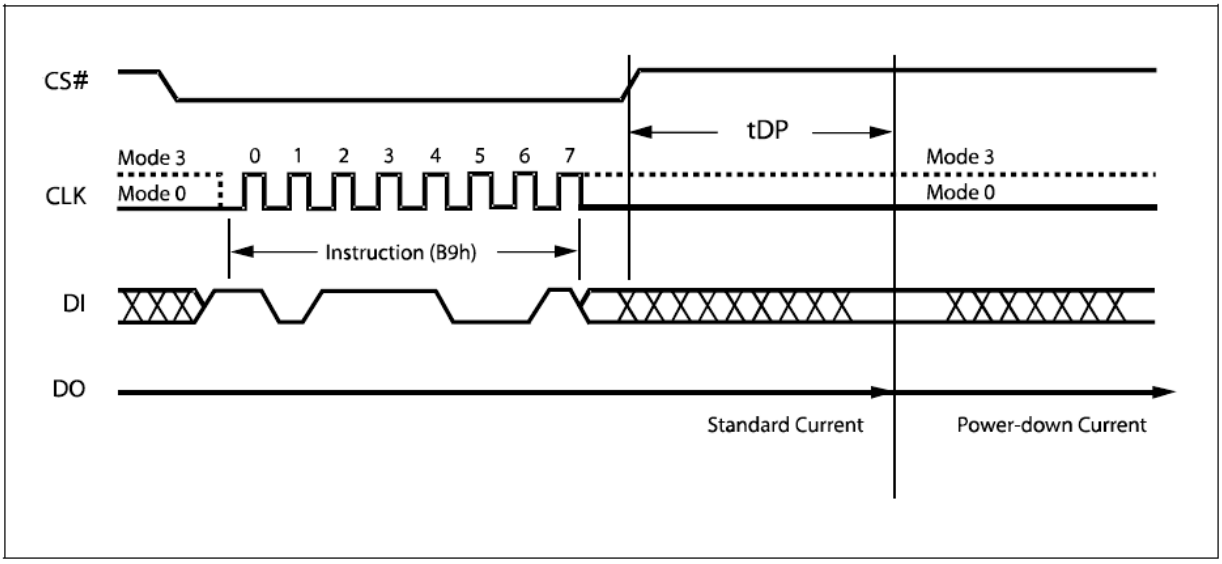
Erase/Program Resume Instruction (SPI Mode)



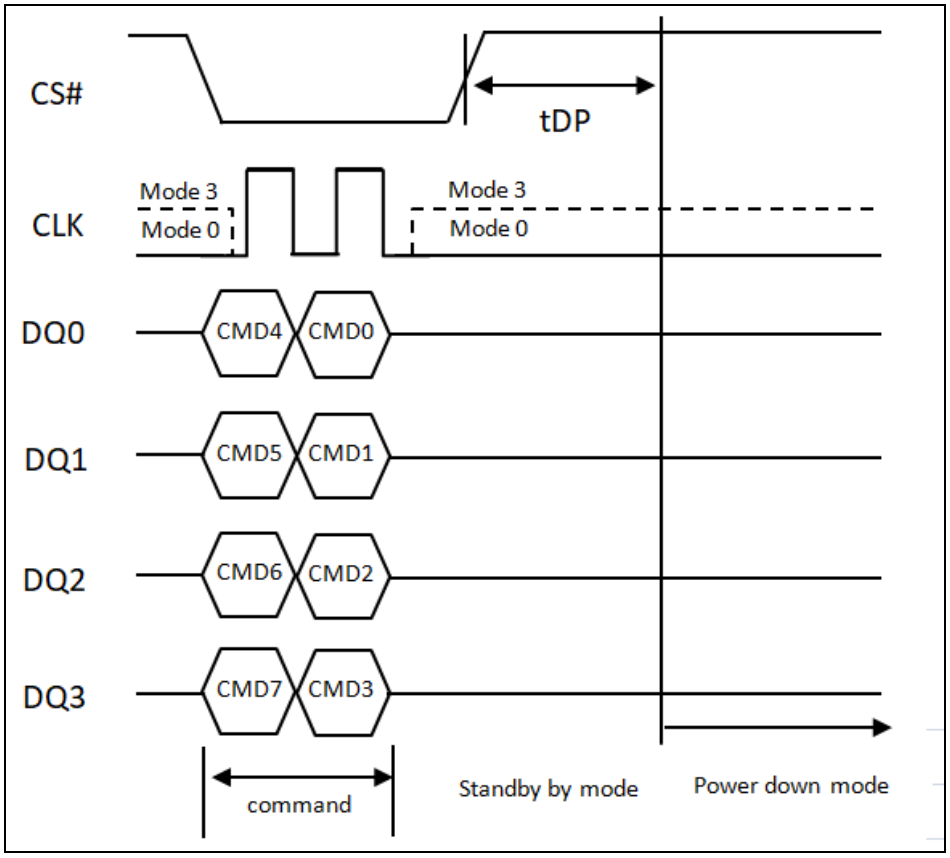
Erase/Program Resume Instruction (QPI Mode)

Power-down (B9h)

Executing the Power-down (B9h) instruction is the only way to put the device in the lowest consumption mode (the Deep Power-down mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Program and Erase instructions.
Driving Chip Select (CS#) high deselects the device, and puts the device in the Standby mode (if there is no internal cycle currently in progress). But this mode is not the Power-down mode. The Power-down mode can only be entered by executing the Power-down instruction, to reduce the standby current (from I_{CC1} to I_{CC2}, as specified in DC Characteristics table.)
Once the device has entered the Power-down mode, all instructions are ignored except the Release from Power-down, Read Device ID and Software Reset instruction which release the device from this mode. The Release from Power-down and Read Device ID (RDI) instruction also allows the Device ID of the device to be output on Serial Data Output (DO).
The Power-down mode automatically stops at Power-down, and the device always Powers-up in the Standby mode. The Power-down (DP) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code on Serial Data Input (DI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.
Chip Select (CS#) must be driven high after the eighth bit of the instruction code has been latched in, otherwise the Power-down instruction is not executed. As soon as Chip Select (CS#) is driven high, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the Power-down mode is entered.
Any Power-down instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.
The instruction is workable while using the Enter QPI mode (EQPI) (38h) command.



Deep Power-down Instruction (SPI Mode)



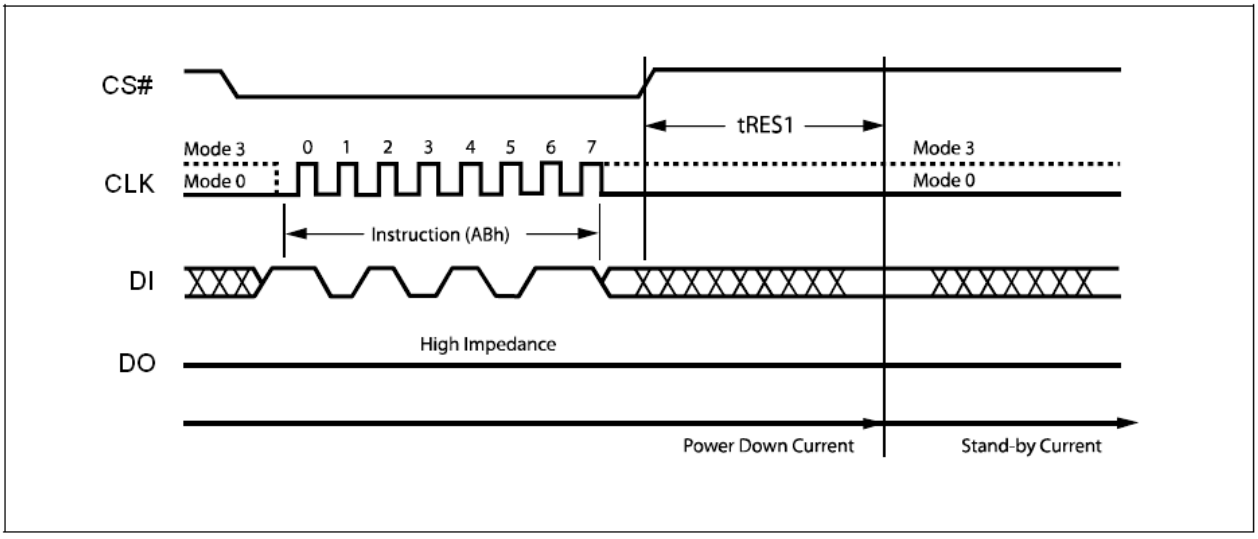
Deep Power-down Instruction (QPI Mode)

Release Power-down / Device ID (ABh)

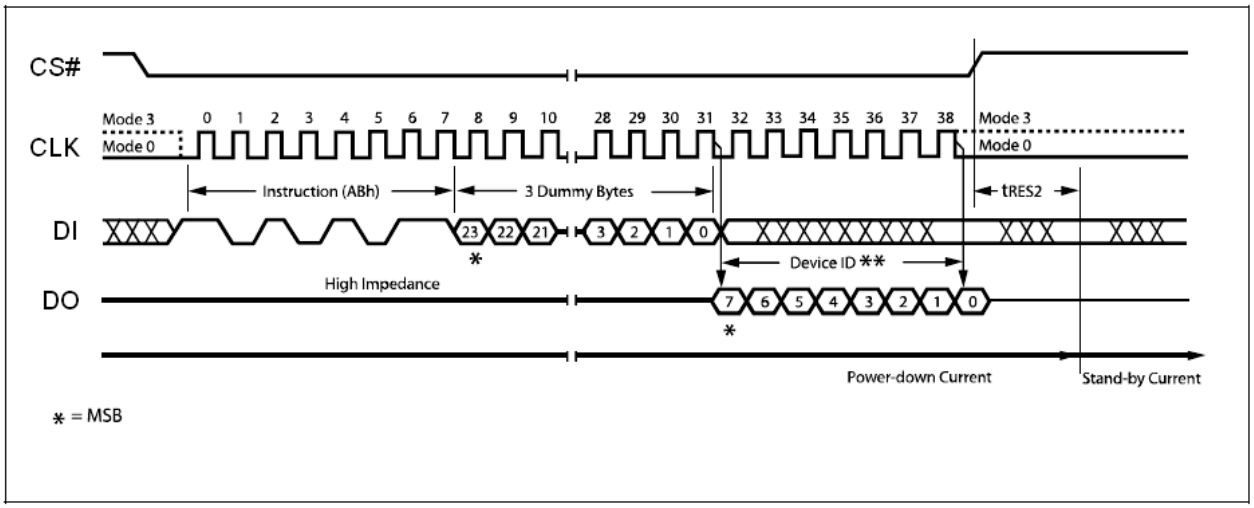
Once the device has entered the Power-down mode, all instructions are ignored except the Release from Power-down and Read Device ID instruction. Executing this instruction takes the device out of the Deep Power-down mode.
Please note that this is not the same as, or even a subset of, the JEDEC 16-bit Electronic Signature that is read by the Read Identifier (RDID) instruction. The old-style Electronic Signature is supported for reasons of backward compatibility, only, and should not be used for new designs. New designs should, instead, make use of the JEDEC 16-bit Electronic Signature, and the Read Identifier (RDID) instruction.

When used only to release the device from the power-down state, the instruction is issued by driving the CS# pin low, shifting the instruction code “ABh” and driving CS# high. After the time duration of t_{RES1} (See AC Characteristics) the device will resume normal operation and other instructions will be accepted. The CS# pin must remain high during the t_{RES1} time duration.
When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the CS# pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Release Power-down / Device ID Instruction Sequence Diagram figure. The Device ID value for the DEVICE is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving CS# high.
When Chip Select (CS#) is driven high, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Standby Power mode is delayed by t_{RES2}, and Chip Select (CS#) must remain high for at least t_{RES2} (max), as specified in AC Characteristics table. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.
Except while an Erase, Program or Write Status Register cycle is in progress, the Release from Deep Power-down and Read Device ID (RDI) instruction always provides access to the 8bit Device ID of the device, and can be applied even if the Deep Power-down mode has not been entered.
Any Release from Deep Power-down and Read Device ID (RDI) instruction while an Erase, Program or Write Status Register cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

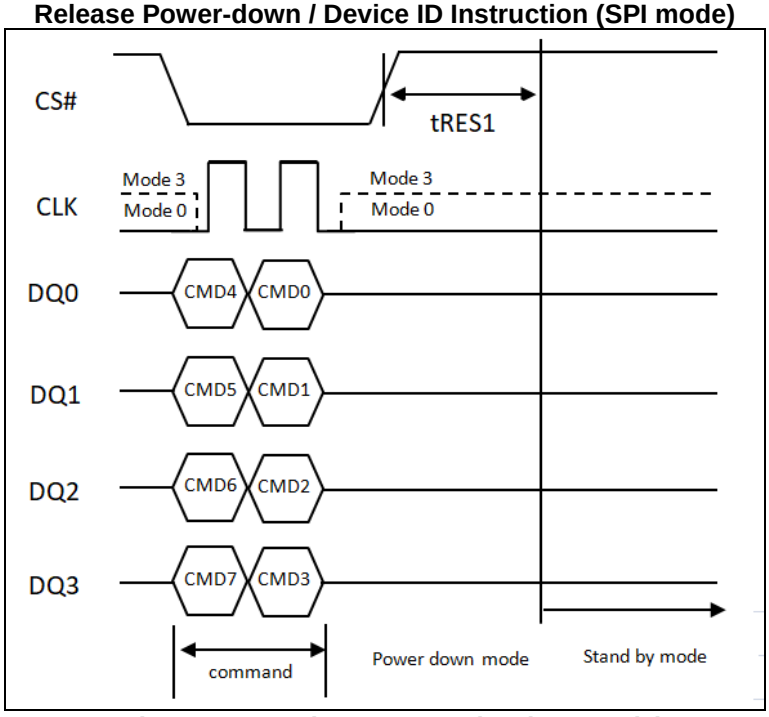
The instruction is workable while using the Enter QPI mode (EQPI) (38h) command.



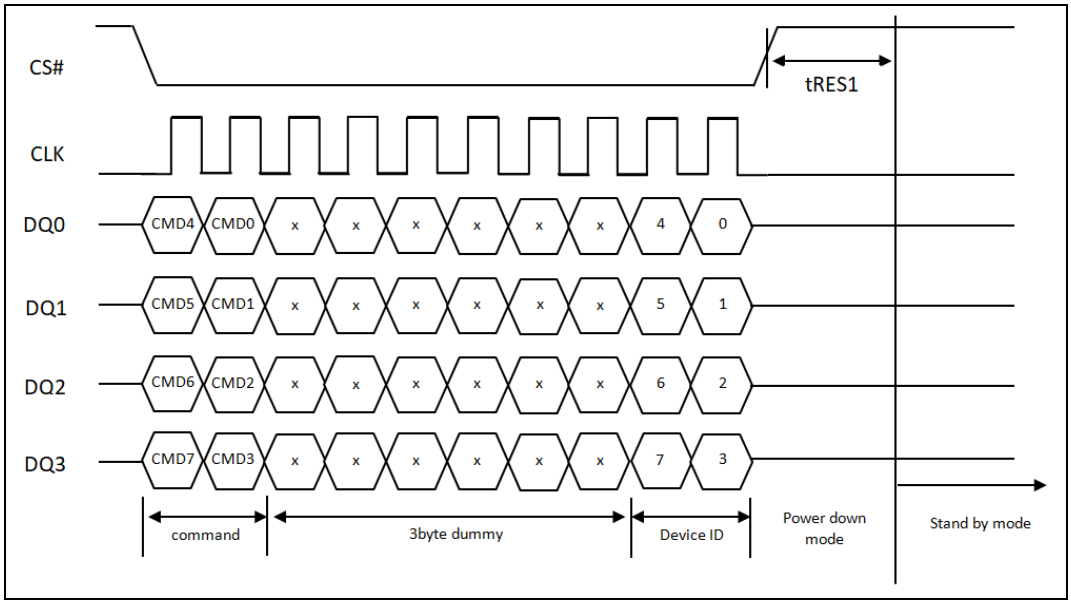
Release Power-down Instruction (SPI mode)



Release Power-down / Device ID Instruction (SPI mode)



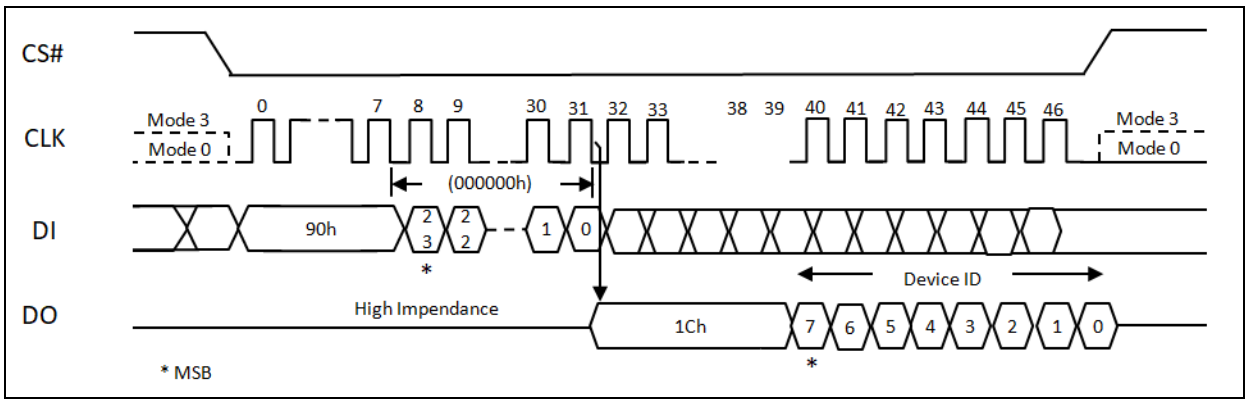
Release Power-down Instruction (QPI Mode)



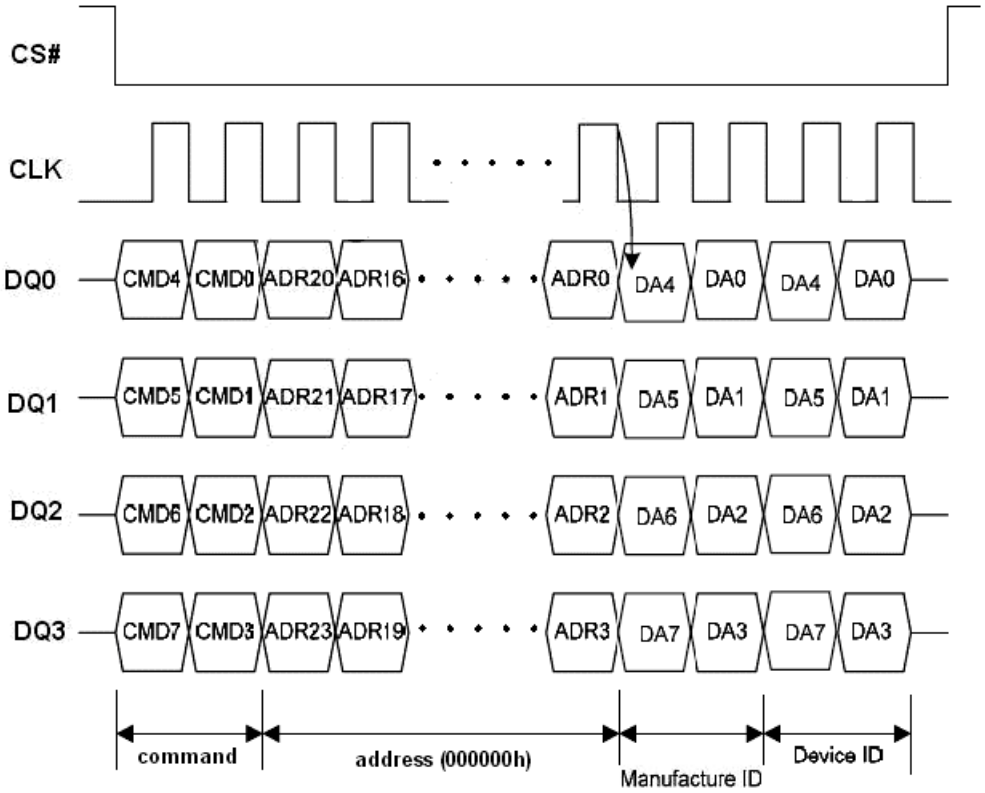
Release Power-down / Device ID Instruction (QPI Mode)

Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.
The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code “90h” followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Read Manufacturer / Device ID Diagram figure.
The Device ID values for the DEVICE are listed in Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first
The instruction sequence is shown in Read Manufacturer / Device ID Diagram in QPI Mode figure while using the Enter QPI mode (38h) command.



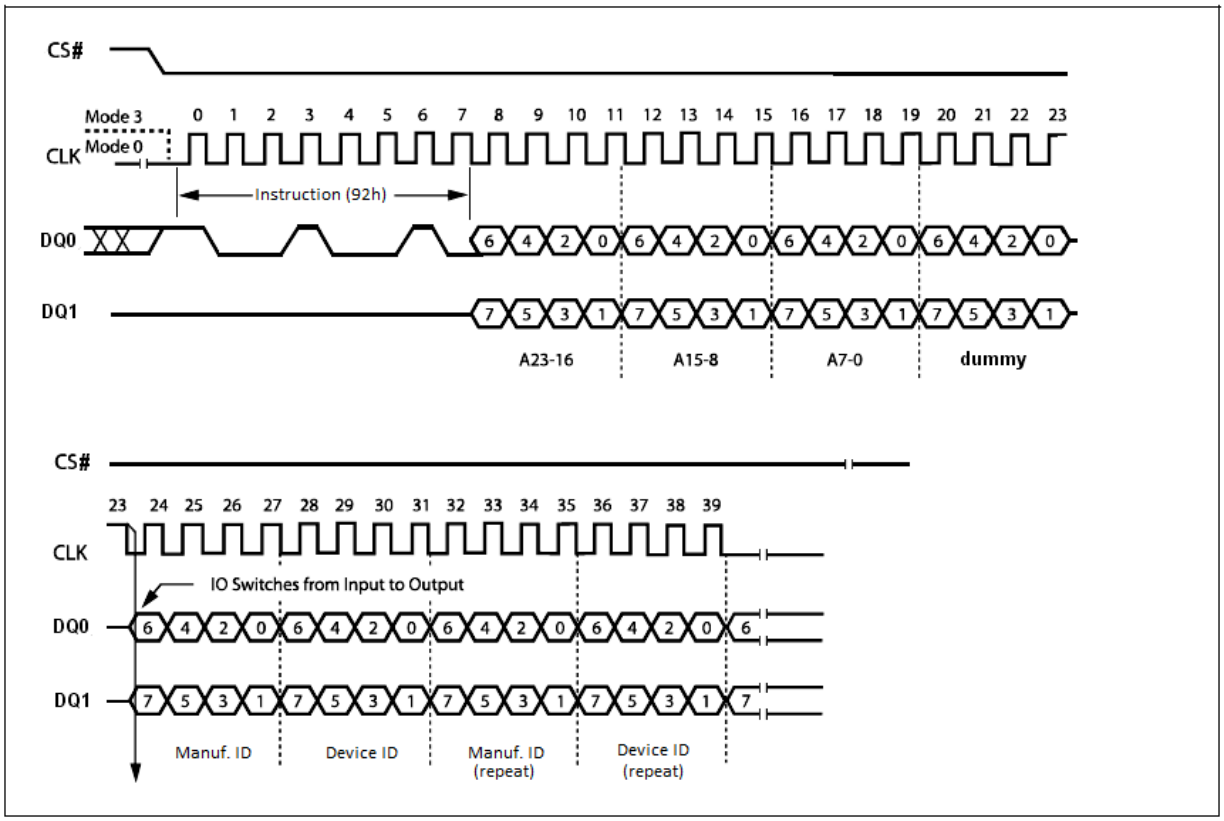
Read Manufacturer / Device ID Instruction (SPI mode)



Read Manufacturer / Device ID Instruction (in QPI mode)

Read Manufacturer / Device ID Dual I/O (92h)

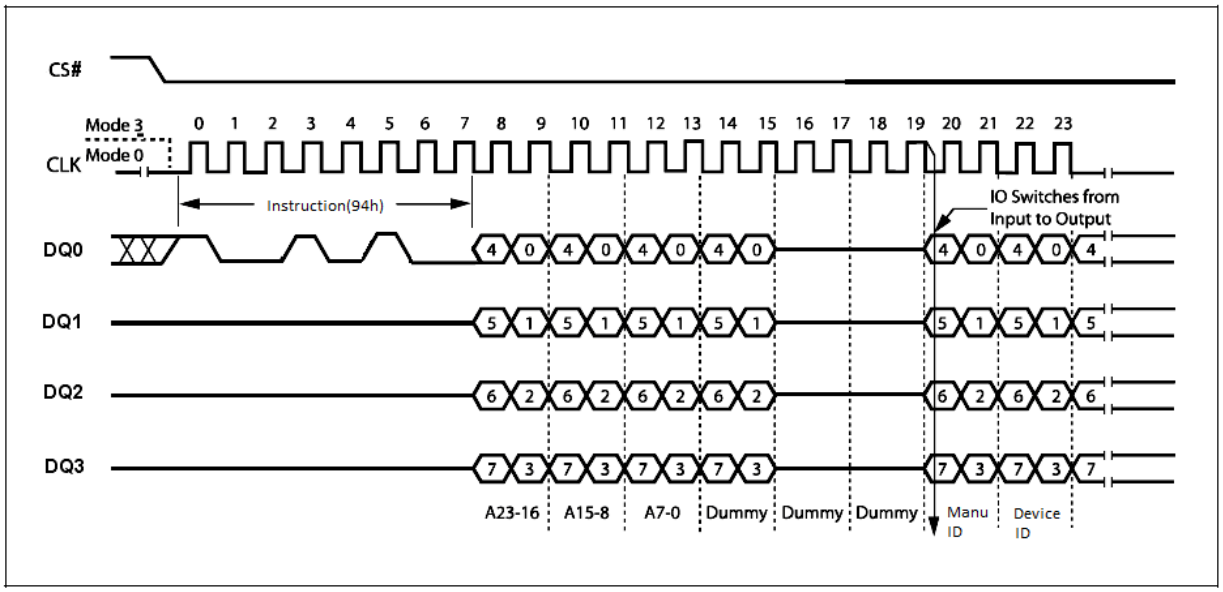
The Read Manufacturer/Device ID Dual I/O instruction is very similar to the Dual Input / Output FAST_READ instruction.
The instruction is initiated by driving the CS# pin low and shifting the instruction code “92h” followed by a 24-bit address (A23-A0) of 000000h by using DQ_0 and DQ_1 and one byte dummy. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first byte using DQ_0 and DQ_1.



Read Manufacturer / Device ID Dual I/O Instruction (SPI mode only)

Read Manufacturer / Device ID Quad I/O (94h)

The Read Manufacturer/Device ID by Quad I/O instruction is very similar to the Quad I/O Fast Read instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code “94h” followed by a 24-bit address (A23-A0) of 000000h and three byte of dummy. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Read Manufacturer / Device ID by Quad I/O Diagram figure.

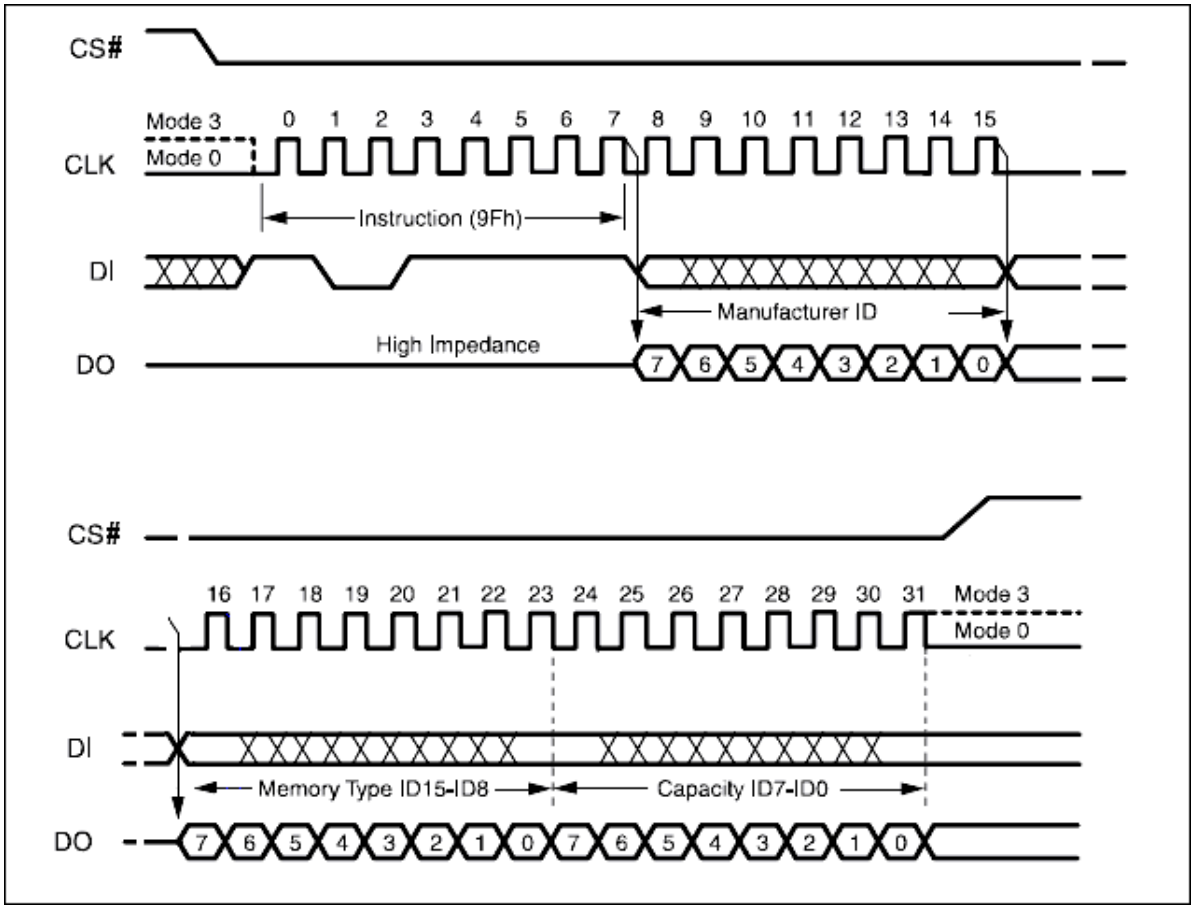


Read Manufacturer / Device ID Quad I/O Instruction (SPI mode only)

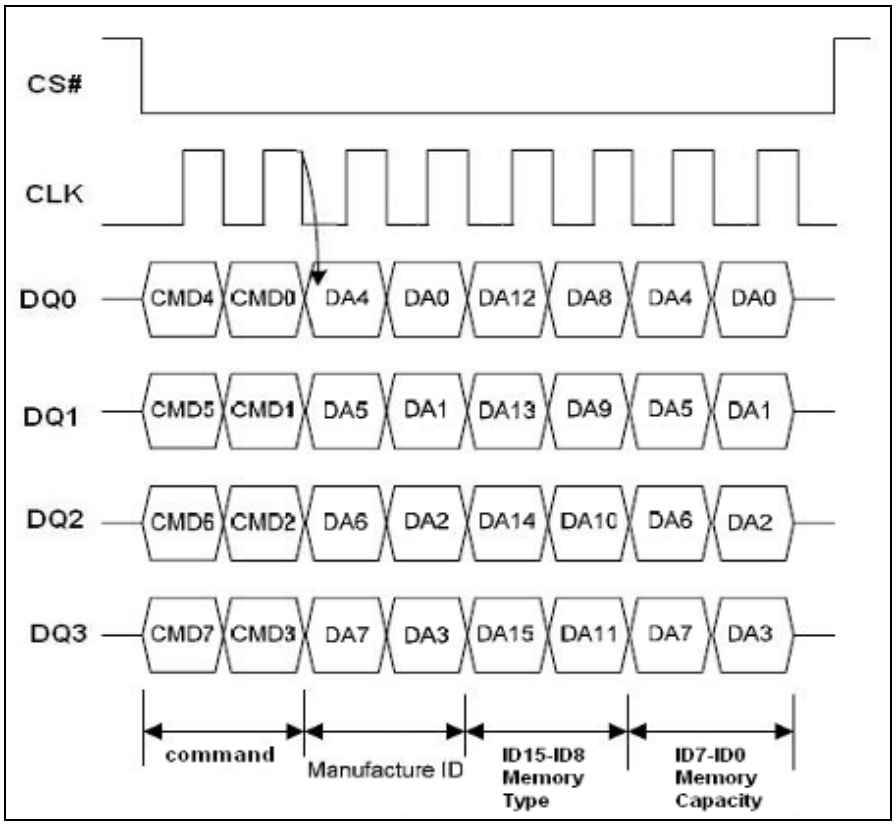
Read JEDEC ID (9Fh)

The Read JEDEC ID (9Fh) instruction allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte.
Any Read JEDEC ID instruction while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The Read JEDEC ID instruction should not be issued while the device is in Power down mode.
The device is first selected by driving Chip Select Low. Then, the 8-bit instruction code for the instruction is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The Read JEDEC ID instruction is terminated by driving Chip Select High at any time during data output.
When Chip Select is driven High, the device is put in the Standby Power mode. Once in the Standby Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

The instruction is workable while using the Enter QPI mode (EQPI) command.



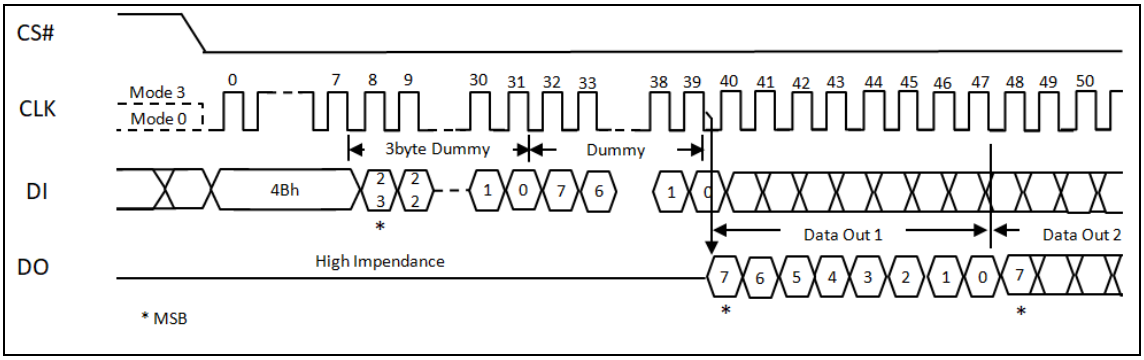
Read Identification Instruction



Read Identification Instruction (QPI Mode)

Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 128-bit number that is unique to each device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the CS# pin low and shifting the instruction code “4Bh” followed by a four dummy bytes (or five dummy bytes depends on address mode). After which, the 128-bit ID is shifted out on the falling edge of CLK. (data read after the 128-bit ID will always be FFh)



Note:

1. The above 3byte Dummy cycles are base on 3-byte address mode, for 4-byte address mode, the Dummy cycles will be increased.

Read Unique ID Instruction (SPI mode only)

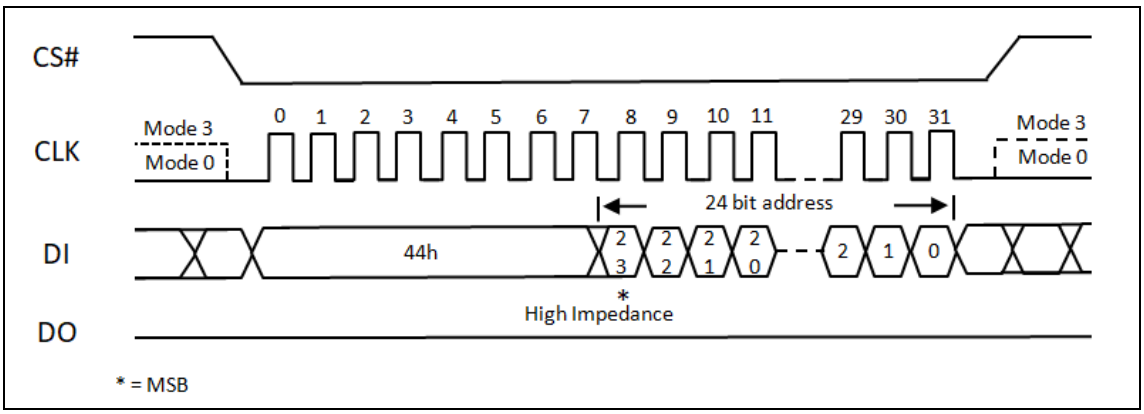
Erase OTP Sector (44h)

The device offers three sets of 2048-byte OTP array which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.
The Erase OTP array instruction is similar to the Sector Erase instruction. A Write Enable instruction must be executed before the device will accept the Erase OTP array Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “44h” followed by a 24-bit address (A23-A0) (or 32-bit address, depends on address mode state) to erase one of the three OTP sectors.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the instruction will not be executed. After CS# is driven high, the self-timed Erase OTP array operation will commence for a time duration of t_{SE} (See AC Characteristics). While the Erase OTP array cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit.
The WIP bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Erase OTP array cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Security Register Lock Bits (SPL0-2) in the Status Register-2 can be used to OTP protect the OTP sectors. Once a lock bit is set to 1, the corresponding OTP sector will be permanently locked, Erase OTP array instruction to that register will be ignored.

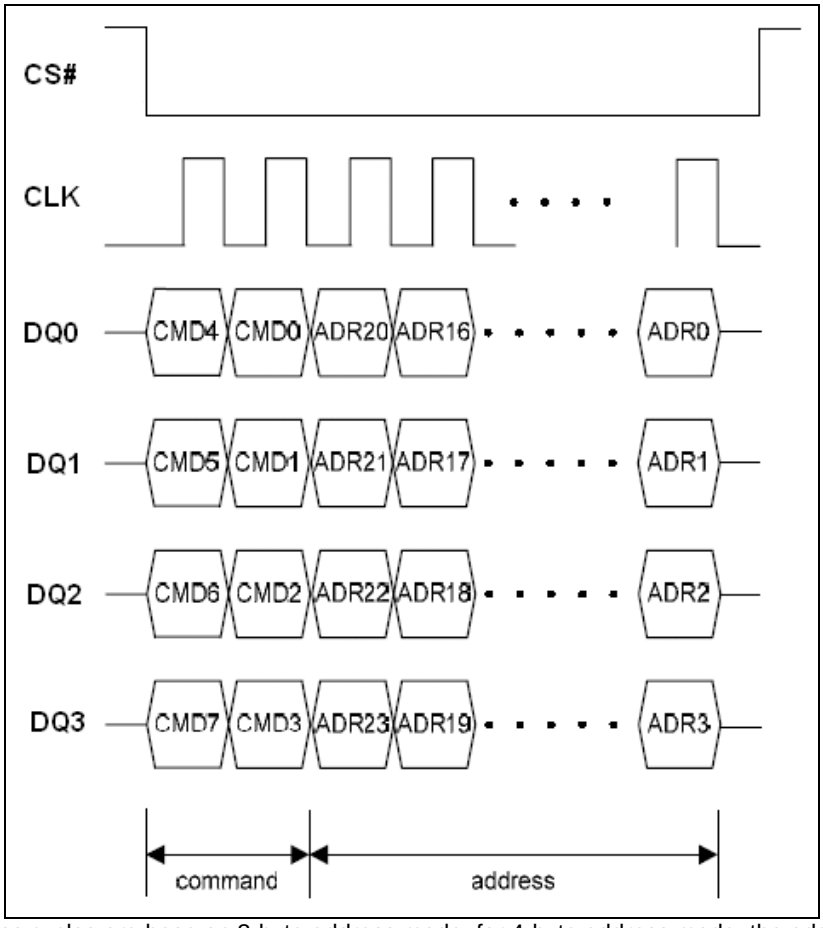
OTP Sector Address

Lock bit	Sector Size	Address Range
SPL0	2048 byte	001000h –0017FFh
SPL1	2048 byte	002000h – 0027FFh
SPL2	2048 byte	003000h – 0037FFh



Note: The above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Erase OTP array Instruction (SPI mode)

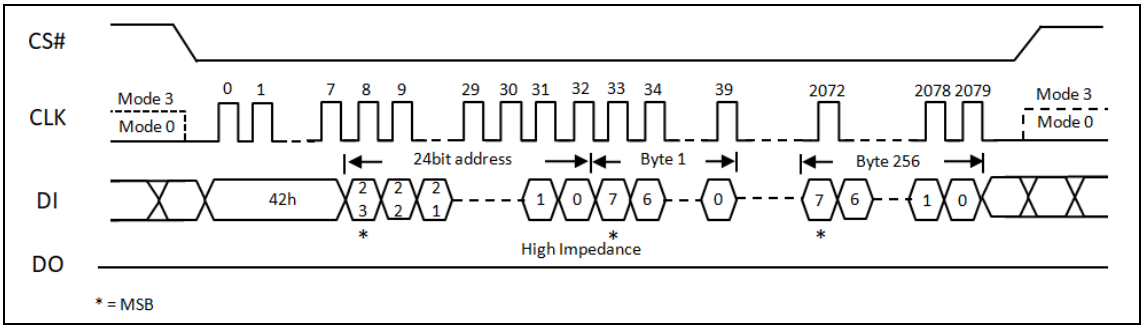


Note: The above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Erase OTP array Instruction (QPI mode)

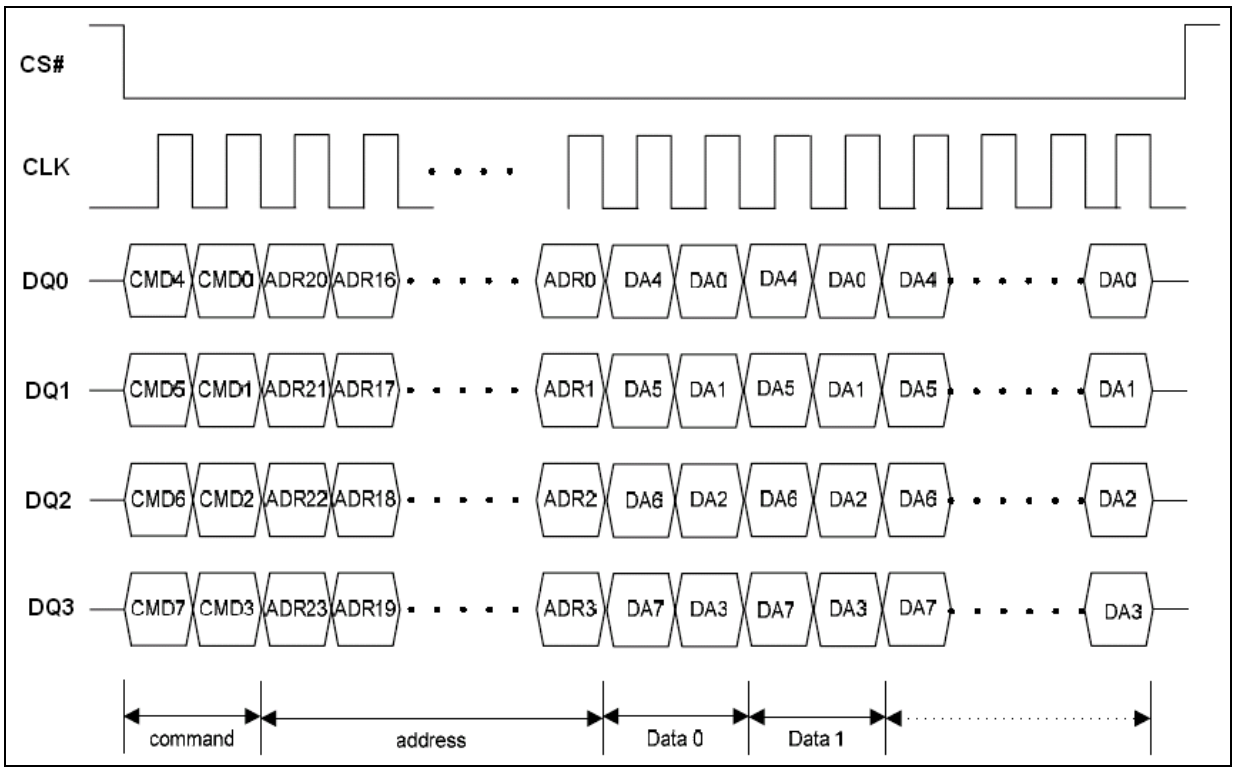
Program OTP array (42h)

The Program OTP array operation is similar to the Page Program instruction. It allows from one byte to 256 bytes of security register data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Program OTP array Instruction.
The instruction is initiated by driving the CS# pin low then shifting the instruction code “42h” followed by a 24-bit address (A23-A0) (or 32-bit address, depends on address mode state) and at least one data byte, into the DI pin. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. The Program OTP array instruction sequence is shown in Program OTP array figure. The OTP array Lock Bits (SPL0-SPL2) in Status Register2 can be used to OTP protect the OTP array data. Once a lock bit is set to 1, the corresponding OTP array will be permanently locked, Program OTP array instruction to that register will be ignored.



Note: The above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Program OTP array (SPI mode)

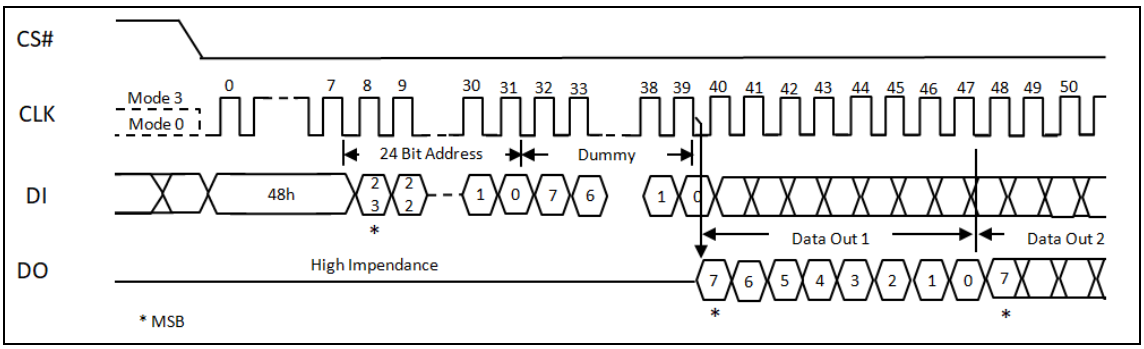


Note: The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Program OTP array (QPI Mode)

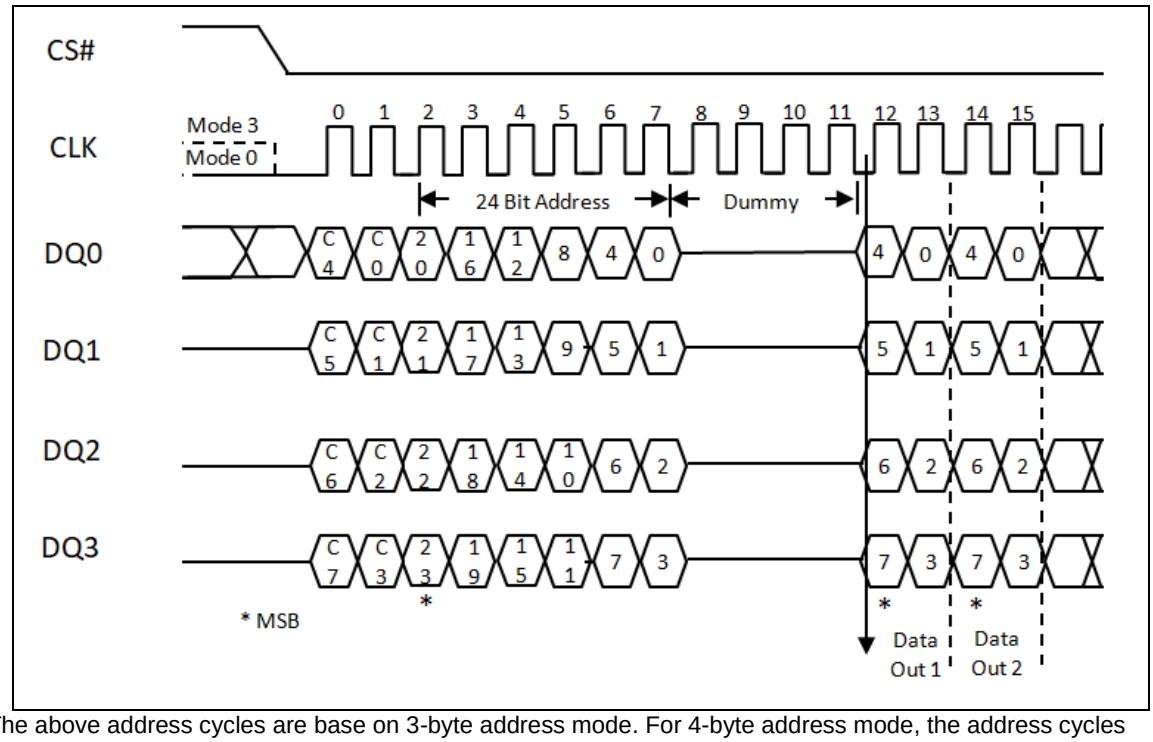
Read OTP array (48h)

The Read OTP array instruction is similar to the Fast Read instruction and allows one or more data bytes to be sequentially read from one of the three OTP array. The instruction is initiated by driving the CS# pin low and then shifting the instruction code “48h” followed by a 24-bit address (A23-A0) (or 32-bit address, depends on address mode state) and eight “dummy” clocks into the DI pin.
The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out.
The instruction is completed by driving CS# high. If a Read OTP array instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle. The Read OTP array instruction allows clock rates from D.C. to a maximum of F_R (see AC Electrical Characteristics).
If read address is out of OTP array range, the data output will always be FFh



Note: The above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Read OTP array (SPI mode)



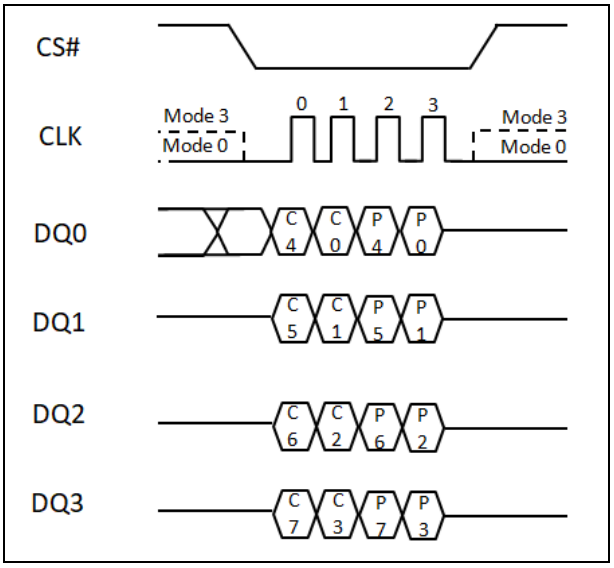
Note: The above address cycles are base on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Read OTP array (QPI Mode)

Set Read Parameters (C0h)

In QPI mode, to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency, “Set Read Parameters (C0h)” instruction can be used to configure the number of dummy clocks for “Fast Read (0Bh/0Dh)”, “Fast Read Quad I/O (EBh/ECh/EDh/EEh)” , “Burst Read with Wrap (0Ch/0Eh)” instructions, and to configure the number of bytes of “Wrap Length” for the “Burst Read with Wrap (0Ch/0Eh)” instruction.
In Standard SPI mode, the “Set Read Parameters (C0h)” instruction is not accepted. The dummy clocks for various Read instructions in Standard/Dual/Quad SPI mode are defined by SR3.3 and SR3.4. The “Wrap Length” is set by W5-4 bit in the “Set Burst with Wrap (77h)” instruction.
After a Power-Up or Reset instruction, the default "Wrap Length" is 8 Bytes and the default number of dummy clocks is 4 for STR, 10 for DTR. The number of dummy clocks is only programmable for “Fast Read (0Bh/0Dh)”, “Fast Read Quad I/O (EBh/ECh/EDh/EEh)” and “Burst Read with Wrap (0Ch/0Eh)” instructions in the QPI mode. Whenever the device is switched from SPI mode to QPI mode, the number of dummy clocks should be set again before any 0B/0Dh, EBh/ECh/EDh/EEh or 0C/0Eh instructions.

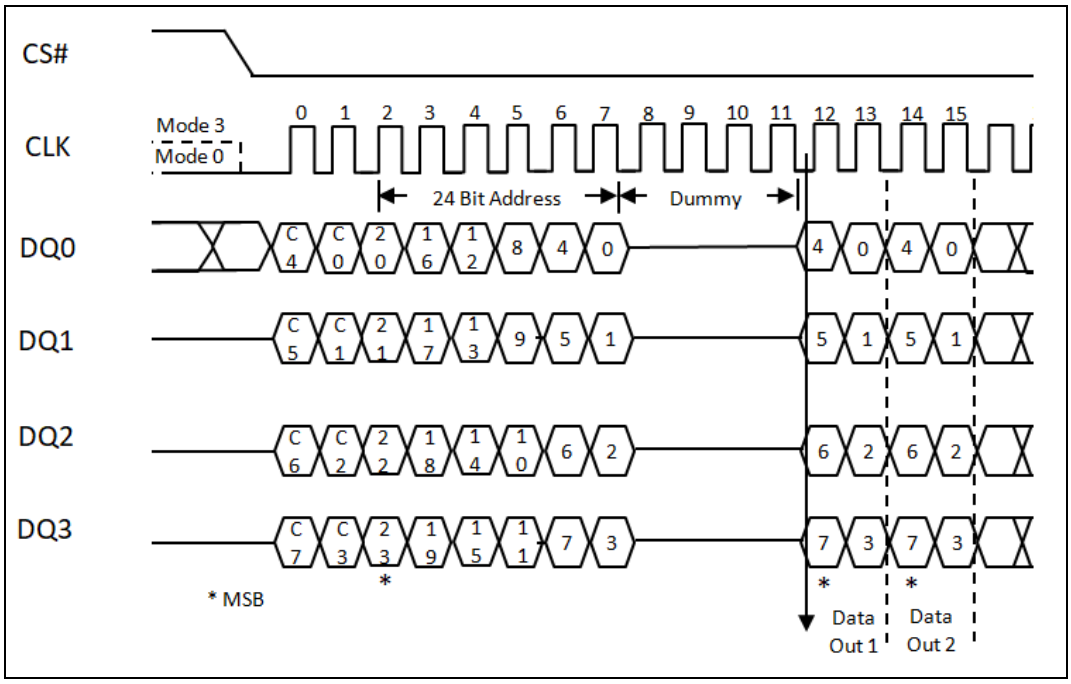
P1,P0	Wrap length
00 (default)	8 byte
01	16 byte
10	32 byte
11	64 byte



Set Read Parameters Instruction (QPI mode only)

Burst Read with Wrap (0Ch)

This device supports Burst Read with wrap in QPI mode. To execute a Burst Read with wrap operation the host drivers CS# low, and sends the Burst Read with wrap (0Ch) command cycle, followed by three address bytes (or four address bytes depends on address mode state) and default four dummy clocks in QPI mode.
After the dummy byte, the device outputs data on the falling edge of the CLK signal starting from the specific address location. The data output stream is continuous through all addresses until terminated by a low-to high transition of CS# signal.
During Read Burst, the internal address point automatically increments until the last byte of the burst reached, then jumps to first byte of the burst. All bursts are aligned to addresses within the burst length. For example, if the burst length is 8 bytes, and the start address is 06h, the burst sequence should be: 06h, 07h, 00h, 01h, 02h, 03h, 04h, 05, 06, etc. The pattern would repeat until the command was terminated by pulling CS# as high status.



Note:

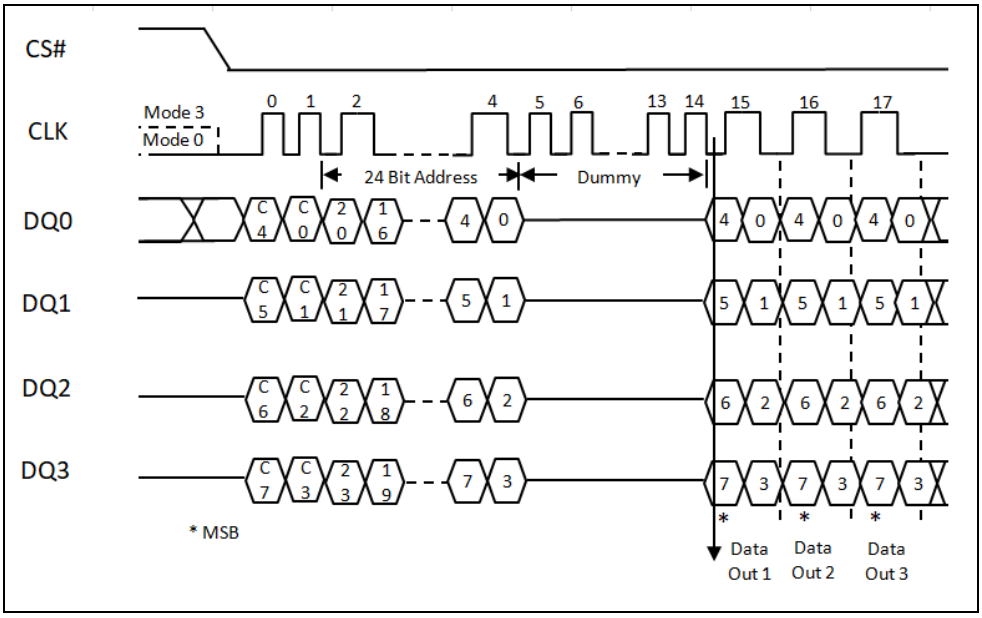
1. The above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.
2. The dummy clock and wrap length can be set by Set Parameter (C0h)

Burst Read with Wrap Instruction (QPI Mode only)

DTR Burst Read with Wrap (0Eh)

The DDR Burst Read with Wrap (0Eh) instruction enable Double Data Rate throughput in QPI mode. The address is latched on both rising and falling edge of CLK, and data shift out on both rising and falling edge on CLK at a maximum frequency F_R. The 8-bit address can be latched-in at one clock, and 8-bit data can be read out at one clock, which means four bits at rising edge of clock, the other four bits at falling edge of clock. Once writing DDR Burst Read with Wrap (0Eh) instruction, the following address/dummy/data out will perform as 8-bit instead of previous 1-bit.
The sequence of issuing DDR Burst Read with Wrap (0Eh) instruction is: CS# goes low -> sending DDR Read Burst with Wrap (0Eh) instruction (4-bit per clock) -> 24 bit address (or 32bit address depends on mode status) interleave on DQ_0-DQ_3 (8-bit per clock) -> ten dummy clocks -> data out interleave on DQ_0-DQ_3 (8-bit per clock) -> to end DDR Burst Read with Wrap (0Eh) operation can use CS# to high at any time during data out.

During DDR Burst Read with Wrap, the first address byte can be at any location. The internal address point automatically increments until the last byte of the burst reached, then jumps to first byte of the burst. All bursts are aligned to addresses within the burst length. For example, if the burst length is 8 bytes, and the start address is 06h, the burst sequence should be: 06h, 07h, 00h, 01h, 02h, 03h, 04h, 05, 06, etc. The pattern would repeat until the command was terminated by pulling CS# as high status.



Note:
1. The above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

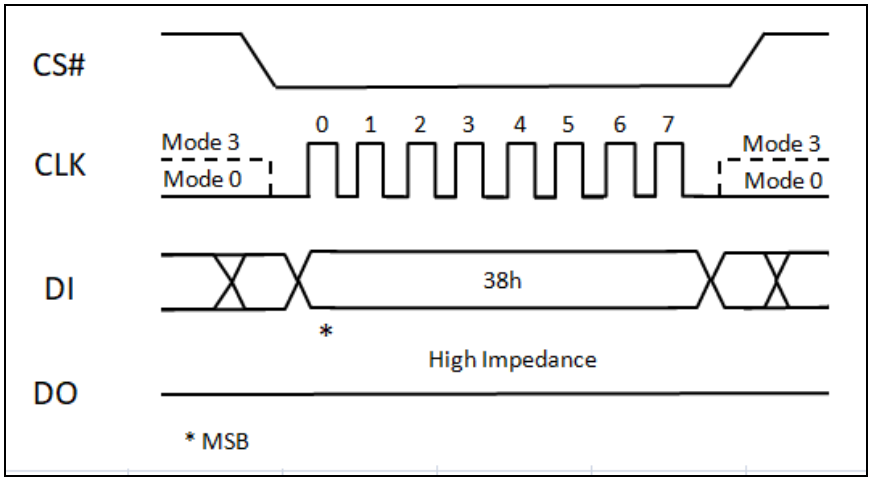
2. Dummy clock and wrap length can be set by Set Parameter (C0h)

DDR Read Burst with Wrap Instruction (QPI mode only)

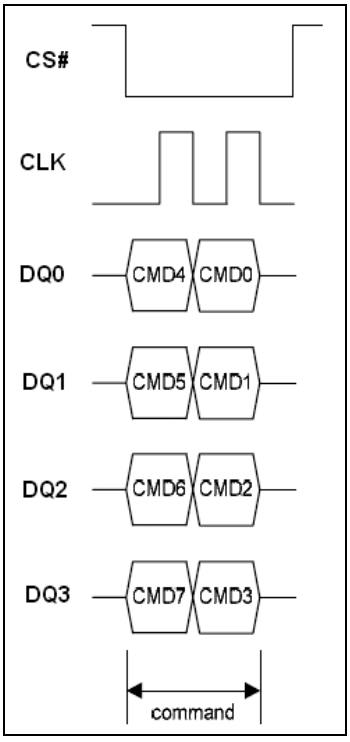
Enter QPI Mode (38h) and Exit QPI Mode (FFh)

The Enter QPI mode (EQPI) instruction will enable the flash device for Quad SPI bus operation. Before switching the device to QPI mode, the Quad Enable (QE) bit in Status Register-2 must be set to 1 first, and the "Enter QPI (38h)" instruction must be issued. If the Quad Enable (QE) bit is 0, the "Enter QPI (38h)" instruction will be ignored and the device will remain in SPI mode.
Upon completion of the instruction, all instructions thereafter will be 4-bit multiplexed input/output until a power cycle or "Reset Quad I/O instruction" instruction. The device did not support the Read Data Bytes (READ) (03h/13h), Fast Read Dual Output (3Bh/3Ch), Fast Read Dual I/O (BBh/BCh), Fast Read Quad Output (6Bh/6Ch), DTR Fast Read Dual I/O (BDh) and Word Fast Read Quad I/O(E7h) modes while the Enter QPI mode (EQPI) (38h) turns on.

The Exit QPI instruction resets the device to 1-bit Standard SPI operation. To execute a Exit QPI operation, the host drives CS# low, sends the Exit QPI command cycle (FFh) then, drives CS# high. This command can't be used in Standard SPI mode. When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch (WEL) and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.



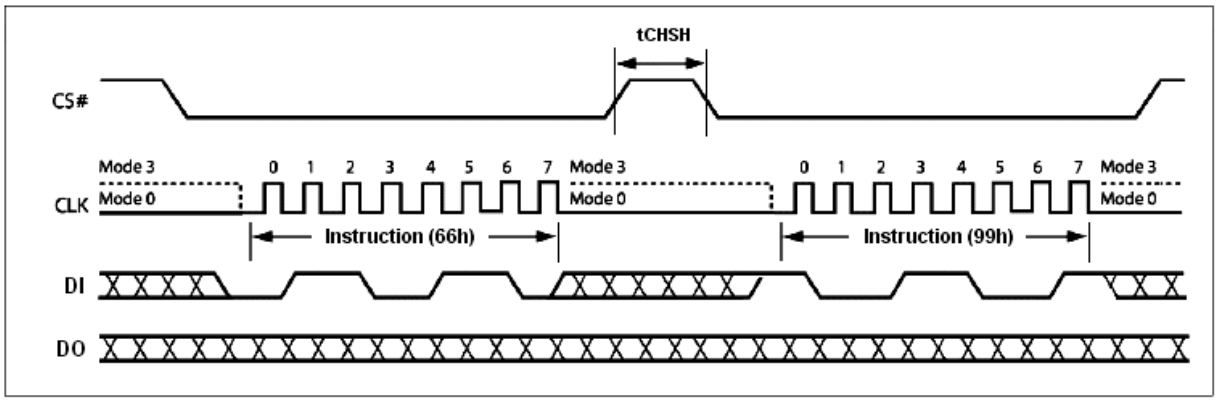
Enter QPI mode Instruction(SPI mode only)



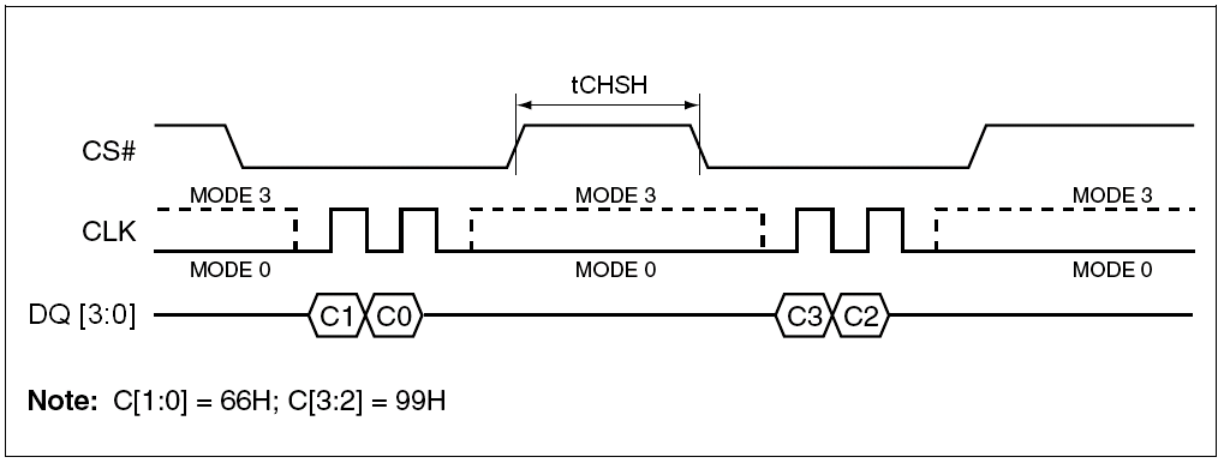
Exit QPI Instruction (QPI Mode only)

Enable Reset (66h) and Reset Device (99h)

The Reset operation is used as a system (software) reset that puts the device in normal operating Ready mode. This operation consists of two commands: Reset-Enable (RSTEN) and Reset (RST).
To reset the device the host drives CS# low, sends the Reset-Enable command (66h), and drives CS# high. Next, the host drives CS# low again, sends the Reset command (99h), and drives CS# high.
The Reset operation requires the Reset-Enable command followed by the Reset command. Any command other than the Reset command after the Reset-Enable command will disable the Reset-Enable.
A successful command execution will let any on-going internal operations be terminated and the device will return to its default power-on state and all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Read parameter setting (P7-P0) and Wrap Bit setting (W6-W4)
A device reset during an active Program or Erase operation aborts the operation, which can cause the data of the targeted address range to be corrupted or lost. It is recommended that the WIP bit and SUS bit in the Status Register be checked before issuing a reset command sequence. Depending on the prior operation, the reset timing may vary. Recovery from a Write operation requires more software latency time (t_{SR}) than recovery from other operations. During this period, no command will be accepted.



Enable Reset and Reset Instructions (SPI mode)

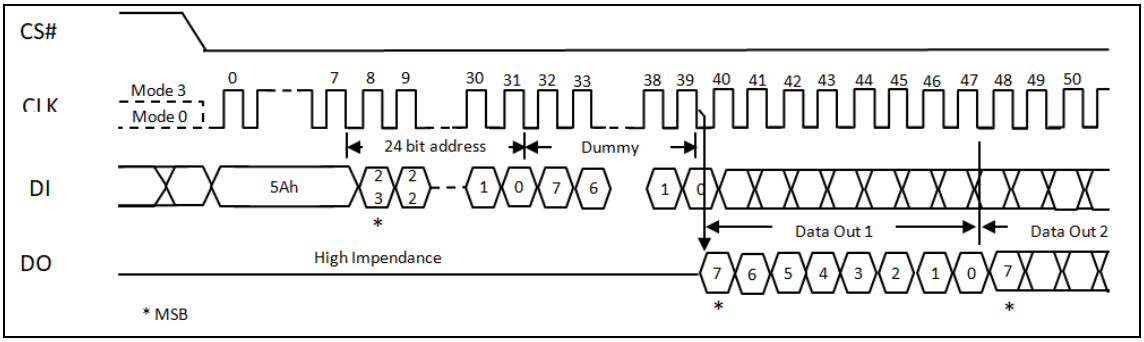


Enable Reset and Reset Instructions (QPI Mode)

Read SFDP Register (5Ah)

The device features Serial Flash Discoverable Parameters (SFDP) mode. Host system can retrieve the operating characteristics, structure and vendor specified information such as identifying information, memory size, operating voltage and timing information of this device by SFDP mode.
The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read SFDP Mode is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (CLK). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency F_R, during the falling edge of Serial Clock (CLK).
The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, data read will always be FFh. The Serial Flash Discoverable Parameters (SFDP) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes at Serial Flash Discoverable Parameters (SFDP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.
The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216B

After each Byte of data is shifted out, the Byte address is automatically incremented to the next Byte address. The last Byte address of the register is FFh (data read after the last address will always be FFh).

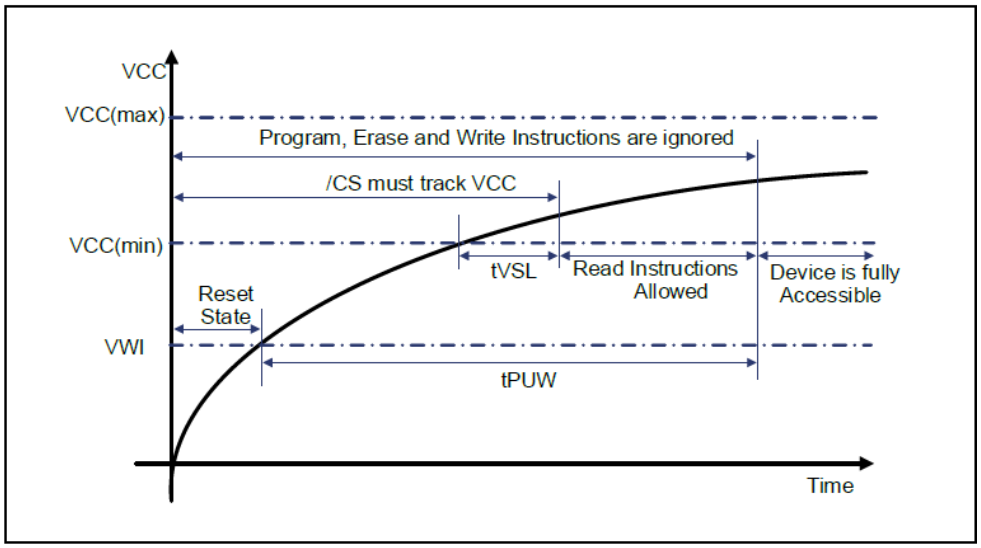


Read SFDP Mode and Unique ID Number Instruction (SPI mode only)

Power-Up and Power-Down Timing[1]

Parameter	Symbol	Min.	Max.	Unit
V_{CC} (min) to CS# Low	t_{VSL}	1.8	-	ms
Time Delay Before Write Instruction	t_{PUW}	2	-	ms
Write Inhibit Voltage	V_{WI}	1.5	2.3	V
The minimum duration for ensuring initialization will occur	t_{PWD}	100	-	µs
V_{CC} voltage needed to below V_{PWD} for ensuring initialization will occur	V_{PWD}	-	1	V

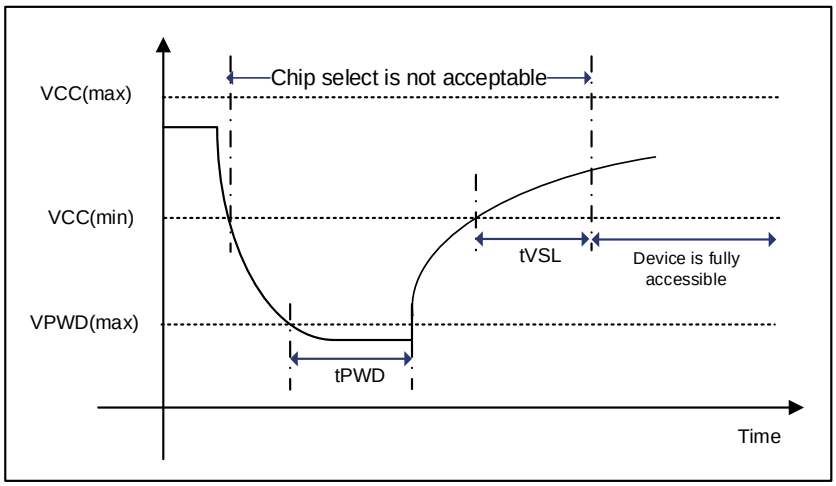
.
Note:
1. These parameters are characterized only.
2. CS# must track V_{CC} during power down



Power-up Timing and Voltage Levels

Power Down Requirement

During Power-down, the system must initialize the power-up procedure only when V_{CC} drops below V_{PWD} and hold a t_{PWD} for the device to initialize correctly.



Power-Down and Power-up Requirement

ELECTRICAL CHARACTERISTICS

DC Characteristics[1]

(T_A = -40°C to 85°C; V_{CC} = 2.3-3.6V)

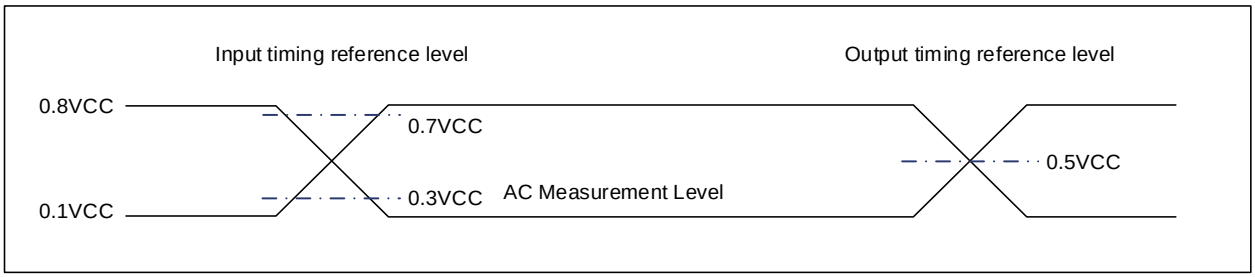
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current			-	-	± 2	µA
I_{LO}	Output Leakage Current			-	-	± 2	µA
I_{CC1}	Standby Current	CS# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	T_A = -40°C to 85°C	-	12	30	µA
I_{CC2}	Power-down Current	CS# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	T_A = -40°C to 85°C	-	0.5	10	µA
I_{CC3}	Operating Current (READ) [1]	CLK = 0.1 V_{CC} / 0.9 V_{CC} at 166MHz, DQ = open (x4 I/O)		-	10	25	mA
		CLK = 0.1 V_{CC} / 0.9 V_{CC} at 80MHz, DQ = open (x4 I/O)		-	6	20	mA
		CLK = 0.1 V_{CC} / 0.9 V_{CC} at 108MHz, DQ = open (x4 I/O) DTR		-	10	25	mA
I_{CC5}	Operating Current (PP)	CS# = V_{CC}		-	7	15	mA
I_{CC6}	Operating Current (WRSR)	CS# = V_{CC}		-	4	12	mA
I_{CC7}	Operating Current (SE, BE)	CS# = V_{CC}		-	7	15	mA
I_{CC7}	Operating Current (CE)	CS# = V_{CC}		-	6	15	mA
V_{IL}	Input Low Voltage			-0.5	-	V_{CC} x0.3	V
V_{IH}	Input High Voltage			V_{CC} x0.7	-	V_{CC}+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA		-	-	0.2	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA		V_{CC}-0.2	-	-	V

Note:
1. 0XFF Pattern.

AC Measurement Conditions[1]

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance		30	pF
T_R, T_F	Input Rise and Fall Times	-	5	ns
V_{IN}	Input Pulse Voltages	$0.1V_{CC}$ to $0.8V_{CC}$		V
IN	Input Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V
OUT	Output Timing Reference Voltages	$0.5V_{CC}$ to $0.5V_{CC}$		V

Note:
1. Output Hi-Z is defined as the point where data out is no longer driven.



AC Measurement I/O Waveform

AC Characteristics[5]

(T_A = -40°C to 85°C; V_{CC} = 2.3-3.6V)

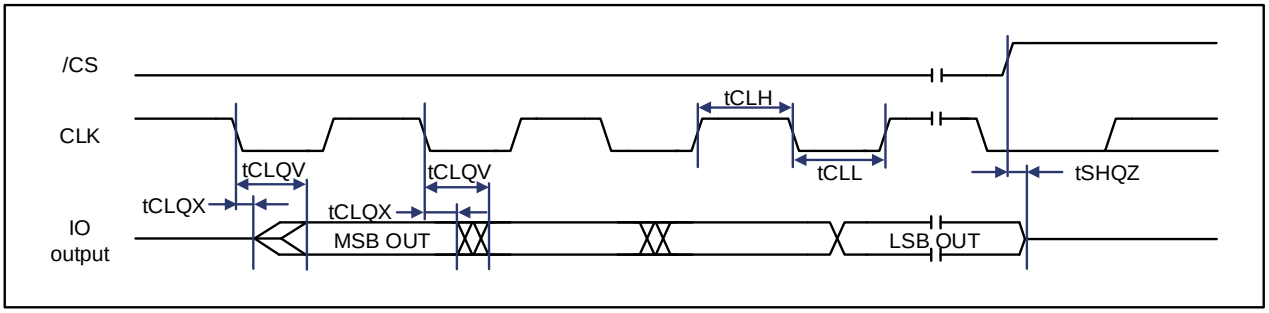
Symbol	Alt	Parameter	Min	Typ	Max	Unit
f_C	f_{C1}	Serial Clock Frequency for: All command except Read (03H) and DTR instructions (2.7~3.6V)	D.C.	-	166[1]	MHz
	f_{C1}	Serial Clock Frequency for: All command except Read (03H) and DTR instructions (2.3~2.7V)	D.C.	-	133[1]	MHz
F_R	f_{C2}	Serial Clock Frequency for: DTR instructions	D.C.	-	108	MHz
f_R		Serial Clock Frequency For: Read (03H) (2.7~3.6V)	D.C.	-	108	MHz
		Serial Clock Frequency For: Read (03H) (2.3~2.7V)	D.C.	-	80	MHz
t_{CLH}, t_{CLL}[1]		Clock High, Low Time	45% PC	-	-	ns
t_{CLCH}[3]		Serial Clock Rise Time (Slew Rate)	0.1	-	-	V / ns
t_{CHCL}[3]		Serial Clock Fall Time (Slew Rate)	0.1	-	-	V / ns
t_{SLCH}	t_{CSS}	CS# Active Setup Time relative to CLK	5	-	-	ns
t_{CHSL}		CS# Not Active Hold Time relative to CLK	5	-	-	ns
t_{DVCH}	t_{DSU}	Data in Setup Time	2	-	-	ns
t_{CHDX}	t_{DH}	Data in Hold Time	3	-	-	ns
t_{CHSH}		CS# Active Hold Time relative to CLK	5	-	-	ns
t_{SHCH}		CS# Not Active Setup Time relative to CLK	5	-	-	ns
t_{SHSL1}	t_{CSH}	CS# Deselect Time (for Read)	10	-	-	ns
t_{SHSL2}	t_{CSH}	CS# Deselect Time (for Erase or Program or write)	30	-	-	ns
t_{SHQZ}[3]	t_{DIS}	Output Disable Time	-	-	6	ns
t_{CLQV}	t_V	Clock Low to Output Valid for 30pF	-	-	7	ns
t_{CLQV}	t_V	Clock Low to Output Valid for 15pF	-	-	6	ns
t_{CLQX}	t_{HO}	Output Hold Time	1	-	-	ns
t_{HLCH}		HOLD# Active Setup Time relative to CLK	5	-	-	ns
t_{CHHH}		HOLD# Active Hold Time relative to CLK	5	-	-	ns
t_{HHCH}		HOLD# Not Active Setup Time relative to CLK	5	-	-	ns
t_{CHHL}		HOLD# Not Active Hold Time relative to CLK	5	-	-	ns

AC Characteristics-Continued

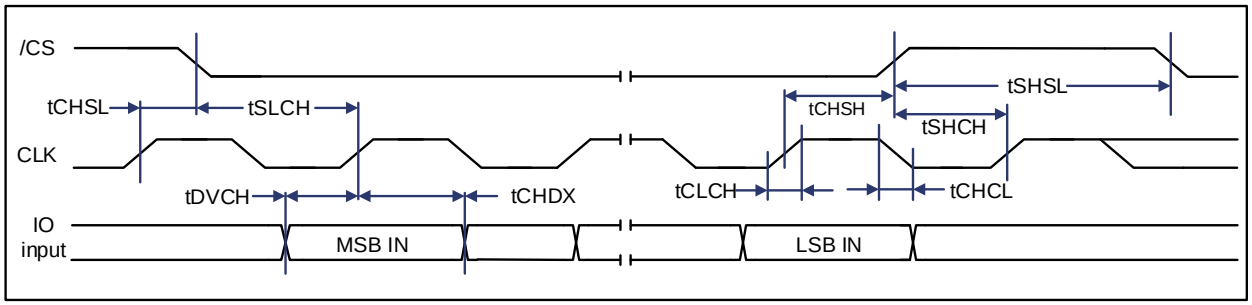
Symbol	Alt	Parameter		Min	Typ	Max	Unit
t_{HHQX}[3]	t_{LZ}	HOLD# to Output Low-Z		-	-	6	ns
t_{HLQZ}[3]	t_{HZ}	HOLD# to Output High-Z		-	-	6	ns
t_{WHSL}[4]		Write Protect Setup Time Before CS# Low		20	-	-	ns
t_{SHWL}[4]		Write Protect Hold Time After CS# High		100	-	-	ns
t_{DP}[3]		CS# High to Power-down Mode		-	-	3	µs
t_{RES1}[3]		CS# High to Standby Mode without ID Read	T_A = -40°C to 85°C	-	-	30	µs
t_{RES2}[4]		CS# High to Standby Mode with ID Read	T_A = -40°C to 85°C	-	-	30	µs
t_{SUS}[3]		CS# High to next Instruction after Suspend		-	-	22	µs
t_{ERS}[2]		Latency Between Resume And Next Suspend		50	-	-	µs
t_{RESET}[3] [5]		RESET# pin Low period to reset the device		1	-	-	µs
t_W		Write Status Register Time		-	0.03	15	ms
t_{PP}		Page Program Time		-	0.25	2	ms
t_{SE}		Sector Erase Time (4KB)		-	25	300	ms
t_{BE1}		Block Erase Time (32KB)		-	80	800	ms
t_{BE2}		Block Erase Time (64KB)		-	120	1000	ms
t_{CE}[7]		Chip Erase Time			40[7]	200	s
t_{SR}		Reset Latency(BUSY = write operation)				28	µs
t_{SR}		Reset Latency(BUSY = read operation)				0.3	µs
t_{SR}		Reset Latency(BUSY = erase operation)				12	ms

Note:

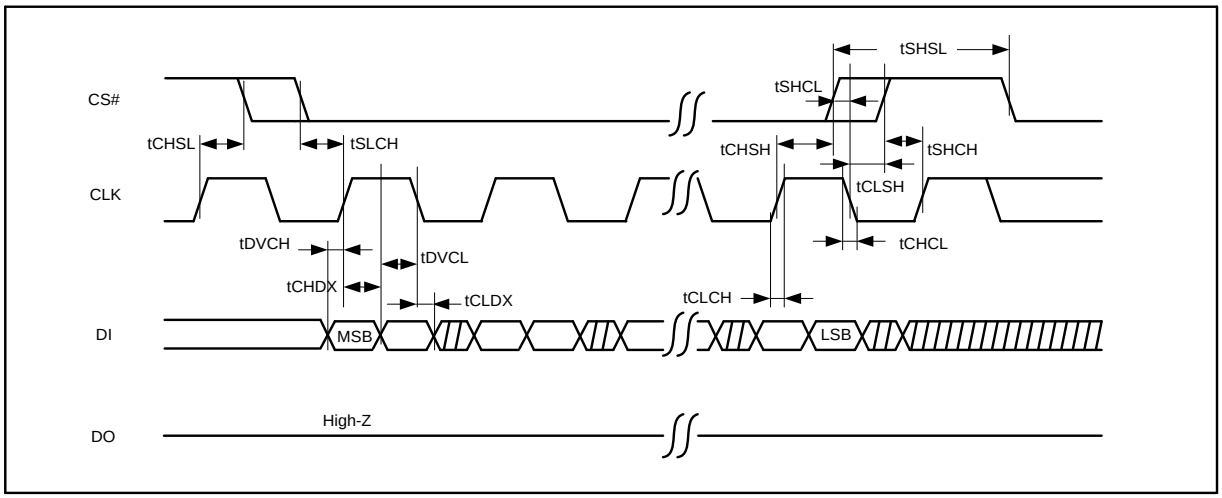
1. For a 4I/O command with 8 dummy clock cycles capable of 166MHz, the start alignment address should maintain [A1,A0]=(0,0).；
2. Clock high or Clock low must be more than or equal to 45% Pc. Pc=1/fc(max)；
3. Value guaranteed by design and/or characterization, not 100% tested in production；
4. Only applicable as a constraint for a Write Status Register instruction when SRP[1:0]=(0,1)；
5. It's possible to reset the device with shorter t_{RESET} (as short as a few hundred ns), a 1us minimum is recommended to ensure reliable operation；
6. The address alignment for Dual/Qual IO read with default dummy；
7. For Blank Flash (FFh pattern), the chip erase typical time will be 3s.



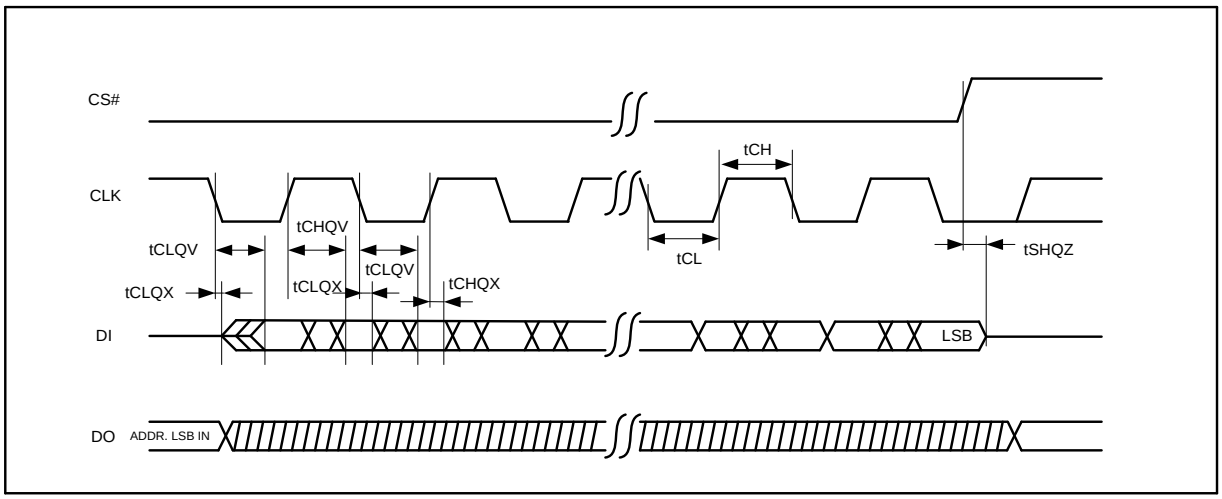
Serial Output Timing



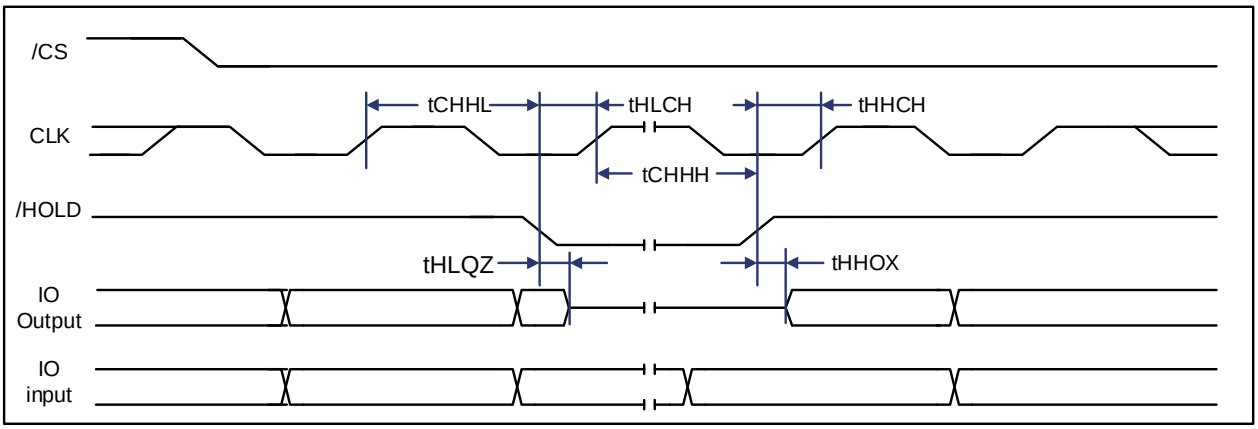
Serial Input Timing



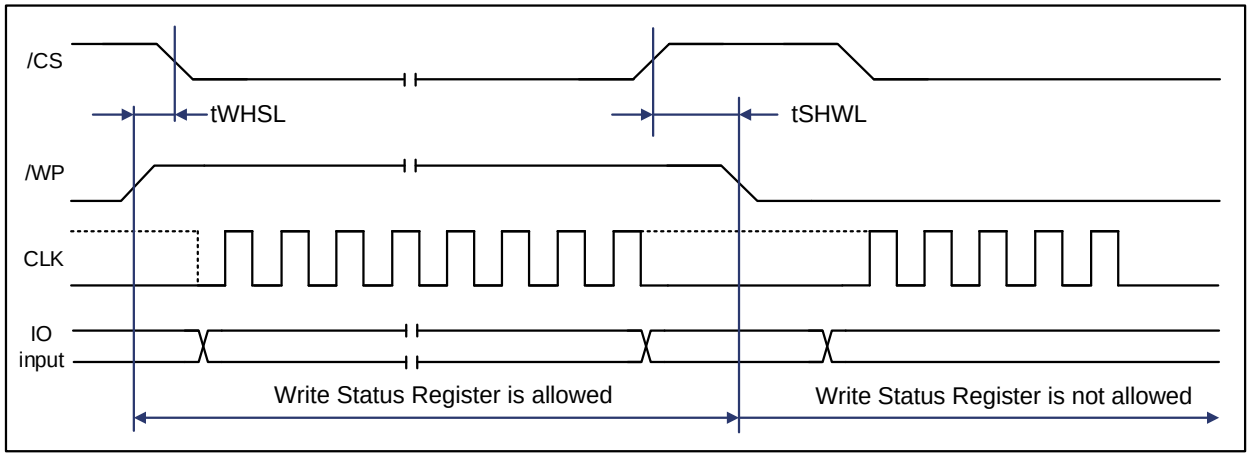
Serial Input Timing (DTR)



Serial Output Timing (DTR)



HOLD# Timing



WP# Timing

OPERATING RANGES[1]

Parameter	Symbol	Conditions	Min.	Max.	Unit
Supply Voltage	V_{CC}	f_C = 166MHz, f_R = 108MHz	2.7	3.6	V
Supply Voltage	V_{CC}	f_C = 133MHz, f_R = 80MHz	2.3	2.7	V
Ambient Operating Temperature	T_A	Industrial	-40	+85	°C

Note:

1. These parameters are characterized only

ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Symbol	Conditions	Range	Unit
Supply Voltage	V_{CC}		-0.6 to 4.6	V
Transient Voltage on Any Pin	V_{IOT}	<20nS Transient Relative to Ground	-2.0 to V_{CC}+2.0	V
Voltage Applied to Any Pin	V_{IO}	Relative to Ground	-0.6 to V_{CC}+0.4	V
Electrostatic Discharge Voltage	V_{ESD}	Human Body Model[2]	-2000 to +2000	V
Storage Temperature	T_{STG}		-65 to +150	°C

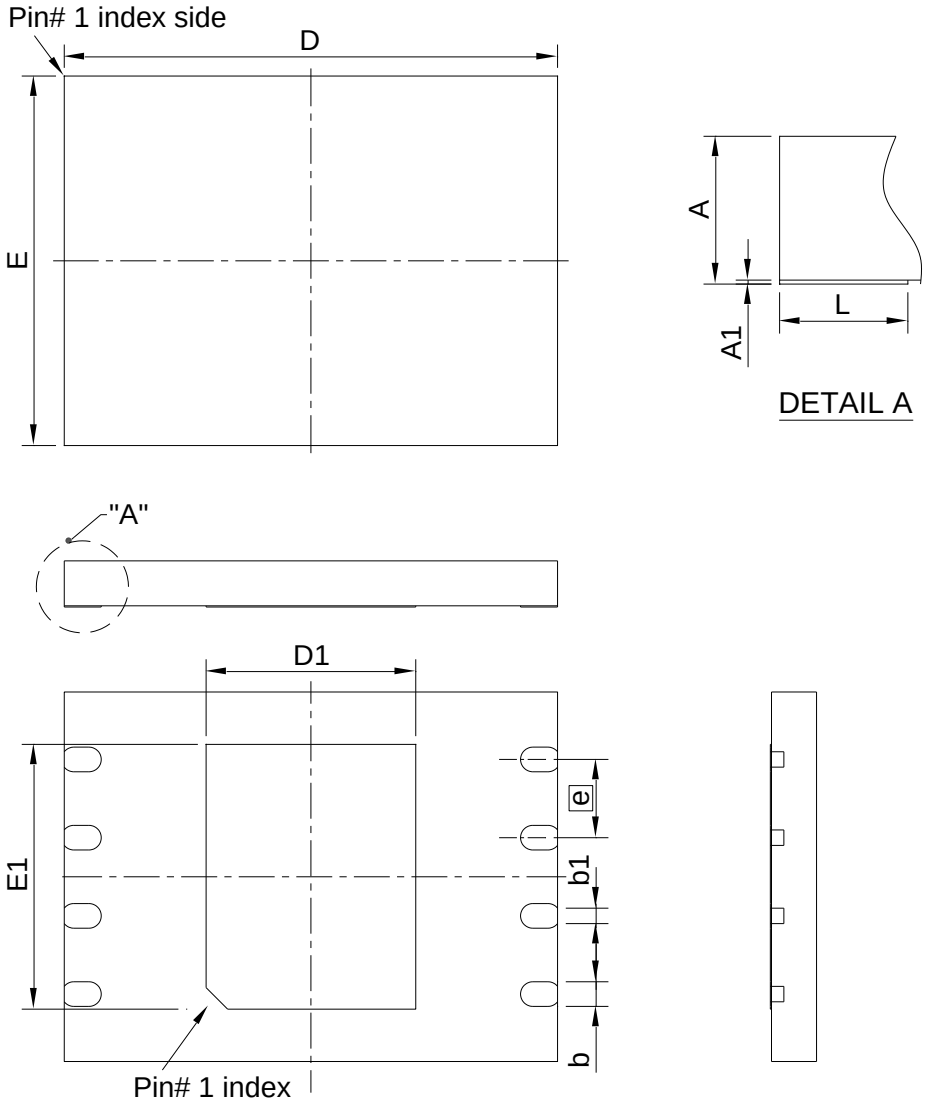
Note:
1. Stresses greater than those spec listed in the "Absolute Maximum Ratings" table may lead to permanent damage to the device. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage;
2. JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms);

CAPACITANCE

Parameter Symbol	Parameter Description	Min	Max	Unit
C_{IN}	Input Capacitance	-	6	pF
C_{OUT}	Output Capacitance	-	8	pF

PACKAGE MECHANICAL

VDFN / WSON8 6x8 mm



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.35	0.40	0.48	0.014	0.016	0.019
b1	0.22	-	0.48	0.009	-	0.019
D	7.90	8.00	8.10	0.311	0.315	0.319
D1	3.30	3.40	3.50	0.130	0.134	0.138
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	4.20	4.30	4.40	0.165	0.169	0.173
e	1.27 BSC			0.050 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024

Controlling dimension : Millimeter.
(Revision date : Sep 09. 2025)

ORDERING INFORMATION

EN25QT256A - Y I P 2V

DIFFERENTIATION CODE
2V = Default QE=0 (Programmable)
2VC = Default QE=1 (Programmable)

PACKAGING CONTENT
P = RoHS, Halogen-Free and REACH compliant

TEMPERATURE RANGE
I = Industrial (-40°C to +85°C)

PACKAGE
Y = VDFN / WSON8 6x8 mm

BASE PART NUMBER
EN = Eon Silicon Solution Inc.
25QT = 3V Serial Flash with 4KB Uniform-Sector
256 = 256 Megabit
A = version identifier

Valid Product IDs

The following table provides the valid product IDs for the EN25QT256A serial NOR Flash memory. Please contact ESMT for specific availability by density and package type.

Valid Product IDs for EN25QT256A

-40°C to 85°C

Package Type	Density	Product IDs (Ordering)	Remark
VDFN / WSON8 6x8mm **Y**	256M-bit	EN25QT256A-YIP2V EN25QT256A-YIP2VC	

Note:
1. Please contact ESMT for details regarding the specific package availability and minimum order quantities.
2. These package types are for reference only. Please refer to the mechanical dimensions for exact specifications.

Revisions List

Revision No	Description	Date
0.1	Initial Release	2026.05.04
0.2	Modify: Ordering Info. Product ID	2026.06.01
0.3	Correct PKG symbol	2026.06.04
1.0	Version upgrade: Preliminary deleted	2026.09.24

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