LPDDR2 SDRAM

4M x 32 Bit x 8 Banks LPDDR2 SDRAM

Feature

- JEDEC LPDDR2-S4B compliance
- HSUL_12 interface (High Speed Unterminated Logic 1.2V)
- Power supply:
  - V_{DD1} = 1.7 to 1.95V
  - V_{DD2}, V_{DDCA}, V_{DDQ} = 1.14 to 1.3V
- 4n prefetch architecture
- Multiplexed, double data rate, command/address inputs; commands entered on every CK edge
- Bidirectional/differential data strobe per byte of data (DQS_t/DQS_c)
- Programmable read latency (RL) and write latency (WL)
- Programmable burst lengths (BL): 4, 8, 16
- Per bank refresh for concurrent operation
- Partial Array Self Refresh (PASR)
- Temperature Compensated Self Refresh (TCSR) by built-in temperature sensor
- Deep Power Down mode (DPD)
- Programmable Driver Strength (DS)
- Clock stop capability

Ordering Information

Product ID	Max Freq. (MHz)	Data Rate (Mb/s/pin)	RL	WL	V_{DD1} / V_{DD2}, V_{DDCA}, V_{DDQ}	Package	Comments
M54D1G3232A-1.8BKG2G	533	1066	8	4	1.8V / 1.2V	134 ball BGA	Pb-free
M54D1G3232A-2.5BKG2G	400	800	6	3			

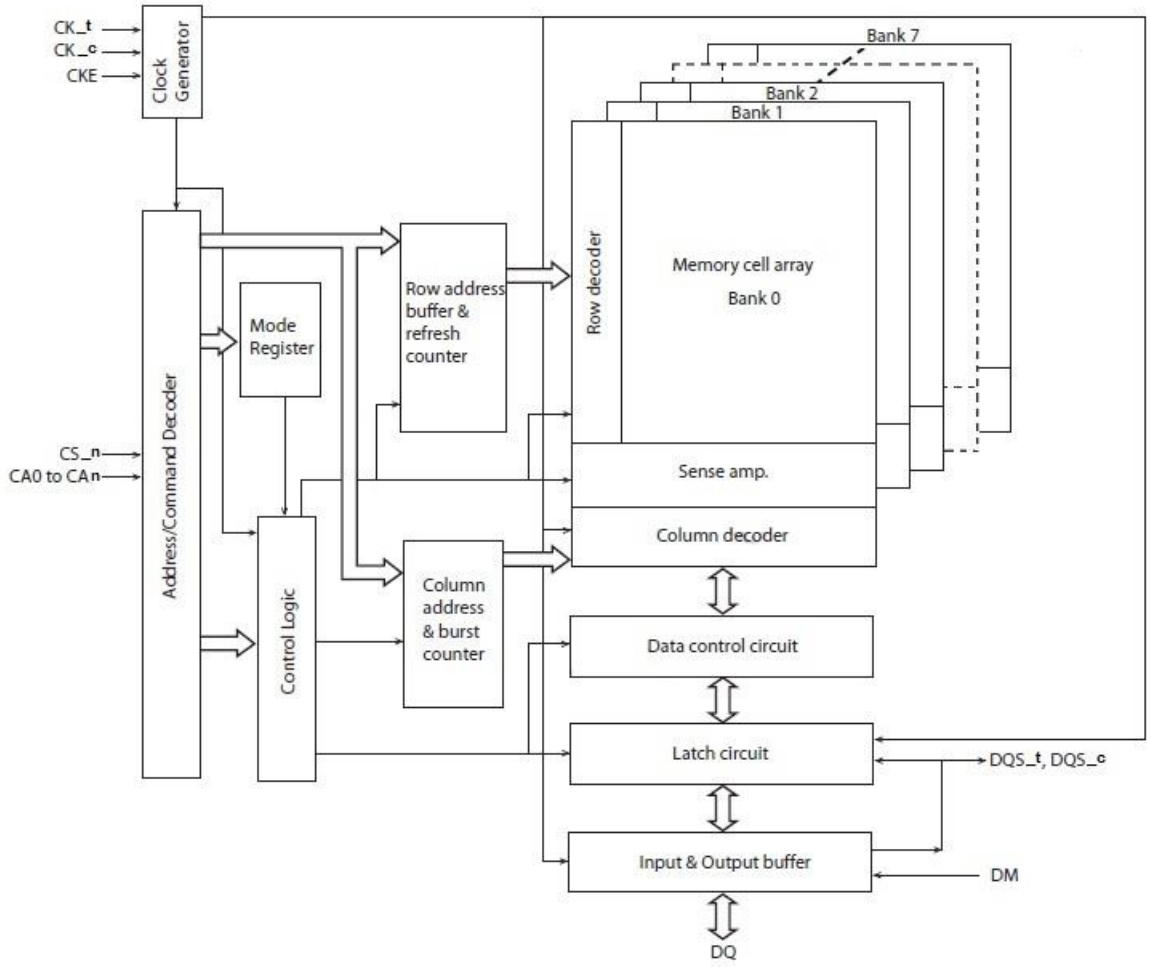
LPDDR2 SDRAM Addressing

Items	1Gb (32Mb x32)
Device Type	S4
Number of Banks	8
Bank Addresses	BA0-BA2
t_{REFI} (us) *2	7.8
Row Addresses	R0-R12
Column Addresses*1	C0-C8

Notes:

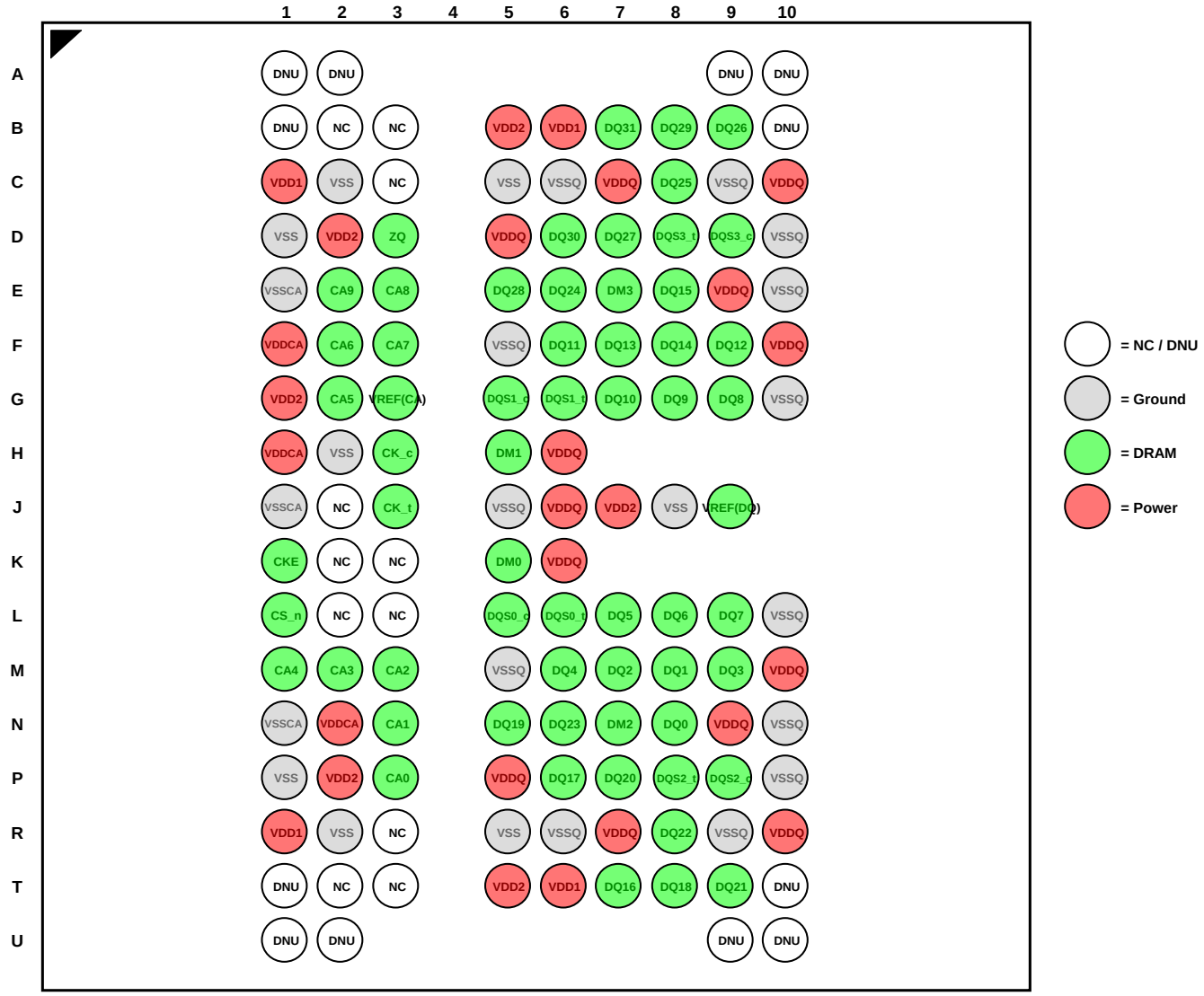
1. The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.
2. t_{REFI} values for all bank refresh is within temperature specification (T_{CASE} <= 85℃).
3. Row and Column Address values on the CA bus that are not used are “don’t care”.

Block Diagram



BALL CONFIGURATION (TOP VIEW)

(BGA 134 Ball, 10mmx11.5mmx1.0mm Body, 0.65mm Ball Pitch)



Ball Descriptions

Pin Name	Type	Function
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK_t. Single Data Rate (SDR) inputs, CS_n and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK_t and CK_c. The positive Clock edge is defined by the crosspoint of a rising CK_t and a falling CK_c. The negative Clock edge is defined by the crosspoint of a falling CK_t and a rising CK_c.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. CKE is sampled at the positive Clock edge.
CS_n	Input	**Chip Select:** CS_n is considered part of the command code and CS_n is sampled at the positive Clock edge.
CA[n:0]	Input	**DDR Command/Address Inputs:** Uni-directional command/address bus inputs. CA is considered part of the command code.
DQ[n:0]	I/O	**Data Inputs/Output:** Bi-directional data bus. n=31 for 32 bits DQ.
DQS[n:0]_t, DQS[n:0]_c	I/O	**Data Strobe (Bi-directional, Differential):** The data strobe is bi-directional (used for read and write data) and differential (DQS_t and DQS_c). It is output with read data and input with write data. DQS_t is edge-aligned to read data and centered with write data. DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7; DQS1_t and DQS1_c to the data on DQ8 - DQ15; DQS2_t and DQS2_c correspond to the data on DQ16 - DQ23; DQS3_t and DQS3_c to the data on DQ24 - DQ31.
DM[n:0]	Input	**Input Data Mask:** DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS_t. Although DM is for input only, the DM loading shall match the DQ and DQS_t (or DQS_c). DM0 is the input data mask signal for the data on DQ0-7, DM1 is the input data mask signal for the data on DQ8-15, DM2 is the input data mask signal for the data on DQ16-23, DM3 is the input data mask signal for the data on DQ24-31.

Pin Name	Type	Function
VDD1	Supply	**Core power supply 1:** Core power supply.
VDD2	Supply	**Core power supply 2:** Core power supply
VDDCA	Supply	**Input Receiver Power Supply:** Power supply for CA[n:0], CKE, CS_n, CK_t, and CK_c input buffers.
VDDQ	Supply	**I/O Power Supply:** Power supply for Data input/output buffers.
VREF(CA)	Supply	**Reference Voltage for CA Command and Control Input Receiver:** Reference voltage for all CA[n:0], CKE, CS_n, CK_t, and CK_c input buffers.
VREF(DQ)	Supply	**Reference Voltage for DQ Input Receiver:** Reference voltage for all Data input buffers.
VSS	Supply	**Ground.**
VSSCA	Supply	**Ground for Input Receivers.**
VSSQ	Supply	**I/O Ground.**
ZQ	I/O	**Reference Pin for Output Drive Strength Calibration.**
NC / DNU	-	No Connection / Do Not Use

Notes: Data includes DQ and DM.

Electrical Specifications

Absolute Maximum DC Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Parameter	Symbol	Min	Max	Unit	Notes
V_{DD1} supply voltage relative to V_{SS}	V_{DD1}	-0.4	+2.3	V	1
V_{DD2} supply voltage relative to V_{SS}	V_{DD2}	-0.4	+1.6	V	1
V_{DDCA} supply voltage relative to V_{SSCA}	V_{DDCA}	-0.4	+1.6	V	1, 2
V_{DDQ} supply voltage relative to V_{SSQ}	V_{DDQ}	-0.4	+1.6	V	1, 3
Voltage on any ball relative to V_{SS}	V_{IN}, V_{OUT}	-0.4	+1.6	V	
Storage Temperature	T_{STG}	-55	+125	°C	4

Notes:

1. See “Power Ramp” section.
2. $V_{REFCA} \leqq 0.6 \times V_{DDCA}$; however, V_{REFCA} may be $\geqq V_{DDCA}$ provided that $V_{REFCA} \leqq 300mV$.
3. $V_{REFDQ} \leqq 0.6 \times V_{DDQ}$; however, V_{REFDQ} may be $\geqq V_{DDQ}$ provided that $V_{REFDQ} \leqq 300mV$.
4. Storage Temperature is the case surface temperature on the center/top side of the LPDDR2 device. For the measurement conditions, please refer to JESD51-2 standard.

AC & DC Operating Conditions

Recommended DC Operating Conditions

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR2 Device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

Symbol	Min	Typ	Max	Power Supply	Unit
V_{DD1}	1.7	1.8	1.95	Core power 1	V
V_{DD2}	1.14	1.2	1.3	Core power 2	V
V_{DDCA}	1.14	1.2	1.3	Input buffer power	V
V_{DDQ}	1.14	1.2	1.3	I/O buffer power	V

Notes: V_{DD1} uses significantly less power than V_{DD2}.

Input Leakage Current

Parameter / Condition	Symbol	Min	Max	Unit	Note
Input Leakage current For CA, CKE, CS_n, CK_t, CK_c Any input 0V ≦ V_{IN} ≦ V_{DDCA} (All other pins not under test = 0V)	I_L	-2	2	uA	1
V_{REF} supply leakage current V_{REFDQ} = V_{DDQ}/2 or V_{REFCA} = V_{DDCA}/2 (All other pins not under test = 0V)	I_{VREF}	-1	1	uA	2

Notes:

1. Although DM is for input only, the DM leakage shall match the DQ and DQS_t/DQS_c output leakage specification.
2. The minimum limit requirement is for testing purposes. The leakage current on V_{REFCA} and V_{REFDQ} pins should be minimal.

Operating Temperature Range

Parameter / Condition	Symbol	Rating	Unit
Standard	T_{CASE}	-25 to +85	°C

Notes:

1. Operating temperature is the case surface temperature on the center/top side of the LPDDR2 device. For the measurement conditions, please refer to JESD51-2 standard.
2. Either the device case temperature rating or the temperature sensor may be used to set an appropriate refresh rate, determine the need for AC timing derating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the T_{CASE} rating that applies for the Operating Temperature Range. For example, T_{CASE} may be above 85°C when the temperature sensor indicates a temperature of less than 85°C.

AC and DC Input Measurement Levels

AC and DC Logic Input Levels for Single-Ended Signals

Single-Ended AC and DC Input Levels for CA and CS_n Inputs

Symbol	Parameter	Value		Unit	Note
		Min	Max		
$V_{IHCA(AC)}$	AC input logic high	V_{REF} + 0.220	Note 2	V	1,2
$V_{ILCA(AC)}$	AC input logic low	Note 2	V_{REF} - 0.220	V	1,2
$V_{IHCA(DC)}$	DC input logic high	V_{REF} + 0.130	V_{DDCA}	V	1
$V_{ILCA(DC)}$	DC input logic low	V_{SSCA}	V_{REF} - 0.130	V	1
$V_{REFCA(DC)}$	Reference Voltage for CA and CS_n inputs	0.49 * V_{DDCA}	0.51 * V_{DDCA}	V	3,4

Notes:
1. For CA and CS_n input only pins. $V_{REF} = V_{REFCA(DC)}$.
2. See “Overshoot and Undershoot Specifications” section.
3. The ac peak noise on V_{REFCA} may not allow V_{REFCA} to deviate from $V_{REFCA(DC)}$ by more than +/-1% V_{DDCA} (for reference: approx. +/- 12 mV).
4. For reference: approx. $V_{DDCA}/2$ +/- 12 mV.

Single-Ended AC and DC Input Levels for CKE

Symbol	Parameter	Min	Max	Unit	Note
V_{IHCKE}	CKE Input High Level	0.8 * V_{DDCA}	Note 1	V	1
V_{ILCKE}	CKE Input Low Level	Note 1	0.2 * V_{DDCA}	V	1

Note: See “Overshoot and Undershoot Specifications” section.

Single-Ended AC and DC Input Levels for DQ and DM

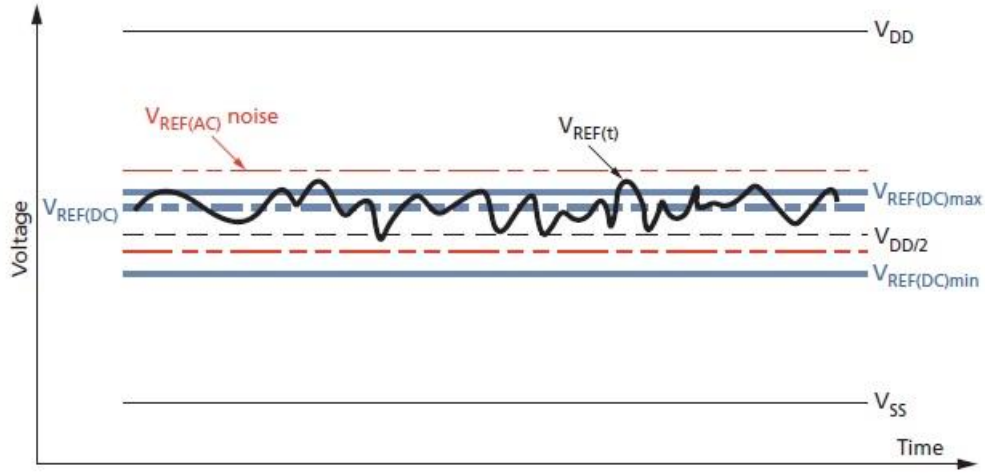
Symbol	Parameter	Value		Unit	Note
		Min	Max		
$V_{IHDQ(AC)}$	AC input logic high	V_{REF} + 0.220	Note 2	V	1,2
$V_{ILDQ(AC)}$	AC input logic low	Note 2	V_{REF} - 0.220	V	1,2
$V_{IHDQ(DC)}$	DC input logic high	V_{REF} + 0.130	V_{DDQ}	V	1
$V_{ILDQ(DC)}$	DC input logic low	V_{SSQ}	V_{REF} - 0.130	V	1
$V_{REFDQ(DC)}$	Reference Voltage for DQ, DM inputs	0.49 * V_{DDQ}	0.51 * V_{DDQ}	V	3,4

Notes:
1. For DQ input only pins. $V_{REF} = V_{REFDQ(DC)}$.
2. See “Overshoot and Undershoot Specifications” section.
3. The ac peak noise on V_{REFDQ} may not allow V_{REFDQ} to deviate from $V_{REFDQ(DC)}$ by more than +/-1% V_{DDQ} (for reference: approx. +/- 12 mV).
4. For reference: approx. $V_{DDQ}/2$ +/- 12 mV.

V_{REF} Tolerances

The DC tolerance limits and AC noise limits for the reference voltages V_{REFCA} and V_{REFDQ} are illustrated in the Figure below. It shows a valid reference voltage $V_{REF}(t)$ as a function of time. (V_{REF} stands for V_{REFCA} and V_{REFDQ} likewise). V_{DD} stands for V_{DDCA} for V_{REFCA} and V_{DDQ} for V_{REFDQ}. $V_{REF(DC)}$ is the linear average of $V_{REF}(t)$ over a very long period of time (e.g. 1 sec) and is specified as a fraction of the linear average of V_{DDQ} or V_{DDCA} also over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in Table of "Single-Ended AC and DC Input Levels for CA and CS_n Inputs". Furthermore $V_{REF}(t)$ may temporarily deviate from $V_{REF(DC)}$ by no more than +/- 1% V_{DD}. $V_{REF}(t)$ cannot track noise on V_{DDQ} or V_{DDCA} if this would send V_{REF} outside these specifications.

Figure of Illustration of V_{REF} DC tolerance and V_{REF} AC noise limits



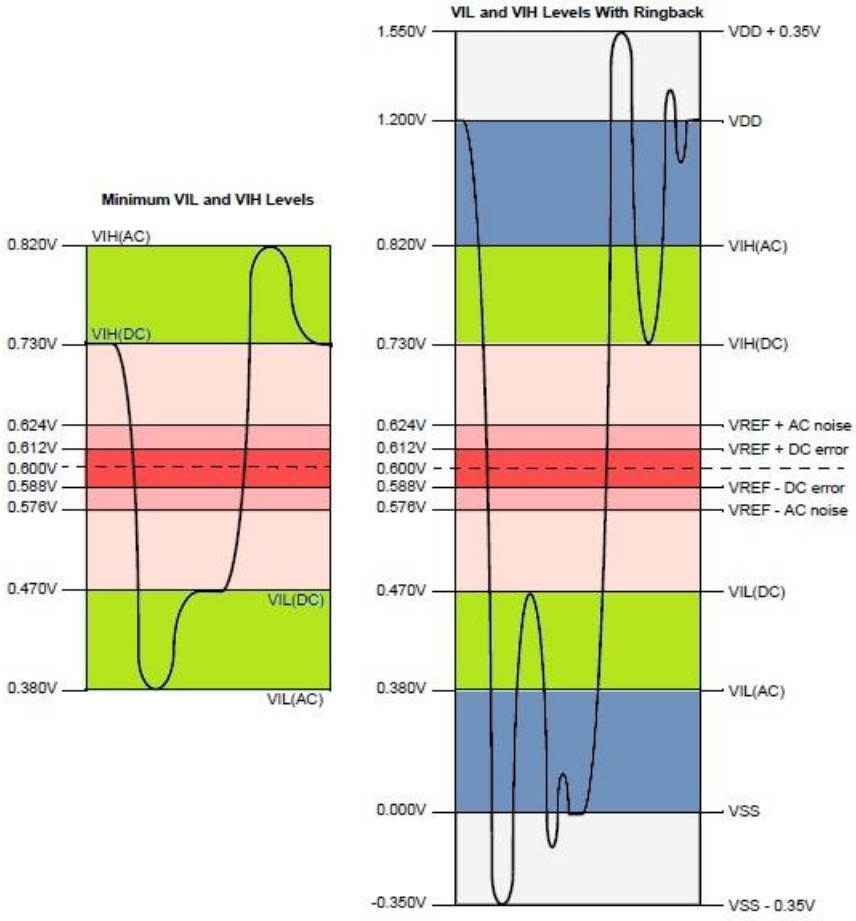
The voltage levels for setup and hold time measurements $V_{IH(AC)}$, $V_{IH(DC)}$, $V_{IL(AC)}$ and $V_{IL(DC)}$ are dependent on V_{REF}.
V_{REF} DC variations affect the absolute voltage a signal must reach to achieve a valid high or low level, as well as the time from which setup and hold times are measured. When V_{REF} is outside these specified levels, devices will function correctly with appropriate timing deratings as long as:

V_{REF} is maintained between 0.44 x V_{DDQ} (or V_{DDCA}) and 0.56 x V_{DDQ} (or V_{DDCA}) and so long as the controller achieves the required single-ended AC and DC input levels from instantaneous V_{REF} (see the Tables of "Single-Ended AC and DC Input Levels for CA and CS_n Inputs" and "Single-Ended AC and DC Input Levels for DQ and DM") Therefore, system timing and voltage budgets need to account for V_{REF} deviations outside of this range.

This also clarifies that the LPDDR2 setup/hold specification and derating values need to include time and voltage associated with V_{REF} AC noise. Timing and voltage effects due to AC noise on V_{REF} up to the specified limit (+/-1% of V_{DD}) are included in LPDDR2 timings and their associated deratings.

Input Signal

LPDDR2-466 to LPDDR2-1066 Input Signal



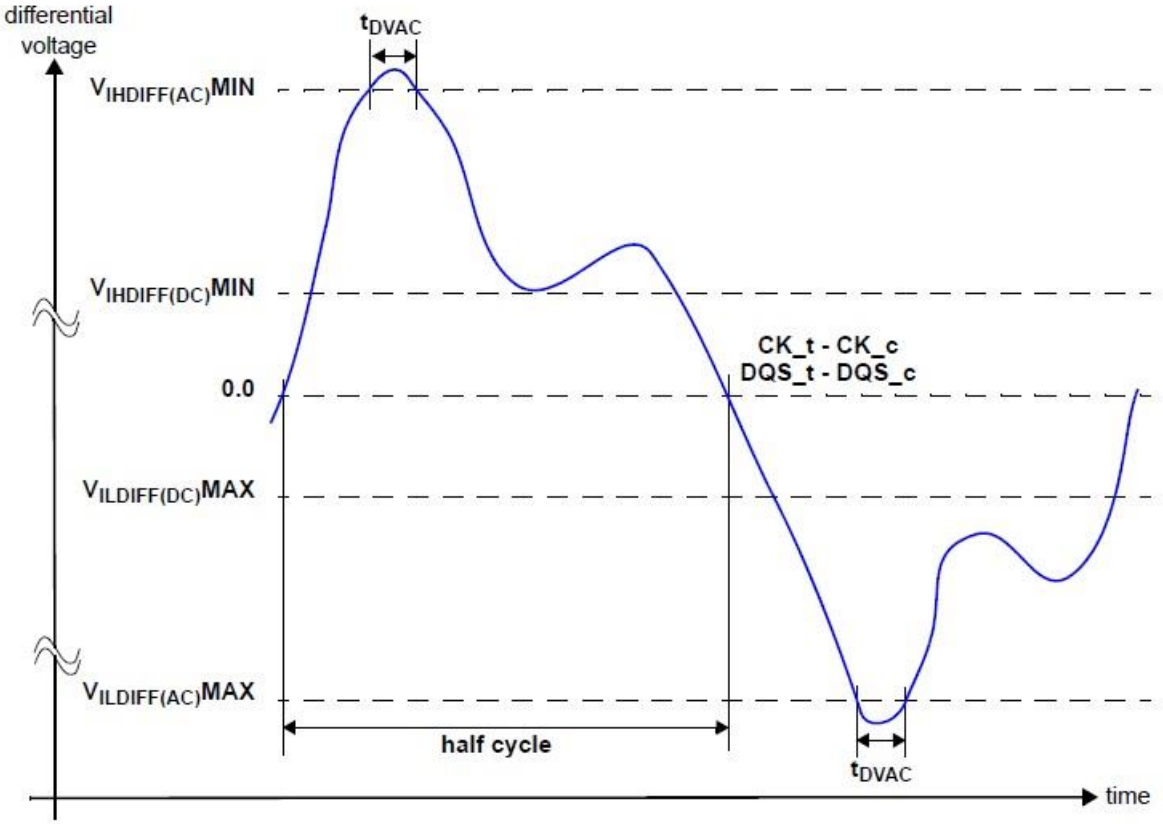
Notes:

1. Numbers reflect nominal values.
2. For CA0-9, CK_t, CK_c, and CS_n, V_{DD} stands for V_{DDCA}. For DQ, DM, DQS_t, and DQS_c, V_{DD} stands for V_{DDQ}.
3. For CA0-9, CK_t, CK_c, and CS_n, V_{SS} stands for V_{SSCA}. For DQ, DM, DQS_t, and DQS_c, V_{SS} stands for V_{SSQ}.

AC and DC Logic Input Levels for Differential Signals

Differential signal definition

Figure of Differential AC swing time and t_{DVAC}



Differential swing requirements for clock and strobe

Table of Differential AC and DC Input Levels

For CK_t and CK_c, $V_{REF} = V_{REFCA(DC)}$; For DQS_t and DQS_c, $V_{REF} = V_{REFDQ(DC)}$

Symbol	Parameter	Value		Unit	Note
		Min	Max		
$V_{IHDIFF(DC)}$	Differential input high	2x ($V_{IH(DC)}$ - V_{REF})	Note 1	V	3
$V_{ILDIFF(DC)}$	Differential input low	Note 1	2x (V_{REF} - $V_{IL(DC)}$)	V	3
$V_{IHDIFF(AC)}$	Differential input high AC	2x ($V_{IH(AC)}$ - V_{REF})	Note 1	V	2
$V_{ILDIFF(AC)}$	Differential input low AC	Note 1	2x (V_{REF} - $V_{IL(AC)}$)	V	2

Notes:

1. These values are not defined, however the single-ended signals CK_t, CK_c, DQS_t and DQS_c need to be within the respective limits ($V_{IH(DC)}$ max, $V_{IL(DC)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to “Overshoot and Undershoot Specifications” section.
2. For CK_t - CK_c use $V_{IH}/V_{IL(AC)}$ of CA and V_{REFCA}; for DQS_t and DQS_c, use $V_{IH}/V_{IL(AC)}$ of DQs and V_{REFDQ}. If a reduced AC high or AC low level is used for a signal group, the reduced level also applies.
3. Used to define a differential signal slew rate.

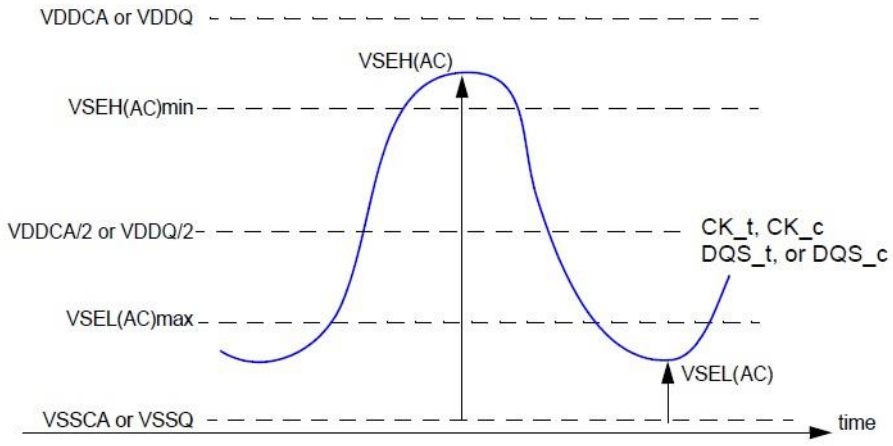
Table of Allowed time before ringback (t_{DVAC}) for CK_t - CK_c and DQS_t - DQS_c

Slew Rate [V/ns]	t_{DVAC} (ps) @ $\lvert V_{IH}/V_{ILDIFF(AC)}\rvert$ = 440mV	t_{DVAC} (ps) @ $\lvert V_{IH}/V_{ILDIFF(AC)}\rvert$ = 600mV
	Min	Min
> 4.0	175	75
4.0	170	57
3.0	167	50
2.0	163	38
1.8	162	34
1.6	161	29
1.4	159	22
1.2	155	13
1.0	150	0
< 1.0	150	0

Single-ended requirements for differential signals

Each individual component of a differential signal (CK_t, DQS_t, CK_c, or DQS_c) has also to comply with certain requirements for single-ended signals.
CK_t and CK_c shall meet $V_{SEH(AC)}$ min / $V_{SEL(AC)}$ max in every half-cycle.
DQS_t, DQS_c shall meet $V_{SEH(AC)}$ min / $V_{SEL(AC)}$ max in every half-cycle preceeding and following a valid transition.
Note that the applicable AC levels for CA and DQ's are different per speed-bin.

Figure of Single-ended requirement for differential signals



Note that while CA and DQ signal requirements are with respect to V_{REF}, the single-ended components of differential signals have a requirement with respect to $V_{DDQ}/2$ for DQS_t, DQS_c and $V_{DDCA}/2$ for CK_t, CK_c; this is nominally the same.

The transition of single-ended signals through the AC levels is used to measure setup time. For single-ended components of differential signals the requirement to reach $V_{SEL(AC)}$ max, $V_{SEH(AC)}$ min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

The signal ended requirements for CK_t, CK_c, DQS_t and DQS_c are found in Tables of "Single-Ended AC and DC Input Levels for CA and CS_n Inputs" and "Single-Ended AC and DC Input Levels for DQ and DM" respectively.

Table of Single-ended levels for CK_t, DQS_t, CK_c, DQS_c

Symbol	Parameter	Value		Unit	Note
		Min	Max		
$V_{SEH\ (AC)}$	Single-ended high-level for strobes	(V_{DDQ}/2) + 0.220	Note 3	V	1,2
	Single-ended high-level for CK_t, CK_c	(V_{DDCA}/2) + 0.220	Note 3	V	1,2
$V_{SEL\ (AC)}$	Single-ended low-level for strobes	Note 3	(V_{DDQ}/2) - 0.220	V	1,2
	Single-ended low-level for CK_t, CK_c	Note 3	(V_{DDCA}/2) - 0.220	V	1,2

Notes:

1. For CK_t, CK_c use $V_{SEH}/V_{SEL(AC)}$ of CA; for strobes (DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c) use $V_{IH}/V_{IL(AC)}$ of DQs.
2. $V_{IH(AC)}/V_{IL(AC)}$ for DQs is based on V_{REFDQ}; $V_{SEH(AC)}/V_{SEL(AC)}$ for CA is based on V_{REFCA}; if a reduced AC high or AC low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK_t, CK_c, DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c need to be within the respective limits ($V_{IH(DC)}$ max, $V_{IL(DC)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specifications" section.

Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK_t, CK_c and DQS_t, DQS_c) must meet the requirements in Table of "Single-ended levels for CK_t, DQS_t, CK_c, DQS_c". The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signals to the midlevel between of V_{DD} and V_{SS}.

Figure of V_{IX} Definition

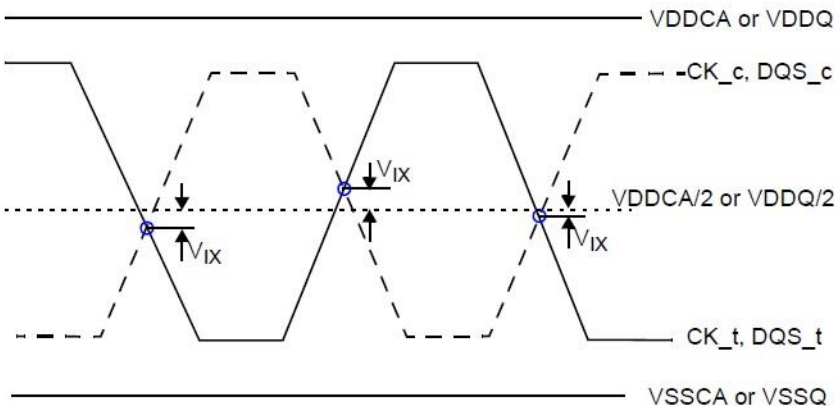


Table of Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	Value		Unit	Note
		Min	Max		
V_{IXCA}	Differential Input Cross Point Voltage relative to V_{DDCA}/2 for CK_t, CK_c	-120	120	mV	1,2
V_{IXDQ}	Differential Input Cross Point Voltage relative to V_{DDQ}/2 for DQS_t, DQS_c	-120	120	mV	1,2

Notes:

1. The typical value of $V_{IX(AC)}$ is expected to be about 0.5 × V_{DD} of the transmitting device, and $V_{IX(AC)}$ is expected to track variations in V_{DD}. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.
2. For CK_t and CK_c, V_{REF} = $V_{REFCA(DC)}$. For DQS_t and DQS_c, V_{REF} = $V_{REFDQ(DC)}$.

Slew Rate Definitions for Single-Ended Input Signals

See “CA and CS_n Setup, Hold and Derating” section for single-ended slew rate definitions for address and command signals.

See “Data Setup, Hold and Slew Rate Derating” section for single-ended slew rate definitions for data signals.

Slew Rate Definitions for Differential Input Signals

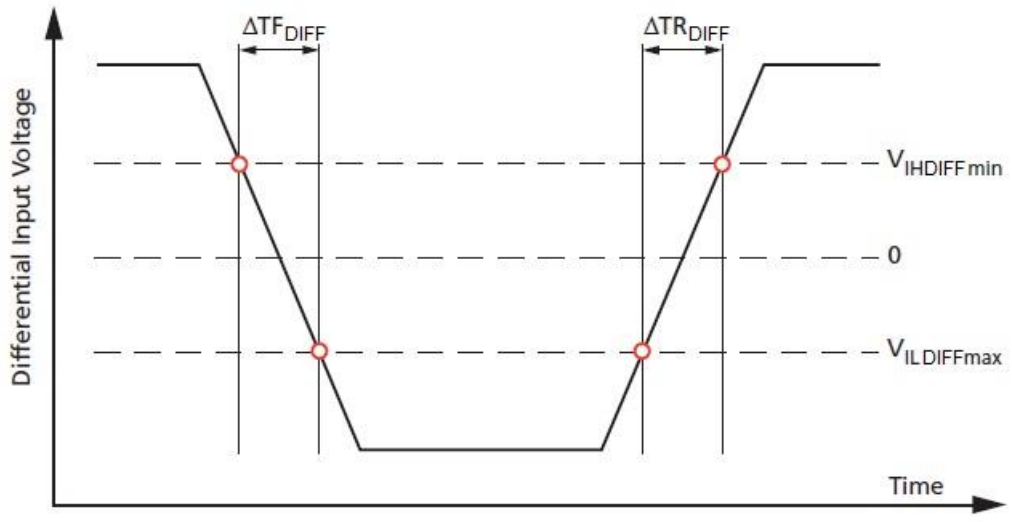
Input slew rate for differential signals (CK_t, CK_c and DQS_t, DQS_c) are defined and measured as shown in Table and Figure below.

Table of Differential Input Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge (CK_t - CK_c and DQS_t - DQS_c).	V_{ILDIFF} max	V_{IHDIFF} min	[V_{IHDIFF} min - V_{ILDIFF} max] / $\triangle TR_{DIFF}$
Differential input slew rate for falling edge (CK_t - CK_c and DQS_t - DQS_c).	V_{IHDIFF} min	V_{ILDIFF} max	[V_{IHDIFF} min – V_{IHDIFF} max] / $\triangle TF_{DIFF}$

Note: The differential signal (i.e. CK_t - CK_c and DQS_t - DQS_c) must be linear between these thresholds

Figure of Differential Input Slew Rate Definition for DQS_t, DQS_c and CK_t, CK_c



AC and DC Output Measurement Levels

Table of Single-Ended AC and DC Output Levels

Symbol	Parameter		Value	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)		0.9 x V_{DDQ}	V	1
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)		0.1 x V_{DDQ}	V	2
$V_{OH(AC)}$	AC output high measurement level (for output slew rate)		V_{REFDQ} + 0.12	V	
$V_{OL(AC)}$	AC output low measurement level (for output slew rate)		V_{REFDQ} - 0.12	V	
I_{OZ}	Output Leakage current (DQ, DM, DQS_t, DQS_c)	Min	-5	uA	
	(DQ, DQS_t, DQS_c are disabled; 0V ≦ V_{OUT} ≦ V_{DDQ}	Max	5	uA	
MM_{PUPD}	Delta R_{ON} between pull-up and pull-down for DQ/DM	Min	-15	%	
		Max	15	%	

Notes:

1. I_{OH} = -0.1 mA.
2. I_{OL} = 0.1 mA.

Table of Differential AC and DC Output Levels

Symbol	Parameter	Value	Unit
$V_{OHDIFF(AC)}$	AC differential output high measurement level (for output SR)	0.2 x V_{DDQ}	V
$V_{OLDIFF(AC)}$	AC differential output low measurement level (for output SR)	-0.2 x V_{DDQ}	V

Single-Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single-ended signals as shown in Table and Figure below.

Table of Single-Ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \triangle TR_{SE}$
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \triangle TF_{SE}$

Note: Output slew rate is verified by design and characterization, and may not be subject to production test.

Figure of Single-Ended Output Slew Rate Definition

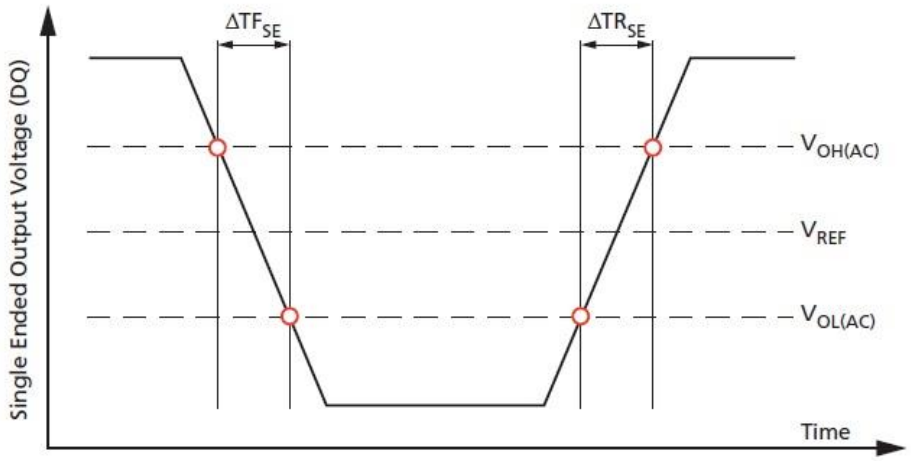


Table of Single-Ended Output Slew Rate *[1~5]

Parameter	Symbol	Value		Unit
		Min	Max	
Single-Ended Output Slew Rate (R_{ON} = 40 +/- 30%)	SRQ_{SE}	1.5	3.5	V/ns
Single-Ended Output Slew Rate (R_{ON} = 60 +/- 30%)	SRQ_{SE}	1.0	2.5	V/ns
Output Slew Rate Matching Ratio (pull-up to pull-down)		0.7	1.4	-

Notes:

1. Description: SR = Slew Rate; Q: Query Output (like in DQ, which stands for Data-in, Query-Output); SE: Single-Ended Signals
2. Measured with output reference load.
3. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
4. The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$.
5. Slew rates are measured under normal simultaneous switching output (SSO) conditions, with 1/2 of DQ signals per data byte driving logic-high and 1/2 of DQ signals per data byte driving logic-low.

Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OLDIFF(AC)}$ and $V_{OHDIFF(AC)}$ for differential signals as shown in Table and Figure below.

Table of Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	to	
Differential output slew rate for rising edge	$V_{OLDIFF(AC)}$	$V_{OHDIFF(AC)}$	$[V_{OHDIFF(AC)} - V_{OLDIFF(AC)}] / \triangle TR_{DIFF}$
Differential output slew rate for falling edge	$V_{OHDIFF(AC)}$	$V_{OLDIFF(AC)}$	$[V_{OHDIFF(AC)} - V_{OLDIFF(AC)}] / \triangle TF_{DIFF}$

Note: Output slew rate is verified by design and characterization, and may not be subject to production test.

Figure of Differential Output Slew Rate Definition

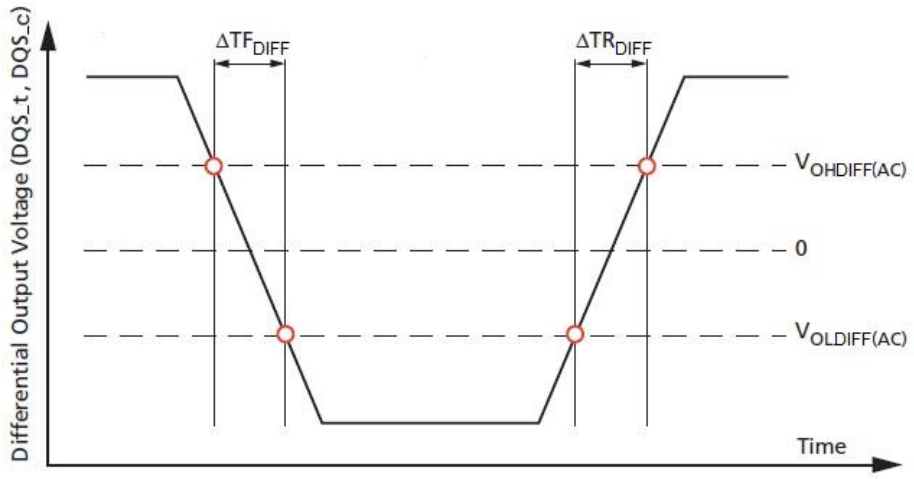


Table of Differential Output Slew Rate *1~4

Parameter	Symbol	Value		Unit
		Min	Max	
Differential Output Slew Rate (R_{ON} = 40 +/- 30%)	SRQ_{DIFF}	3.0	7.0	V/ns
Differential Output Slew Rate (R_{ON} = 60 +/- 30%)	SRQ_{DIFF}	2.0	5.0	V/ns

Notes:

1. Description: SR = Slew Rate; Q: Query Output (like in DQ, which stands for Data-in, Query-Output); DIFF: Differentia Signals
2. Measured with output reference load.
3. The output slew rate for falling and rising edges is defined and measured between $V_{OLDIFF(AC)}$ and $V_{OHDIFF(AC)}$.
4. Slew rates are measured under normal simultaneous switching output (SSO) conditions, with 1/2 of DQ signals per data byte driving logic-high and 1/2 of DQ signals per data byte driving logic-low.

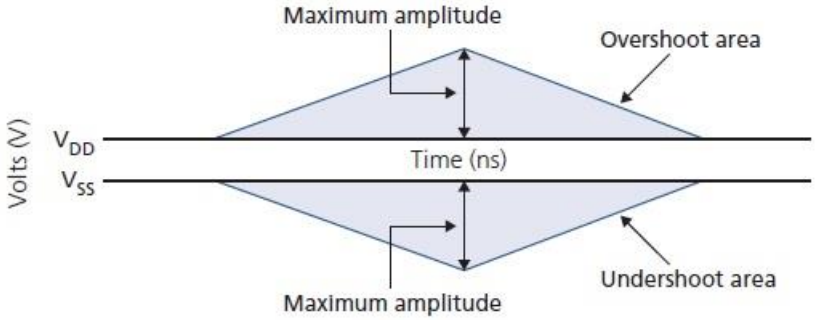
AC Overshoot/Undershoot Specification

Parameter		1066	800	Unit
Maximum peak amplitude allowed for overshoot area.	Max	0.35		V
Maximum peak amplitude allowed for undershoot area.	Max	0.35		V
Maximum area above V_{DD}[1].	Max	0.15	0.20	V-ns
Maximum area below V_{SS}[2].	Max	0.15	0.20	V-ns

(CA0-9, CS_n, CKE, CK_t, CK_c, DQ, DQS_t, DQS_c, DM)

Notes:
1. For CA0-9, CK_t, CK_c, CS_n, and CKE, V_{DD} stands for V_{DDCA}. For DQ, DM, DQS_t, and DQS_c, V_{DD} stands for V_{DDQ}.
2. For CA0-9, CK_t, CK_c, CS_n, and CKE, V_{SS} stands for V_{SSCA}. For DQ, DM, DQS_t, and DQS_c, V_{SS} stands for V_{SSQ}.

Figure of Overshoot/Undershoot Definition



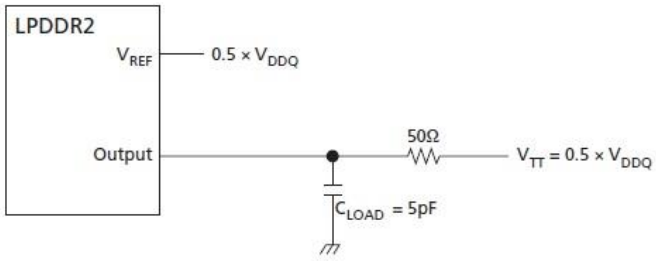
Notes:
1. For CA0-9, CK_t, CK_c, CS_n, and CKE, V_{DD} stands for V_{DDCA}. For DQ, DM, DQS_t, and DQS_c, V_{DD} stands for V_{DDQ}.
2. For CA0-9, CK_t, CK_c, CS_n, and CKE, V_{SS} stands for V_{SSCA}. For DQ, DM, DQS_t, and DQS_c, V_{SS} stands for V_{SSQ}.

Output buffer characteristics

HSUL_12 Driver Output Timing Reference Load

These “Timing Reference Loads” are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

Figure of HSUL_12 Driver Output Reference Load for Timing and Slew Rate



Note: All output timing parameter values (like t_{DQSCK}, t_{DQSQ}, t_{QHS}, t_{HZ}, t_{RPRE} etc.) are reported with respect to this reference load. This reference load is also used to report slew rate.

R_{ONPU} and R_{ONPD} Resistor Definition

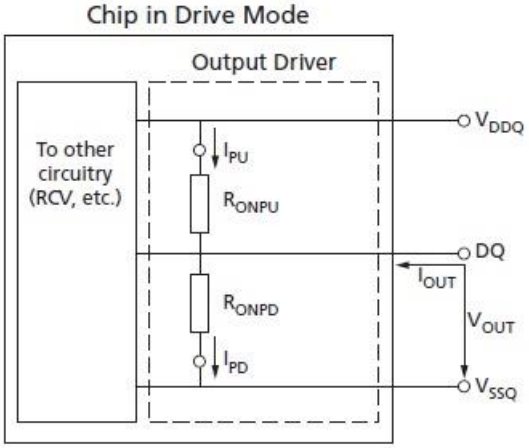
$$R_{ONPU} = \frac{V_{DDQ} - V_{OUT}}{ABS(I_{OUT})}$$

When R_{ONPU} is turned off.

$$R_{ONPD} = \frac{V_{OUT}}{ABS(I_{OUT})}$$

When R_{ONPD} is turned off.

Figure of Output Driver: Definition of Voltages and Currents



R_{ONPU} and R_{ONPD} Characteristics with ZQ Calibration

Output driver impedance R_{ON} is defined by the value of the external reference resistor R_{ZQ}. Nominal R_{ZQ} is 240 ohm.

Table of Output Driver DC Electrical Characteristics with ZQ Calibration

$R_{ON, nom}$	Resistor	V_{OUT}	Min	Nom	Max	Unit	Notes
34.3 Ω	R_{ON34PD}	0.5 x V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/7	1,2,3,4
	R_{ON34PU}	0.5 x V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/7	1,2,3,4
40.0 Ω	R_{ON40PD}	0.5 x V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/6	1,2,3,4
	R_{ON40PU}	0.5 x V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/6	1,2,3,4
48.0 Ω	R_{ON48PD}	0.5 x V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/5	1,2,3,4
	R_{ON48PU}	0.5 x V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/5	1,2,3,4
60.0 Ω	R_{ON60PD}	0.5 x V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/4	1,2,3,4
	R_{ON60PU}	0.5 x V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/4	1,2,3,4
80.0 Ω	R_{ON80PD}	0.5 x V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/3	1,2,3,4
	R_{ON80PU}	0.5 x V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/3	1,2,3,4
120.0 Ω	$R_{ON120PD}$	0.5 x V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/2	1,2,3,4
	$R_{ON120PU}$	0.5 x V_{DDQ}	0.85	1.00	1.15	R_{ZQ}/2	1,2,3,4
Mismatch between pull-up and pull-down	MM_{PUPD}		-15.00		+15.00	%	1,2,3,4,5

Notes:

1. Applies across entire operating temperature range, after calibration.
2. R_{ZQ} = 240 ohm.
3. The tolerance limits are specified after calibration with fixed voltage and temperature. For behavior of the tolerance limits if temperature or voltage changes after calibration.
4. Pull-down and pull-up output driver impedances should be calibrated at 0.5 x V_{DDQ}.
5. Measurement definition for mismatch between pull-up and pull-down, MM_{PUPD}: Measure R_{ONPU} and R_{ONPD}, both at 0.5 x V_{DDQ}:

$$MM_{PUPD} = \frac{R_{ONPU} - R_{ONPD}}{R_{ON, nom}} \times 100$$

For example, with MM_{PUPD}(max) = 15% and R_{ONPD} = 0.85, R_{ONPU} must be less than 1.0.

Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the Tables shown below.

Table of Output Driver Sensitivity Definition

Resistor	V_{OUT}	Min	Max	Unit
R_{ONPD}	0.5 x V_{DDQ}	85 – ($dR_{ON}dT$ x |ΔT|) – ($dR_{ON}dV$ x |ΔV|)	115 + ($dR_{ON}dT$ x |ΔT|) + ($dR_{ON}dV$ x |ΔV|)	%
R_{ONPU}				

Notes:

1. ΔT = T-T (@ calibration), ΔV =V-V (@ calibration)
2. $dR_{ON}dT$ and $dR_{ON}dV$ are not subject to production test but are verified by design and characterization.

Table of Output Driver Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit
$dR_{ON}dT$	R_{ON} Temperature Sensitivity	0.00	0.75	% / C
$dR_{ON}dV$	R_{ON} Voltage Sensitivity	0.00	0.20	% / mV

R_{ONPU} and R_{ONPD} Characteristics without ZQ Calibration

Output driver impedance R_{ON} is defined by design and characterization as default setting.

Table of Output Driver DC Electrical Characteristics without ZQ Calibration

$R_{ON, nom}$	Resistor	V_{OUT}	Min	Nom	Max	Unit	Notes
34.3 Ω	R_{ON34PD}	0.5 x V_{DDQ}	24	34.3	44.6	Ω	1
	R_{ON34PU}	0.5 x V_{DDQ}	24	34.3	44.6	Ω	1
40.0 Ω	R_{ON40PD}	0.5 x V_{DDQ}	28	40	52	Ω	1
	R_{ON40PU}	0.5 x V_{DDQ}	28	40	52	Ω	1
48.0 Ω	R_{ON48PD}	0.5 x V_{DDQ}	33.6	48	62.4	Ω	1
	R_{ON48PU}	0.5 x V_{DDQ}	33.6	48	62.4	Ω	1
60.0 Ω	R_{ON60PD}	0.5 x V_{DDQ}	42	60	78	Ω	1
	R_{ON60PU}	0.5 x V_{DDQ}	42	60	78	Ω	1
80.0 Ω	R_{ON80PD}	0.5 x V_{DDQ}	56	80	104	Ω	1
	R_{ON80PU}	0.5 x V_{DDQ}	56	80	104	Ω	1
120.0 Ω	$R_{ON120PD}$	0.5 x V_{DDQ}	84	120	156	Ω	1
	$R_{ON120PU}$	0.5 x V_{DDQ}	84	120	156	Ω	1

Note: 1. Applies across entire operating temperature range, without calibration.

R_{ZQ} I-V Curve

Voltage [V]	R_{ON} = 240 (R_{ZQ})							
	Pull-Down				Pull-Up			
	Current [mA] / R_{ON} [Ohms]				Current [mA] / R_{ON} [Ohms]			
	default value after ZQReset		with Calibration		default value after ZQReset		with Calibration	
	Min	Max	Min	Max	Min	Max	Min	Max
	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]
0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
0.05	0.19	0.32	0.21	0.26	-0.19	-0.32	-0.21	-0.26
0.10	0.38	0.64	0.40	0.53	-0.38	-0.64	-0.40	-0.53
0.15	0.56	0.94	0.60	0.78	-0.56	-0.94	-0.60	-0.78
0.20	0.74	1.26	0.79	1.04	-0.74	-1.26	-0.79	-1.04
0.25	0.92	1.57	0.98	1.29	-0.92	-1.57	-0.98	-1.29
0.30	1.08	1.86	1.17	1.53	-1.08	-1.86	-1.17	-1.53
0.35	1.25	2.17	1.35	1.79	-1.25	-2.17	-1.35	-1.79
0.40	1.40	2.46	1.52	2.03	-1.40	-2.46	-1.52	-2.03
0.45	1.54	2.74	1.69	2.26	-1.54	-2.74	-1.69	-2.26
0.50	1.68	3.02	1.86	2.49	-1.68	-3.02	-1.86	-2.49
0.55	1.81	3.30	2.02	2.72	-1.81	-3.30	-2.02	-2.72
0.60	1.92	3.57	2.17	2.94	-1.92	-3.57	-2.17	-2.94
0.65	2.02	3.83	2.32	3.15	-2.02	-3.83	-2.32	-3.15
0.70	2.11	4.08	2.46	3.36	-2.11	-4.08	-2.46	-3.36
0.75	2.19	4.31	2.58	3.55	-2.19	-4.31	-2.58	-3.55
0.80	2.25	4.54	2.70	3.74	-2.25	-4.54	-2.70	-3.74
0.85	2.30	4.74	2.81	3.91	-2.30	-4.74	-2.81	-3.91
0.90	2.34	4.92	2.89	4.05	-2.34	-4.92	-2.89	-4.05
0.95	2.37	5.08	2.97	4.23	-2.37	-5.08	-2.97	-4.23
1.00	2.41	5.20	3.04	4.33	-2.41	-5.20	-3.04	-4.33
1.05	2.43	5.31	3.09	4.44	-2.43	-5.31	-3.09	-4.44
1.10	2.46	5.41	3.14	4.52	-2.46	-5.41	-3.14	-4.52
1.15	2.48	5.48	3.19	4.59	-2.48	-5.48	-3.19	-4.59
1.20	2.50	5.55	3.23	4.65	-2.50	-5.55	-3.23	-4.65

Figure of R_{ON} = 240 Ohms IV Curve after ZQReset

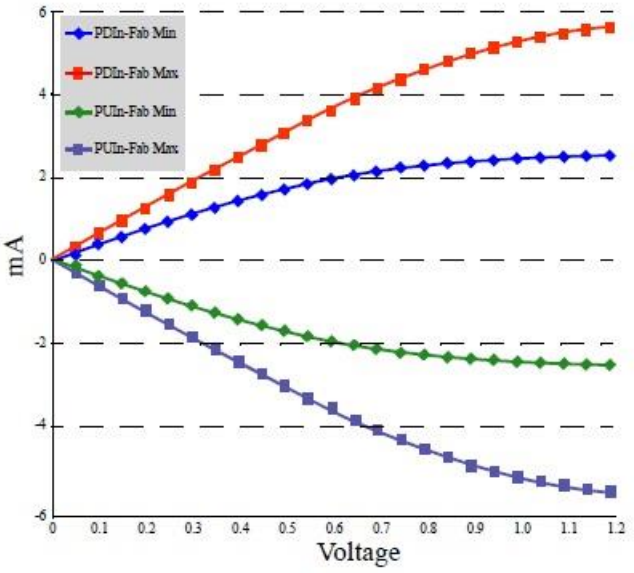
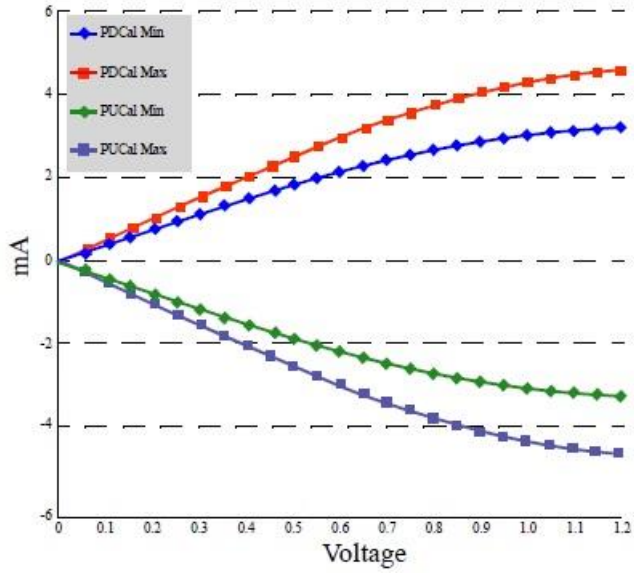


Figure of R_{ON} = 240 Ohms IV Curve after calibration



Input/Output Capacitance

(T_{CASE}, V_{DD1} = 1.7V to 1.95V, $V_{DD2}/V_{DDCA}/V_{DDQ}$ = 1.14V to 1.3V, $V_{SS}/V_{SSCA}/V_{SSQ}$ = 0V)

Parameter	Symbol		Value	Unit	Note
Input capacitance, CK_t and CK_c	CCK	Min	1.0	pF	1,2
		Max	2.0	pF	1,2
Input capacitance delta, CK_t and CK_c	CDCK	Min	0	pF	1,2,3
		Max	0.20	pF	1,2,3
Input capacitance, all other input-only pins	CI	Min	1.0	pF	1,2,4
		Max	2.0	pF	1,2,4
Input capacitance delta, all other input-only pins	CDI	Min	-0.40	pF	1,2,5
		Max	0.40	pF	1,2,5
Input/output capacitance, DQ, DM, DQS_t, DQS_c	CIO	Min	1.25	pF	1,2,6,7
		Max	2.5	pF	1,2,6,7
Input/output capacitance delta, DQS_t, DQS_c	CDDQS	Min	0	pF	1,2,7,8
		Max	0.25	pF	1,2,7,8
Input/output capacitance delta, DQ, DM	CDIO	Min	-0.5	pF	1,2,7,9
		Max	0.5	pF	1,2,7,9
Input/output capacitance ZQ Pin	CZQ	Min	0	pF	1,2
		Max	2.5	pF	1,2

Notes:

1. This parameter applies to die device only (does not include package capacitance).
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with V_{DD1}, V_{DD2}, V_{DDQ}, V_{SS}, V_{SSCA}, V_{SSQ} applied and all other pins floating.
3. Absolute value of CCK_t - CCK_c.
4. CI applies to CS_n, CKE, CA0-CA9.
5. CDI = CI - 0.5 * (CCK_t + CCK_c)
6. DM loading matches DQ and DQS.
7. MR3 I/O configuration DS OP3-OP0 = 0001B (34.3 Ohm typical)
8. Absolute value of CDQS_t and CDQS_c.
9. CDIO = CIO - 0.5 * (CDQS_t + CDQS_c) in byte-lane.

IDD Specification Parameters and Test Conditions

IDD Measurement Conditions

The following definitions are used within the IDD measurement tables:

- LOW: $V_{IN} \leqq V_{IL(DC)}$ MAX
- HIGH: $V_{IN} \geqq V_{IH(DC)}$ MIN
- STABLE: Inputs are stable at a HIGH or LOW level
- SWITCHING: See the following three tables

Table of Definition of Switching for CA Input Signals

Switching for CA								
	CK_t (RISING) / CK_c (FALLING)	CK_t (FALLING) / CK_c (RISING)	CK_t (RISING) / CK_c (FALLING)	CK_t (FALLING) / CK_c (RISING)	CK_t (RISING) / CK_c (FALLING)	CK_t (FALLING) / CK_c (RISING)	CK_t (RISING) / CK_c (FALLING)	CK_t (FALLING) / CK_c (RISING)
Cycle	**N**		**N+1**		**N+2**		**N+3**	
CS_n	HIGH		HIGH		HIGH		HIGH	
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA6	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA7	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA8	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA9	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

Notes:
1. CS_n must always be driven HIGH.
2. 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
3. The above pattern (N, N+1, N+2, N+3...) is used continuously during IDD measurement for IDD values that require SWITCHING on the CA bus.

Table of Definition of Switching for IDD4R

Clock	CKE	CS_n	Clock Cycle Number	Command	CA0-CA2	CA3-CA9	All DQ
Rising	HIGH	LOW	N	Read_Rising	HLH	LHLHLHL	L
Falling	HIGH	LOW	N	Read_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N + 1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N + 1	NOP	HLH	HLHLLHL	L
Rising	HIGH	LOW	N + 2	Read_Rising	HLH	HLHLLHL	H
Falling	HIGH	LOW	N + 2	Read_Falling	LLL	HHHHHHH	H
Rising	HIGH	HIGH	N + 3	NOP	LLL	HHHHHHH	H
Falling	HIGH	HIGH	N + 3	NOP	HLH	LHLHLHL	L

Notes:

1. Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
2. The above pattern (N, N+1...) is used continuously during IDD measurement for IDD4R.

Table of Definition of Switching for IDD4W

Clock	CKE	CS_n	Clock Cycle Number	Command	CA0-CA2	CA3-CA9	All DQ
Rising	HIGH	LOW	N	Write_Rising	HLL	LHLHLHL	L
Falling	HIGH	LOW	N	Write_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N + 1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N + 1	NOP	HLH	HLHLLHL	L
Rising	HIGH	LOW	N + 2	Write_Rising	HLL	HLHLLHL	H
Falling	HIGH	LOW	N + 2	Write_Falling	LLL	HHHHHHH	H
Rising	HIGH	HIGH	N + 3	NOP	LLL	HHHHHHH	H
Falling	HIGH	HIGH	N + 3	NOP	HLH	LHLHLHL	L

Notes:

1. Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
2. Data masking (DM) must always be driven LOW.
3. The above pattern (N, N+1...) is used continuously during IDD measurement for IDD4W.

IDD Specifications

IDD values are for the entire operating voltage range, and all of them are for the entire standard range, with the exception of IDD6ET which is for the entire extended temperature range.

Table of IDD Specification Parameters and Operating Conditions

Parameter / Test Condition	Symbol	Power Supply	Max		Unit	Note
			1066	800		
Operating one bank active-precharge current: $t_{CK} = t_{CK(avg)}$ min; $t_{RC} = t_{RC}$min; CKE is HIGH; CS_n is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD0_1$	V_{DD1}	5	5	mA	3
	$IDD0_2$	V_{DD2}	22	22	mA	3
	$IDD0_{IN}$	V_{DDCA}, V_{DDQ}	4	4	mA	3,4
Idle power down standby current: $t_{CK} = t_{CK(avg)}$min; CKE is LOW; CS_n is HIGH; All banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD2P_1$	V_{DD1}	0.7	0.7	mA	3
	$IDD2P_2$	V_{DD2}	1.5	1.5	mA	3
	$IDD2P_{IN}$	V_{DDCA}, V_{DDQ}	50	50	uA	3,4
Idle power down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CKE is LOW; CS_n is HIGH; All banks idle; CA bus inputs are STABLE; Data bus inputs are STABLE	$IDD2PS_1$	V_{DD1}	0.7	0.7	mA	3
	$IDD2PS_2$	V_{DD2}	1.5	1.5	mA	3
	$IDD2PS_{IN}$	V_{DDCA}, V_{DDQ}	50	50	uA	3,4
Idle non power down standby current: $t_{CK} = t_{CK\ (avg)}$min; CKE is HIGH; CS_n is HIGH; All banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD2N_1$	V_{DD1}	1.2	1.2	mA	3
	$IDD2N_2$	V_{DD2}	15	15	mA	3
	$IDD2N_{IN}$	V_{DDCA}, V_{DDQ}	1	1	mA	3,4
Idle non power down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CKE is HIGH; CS_n is HIGH; All banks idle; CA bus inputs are STABLE; Data bus inputs are STABLE	$IDD2NS_1$	V_{DD1}	1.2	1.2	mA	3
	$IDD2NS_2$	V_{DD2}	10	10	mA	3
	$IDD2NS_{IN}$	V_{DDCA}, V_{DDQ}	1	1	mA	3,4
Active power down standby current: $t_{CK} = t_{CK(avg)}$min; CKE is LOW; CS_n is HIGH; One bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD3P_1$	V_{DD1}	1.2	1.2	mA	3
	$IDD3P_2$	V_{DD2}	2	2	mA	3
	$IDD3P_{IN}$	V_{DDCA}, V_{DDQ}	50	50	uA	3,4
Active power down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CKE is LOW; CS_n is HIGH; One bank active; CA bus inputs are STABLE; Data bus inputs are STABLE	$IDD3PS_1$	V_{DD1}	1.2	1.2	mA	3
	$IDD3PS_2$	V_{DD2}	2	2	mA	3
	$IDD3PS_{IN}$	V_{DDCA}, V_{DDQ}	50	50	uA	3,4
Active non power down standby current: $t_{CK} = t_{CK(avg)}$min; CKE is HIGH; CS_n is HIGH; One bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD3N_1$	V_{DD1}	2	2	mA	3
	$IDD3N_2$	V_{DD2}	15	15	mA	3
	$IDD3N_{IN}$	V_{DDCA}, V_{DDQ}	5	5	mA	3,4

Parameter / Test Condition	Symbol	Power Supply	Max		Unit	Note
			1066	800		
Active non power down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CKE is HIGH; CS_n is HIGH; One bank active; CA bus inputs are STABLE; Data bus inputs are STABLE	$IDD3NS_1$	V_{DD1}	2	2	mA	3
	$IDD3NS_2$	V_{DD2}	10	10	mA	3
	$IDD3NS_{IN}$	V_{DDCA}, V_{DDQ}	4	4	mA	3,4
Operating burst READ current: $t_{CK} = t_{CK(avg)}$min; CS_n is HIGH between valid commands; One bank active; BL = 4; RL = RL(min); CA bus inputs are SWITCHING; 50% data change each burst transfer	$IDD4R_1$	V_{DD1}	1.8	1.8	mA	3
	$IDD4R_2$	V_{DD2}	110	90	mA	3
	$IDD4R_{IN}$	V_{DDCA}	7	7	mA	3
	$IDD4R_Q$	V_{DDQ}	260	250	mA	3,5
Operating burst WRITE current: $t_{CK} = t_{CK(avg)}$min; CS_n is HIGH between valid commands; One bank active; BL = 4; WL = WL(min); CA bus inputs are SWITCHING; 50% data change each burst transfer	$IDD4W_1$	V_{DD1}	1.8	1.8	mA	3
	$IDD4W_2$	V_{DD2}	100	85	mA	3
	$IDD4W_{IN}$	V_{DDCA}, V_{DDQ}	14	14	mA	3,4
All Bank REFRESH Burst current: $t_{CK} = t_{CK(avg)}$min; CKE is HIGH between valid commands; $t_{RC} = t_{RFCab}$ min; Burst refresh; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD5_1$	V_{DD1}	10	10	mA	3
	$IDD5_2$	V_{DD2}	38	38	mA	3
	$IDD5_{IN}$	V_{DDCA}, V_{DDQ}	4	4	mA	3,4
All Bank REFRESH Average current: $t_{CK} = t_{CK(avg)}$min; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}$; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD5AB_1$	V_{DD1}	1	1	mA	3
	$IDD5AB_2$	V_{DD2}	11	11	mA	3
	$IDD5AB_{IN}$	V_{DDCA}, V_{DDQ}	4	4	mA	3,4
Per Bank REFRESH Average current: $t_{CK} = t_{CK(avg)}$min; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}$ / 8; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD5PB_1$	V_{DD1}	1	1	mA	1,3
	$IDD5PB_2$	V_{DD2}	15	15	mA	1,3
	$IDD5PB_{IN}$	V_{DDCA}, V_{DDQ}	4	4	mA	1,3,4
Self refresh current (Standard Temperature Range): CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE; Maximum 1x Self Refresh Rate	$IDD6_1$	V_{DD1}	0.8	0.8	mA	2,3,7,8
	$IDD6_2$	V_{DD2}	2	2	mA	2,3,7,8
	$IDD6_{IN}$	V_{DDCA}, V_{DDQ}	50	50	uA	2,3,4 7,8

Parameter / Test Condition	Symbol	Power Supply	Max		Unit	Note
			1066	800		
Deep power down current: CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE	$IDD8_1$	V_{DD1}	30	30	uA	3
	$IDD8_2$	V_{DD2}	150	150	uA	3
	$IDD8_{IN}$	V_{DDCA}, V_{DDQ}	50	50	uA	3,4

Notes:
1. Per Bank Refresh only applicable for LPDDR2-S4 devices of 1Gb or higher densities.
2. This is the general definition that applies to full array Self Refresh. Refer to Table of "IDD6 Partial Array Self Refresh Current".
3. IDD values published are the maximum of the distribution of the arithmetic mean.
4. Measured currents are the summation of V_{DDQ} and V_{DDCA}.
5. Guaranteed by design with output load of 5pF and R_{ON} = 40Ohm.
6. IDD current specifications are tested after the device is properly initialized.
7. In addition, supplier data sheets may include additional Self Refresh IDD values for temperature subranges within the Standard Temperature Ranges.
8. 1x Self Refresh Rate is the rate at which the LPDDR2-SX device is refreshed internally during Self Refresh before going into the Extended Temperature range.
9. IDD6ET is a typical value, is sampled only and is not tested.

Table of IDD6 Partial Array Self Refresh Current

Parameter		Supply	Value	Unit
IDD6 Partial Array Self Refresh Current	Full Array	V_{DD1}	0.8	mA
		V_{DD2}	2	mA
		V_{DDCA}, V_{DDQ}	50	uA
	1/2 Array	V_{DD1}	0.75	mA
		V_{DD2}	1.8	mA
		V_{DDCA}, V_{DDQ}	50	uA
	1/4 Array	V_{DD1}	0.7	mA
		V_{DD2}	1.6	mA
		V_{DDCA}, V_{DDQ}	50	uA
	1/8 Array	V_{DD1}	0.65	mA
		V_{DD2}	1.5	mA
		V_{DDCA}, V_{DDQ}	50	uA

Electrical Characteristics and AC Timing

Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the LPDDR2 device.

Definition for $t_{CK(avg)}$ and nCK

$t_{CK(avg)}$ is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$t_{CK\,(avg)} = \left(\sum_{j=1}^{N} t_{CKj} \right) / N$$

where $N = 200$

Unit '$t_{CK(avg)}$' represents the actual clock average $t_{CK(avg)}$ of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.
$t_{CK(avg)}$ may change by up to +/-1% within a 100 clock cycle window, provided that all jitter and timing specs are met.

Definition for $t_{CK(abs)}$

$t_{CK(abs)}$ is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge.
$t_{CK(abs)}$ is not subject to production test.

Definition for $t_{CH(avg)}$ and $t_{CL(avg)}$

$t_{CH(avg)}$ is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$t_{CH\,(avg)} = \left(\sum_{j=1}^{N} t_{CHj} \right) / (N \times t_{CK\,(avg)})$$

where $N = 200$

$t_{CL(avg)}$ is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$t_{CL\,(avg)} = \left(\sum_{j=1}^{N} t_{CLj} \right) / (N \times t_{CK\,(avg)})$$

where $N = 200$

Definition for $t_{JIT(per)}$

$t_{JIT(per)}$ is the single period jitter defined as the largest deviation of any signal t_{CK} from $t_{CK(avg)}$.
$t_{JIT(per)}$ = Min/max of {t_{CKi} - $t_{CK(avg)}$ where i = 1 to 200}.
$t_{JIT(per),act}$ is the actual clock jitter for a given system.
$t_{JIT(per),allowed}$ is the specified allowed clock period jitter.
$t_{JIT(per)}$ is not subject to production test.

Definition for $t_{JIT(cc)}$

$t_{JIT(cc)}$ is defined as the absolute difference in clock period between two consecutive clock cycles.
$t_{JIT(cc)}$ = Max of $|\{t_{CKi+1} - t_{CKi}\}|$.
$t_{JIT(cc)}$ defines the cycle to cycle jitter.
$t_{JIT(cc)}$ is not subject to production test.

Definition for $t_{ERR(nper)}$

$t_{ERR(nper)}$ is defined as the cumulative error across n multiple consecutive cycles from $t_{CK(avg)}$.
$t_{ERR(nper),act}$ is the actual clock jitter over n cycles for a given system.
$t_{ERR(nper),allowed}$ is the specified allowed clock period jitter over n cycles.
$t_{ERR(nper)}$ is not subject to production test.

$$t_{ERR\,(nper)} = \left(\sum_{j=i}^{i+n-1} t_{CKj} \right) - n \times t_{CK\,(avg)}$$

$t_{ERR(nper),min}$ can be calculated by the formula shown below:

$$t_{ERR\,(nper),\,min} = (1 + 0.68\ LN\ (n)) \times t_{JIT(per),\,min}$$

$t_{ERR(nper),max}$ can be calculated by the formula shown below:

$$t_{ERR\,(nper),\,max} = (1 + 0.68\ LN\ (n)) \times t_{JIT(per),\,max}$$

Using these equations, $t_{ERR(nper)}$ tables can be generated for each $t_{JIT(per),act}$ value.

Definition for duty cycle jitter $t_{JIT(duty)}$

$t_{JIT(duty)}$ is defined with absolute and average specification of t_{CH} / t_{CL}.

$$t_{JIT\,(duty),\,min} = MIN\ ((t_{CH(abs),\,min} - t_{CH(avg),\,min}), (t_{CL(abs),\,min} - t_{CL(avg),\,min})) \times t_{CK(avg)}$$

$$t_{JIT\,(duty),\,max} = MAX\ ((t_{CH(abs),\,max} - t_{CH(avg),\,max}), (t_{CL(abs),\,max} - t_{CL(avg),\,max})) \times t_{CK(avg)}$$

Definition for $t_{CK(abs)}$, $t_{CH(abs)}$ and $t_{CL(abs)}$

These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times.

Parameter	Symbol	Min	Unit
Absolute Clock Period	$t_{CK(abs)}$	$t_{CK(avg),min} + t_{JIT(per),min}$	ps
Absolute Clock HIGH Pulse Width	$t_{CH(abs)}$	$t_{CH(avg),min} + t_{JIT(duty),min} / t_{CK(avg),min}$	$t_{CK(avg)}$
Absolute Clock LOW Pulse Width	$t_{CL(abs)}$	$t_{CL(avg),min} + t_{JIT(duty),min} / t_{CK(avg),min}$	$t_{CK(avg)}$

Notes:
1. $t_{CK(avg),min}$ is expressed is ps for this table.
2. $t_{JIT(duty),min}$ is a negative value.

Period Clock Jitter

LPDDR2 devices can tolerate some clock period jitter without core timing parameter derating. This section describes device timing requirements in the presence of clock period jitter ($t_{JIT(per)}$) in excess of the values found in Table of "AC Timing" and how to determine cycle time derating and clock cycle derating.

Clock period jitter effects on core timing parameters (t_{RCD}, t_{RP}, t_{RTP}, t_{WR}, t_{WRA}, t_{WTR}, t_{RC}, t_{RAS}, t_{RRD}, t_{FAW})

Core timing parameters extend across multiple clock cycles. Period clock jitter will impact these parameters when measured in numbers of clock cycles. When the device is operated with clock jitter within the specification limits, the LPDDR2 device is characterized and verified to support $tn_{PARAM} = RU\{ t_{PARAM} / t_{CK(avg)} \}$.

When the device is operated with clock jitter outside specification limits, the number of clocks or $t_{CK(avg)}$ may need to be increased based on the values for each core timing parameter.

Cycle time derating for core timing parameters

For a given number of clocks (tn_{PARAM}), for each core timing parameter, average clock period ($t_{CK(avg)}$) and actual cumulative period error ($t_{ERR}(tn_{PARAM})$,act) in excess of the allowed cumulative period error ($t_{ERR}(tn_{PARAM})$,allowed), the equation below calculates the amount of cycle time derating (in ns) required if the equation results in a positive value for a core timing parameter.

$$\text{CycleTimeDerating} = \text{Max}\left\{\left(\frac{t_{PARAM} + t_{ERR}(tn_{PARAM}),act - t_{ERR}(tn_{PARAM}),allowed}{tn_{PARAM}} - t_{CK(avg)}\right), 0\right\}$$

A cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time deratings determined for each individual core timing parameter.

Clock Cycle derating for core timing parameters

For a given number of clocks (tn_{PARAM}) for each core timing parameter, clock cycle derating should be specified with amount of period jitter ($t_{JIT(per)}$).

For a given number of clocks (tn_{PARAM}), for each core timing parameter, average clock period ($t_{CK(avg)}$) and actual cumulative period error ($t_{ERR}(tn_{PARAM})$,act) in excess of the allowed cumulative period error ($t_{ERR}(tn_{PARAM})$,allowed), the equation below calculates the clock cycle derating (in clocks) required if the equation results in a positive value for a core timing parameter.

$$\text{ClockCycleDerating} = \text{RU}\left\{\frac{t_{PARAM} + t_{ERR}(tn_{PARAM}),act - t_{ERR}(tn_{PARAM}),allowed}{t_{CK(avg)}}\right\} - tn_{PARAM}$$

A clock cycle derating analysis should be conducted for each core timing parameter.

Clock jitter effects on Command/Address timing parameters (t_{IS}, t_{IH}, t_{ISCKE}, t_{IHCKE}, t_{ISb}, t_{IHb}, t_{ISCKEb}, t_{IHCKEb})

These parameters are measured from a command/address signal (CKE, CS_n, CA0 - CA9) transition edge to its respective clock signal (CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT(per)}$, as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

Clock jitter effects on Read timing parameters

t_{RPRE}

When the device is operated with input clock jitter, t_{RPRE} needs to be derated by the actual period jitter ($t_{JIT(per)}$,act,max) of the input clock in excess of the allowed period jitter ($t_{JIT(per)}$,allowed,max). Output deratings are relative to the input clock.

$$t_{RPRE\ (min,\ derated)} = 0.9 - \left(\frac{t_{JIT(per)},act,max - t_{JIT(per)},allowed,max}{t_{CK(avg)}} \right)$$

For example,
if the measured jitter into a LPDDR2-800 device has $t_{CK(avg)}$ = 2500 ps, $t_{JIT(per)}$,act,min = -172 ps and $t_{JIT(per)}$,act,max = + 193 ps, then
$t_{RPRE\ (min,derated)}$ = 0.9 - ($t_{JIT(per)}$,act,max - $t_{JIT(per)}$,allowed,max)/$t_{CK(avg)}$ = 0.9 - (193 - 100)/2500= 0.8628 $t_{CK(avg)}$

$t_{LZ(DQ)}$, $t_{HZ(DQ)}$, t_{DQSCK}, $t_{LZ(DQS)}$, $t_{HZ(DQS)}$

These parameters are measured from a specific clock edge to a data signal (DMn, DQm: n=0, 1, 2, 3. m=0-31) transition and will be met with respect to that clock edge. Therefore, they are not affected by the amount of clock jitter applied (i.e. $t_{JIT(per)}$).

t_{QSH}, t_{QSL}

These parameters are affected by duty cycle jitter which is represented by $t_{CH(abs),\ min}$ and $t_{CL(abs),\ min}$.
$t_{QSH(abs),\ min}$ = $t_{CH(abs),\ min}$ - 0.05
$t_{QSL(abs),\ min}$ = $t_{CL(abs),\ min}$ - 0.05
These parameters determine absolute Data-Valid window at the LPDDR2 device pin.
Absolute min data-valid window @ LPDDR2 device pin =
min { ($t_{QSH(abs),\ min}$ * $t_{CK(avg),\ min}$ - $t_{DQSQ,\ max}$ - $t_{QHS,\ max}$), ($t_{QSL(abs),\ min}$ * $t_{CK(avg),\ min}$ - $t_{DQSQ,\ max}$ - $t_{QHS,\ max}$) }
This minimum data-valid window shall be met at the target frequency regardless of clock jitter.

t_{RPST}

t_{RPST} is affected by duty cycle jitter which is represented by $t_{CL(abs)}$. Therefore $t_{RPST(abs),min}$ can be specified by $t_{CL(abs),\ min}$.
$t_{RPST(abs),\ min}$ = $t_{CL(abs),\ min}$ - 0.05 = $t_{QSL(abs),\ min}$

Clock jitter effects on Write timing parameters

t_{DS}, t_{DH}

These parameters are measured from a data signal (DMn, DQm: n=0, 1, 2, 3. m=0-31) transition edge to its respective data strobe signal (DQSn_t, DQSn_c: n=0, 1, 2, 3) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT(per)}$), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

t_{DSS}, t_{DSH}

These parameters are measured from a data strobe signal (DQSx_t, DQSx_c) crossing to its respective clock signal (CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT(per)}$), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

t_{DQSS}

This parameter is measured from a data strobe signal (DQSx_t, DQSx_c) crossing to the subsequent clock signal (CK_t/CK_c) crossing. When the device is operated with input clock jitter, this parameter needs to be derated by the actual period jitter $t_{JIT(per)}$,act of the input clock in excess of the allowed period jitter $t_{JIT(per)}$,allowed.

$$t_{DQSS\,(min,\,derated)} = 0.75 - \left(\frac{t_{JIT(per)},act,min - t_{JIT(per)},allowed,min}{t_{CK(avg)}} \right)$$

$$t_{DQSS\,(max,\,derated)} = 1.25 - \left(\frac{t_{JIT(per)},act,max - t_{JIT(per)},allowed,max}{t_{CK(avg)}} \right)$$

For example,
if the measured jitter into a LPDDR2-800 device has $t_{CK(avg)}$ = 2500 ps, $t_{JIT(per)}$,act,min = -172 ps and $t_{JIT(per)}$,act,max = + 193 ps, then
$t_{DQSS,(min,derated)}$ = 0.75 - ($t_{JIT(per)}$,act,min - $t_{JIT(per)}$,allowed,min)/$t_{CK(avg)}$ = 0.75 - (-172 + 100)/2500 = 0.7788 $t_{CK(avg)}$
and
$t_{DQSS,(max,derated)}$ = 1.25 - ($t_{JIT(per)}$,act,max - $t_{JIT(per)}$,allowed,max)/$t_{CK(avg)}$ = 1.25 - (193 - 100)/2500 = 1.2128 $t_{CK(avg)}$

Refresh Requirements

Table of Refresh Requirement Parameters

Parameter		Symbol	Value	Unit
Number of Banks			8	
Refresh Window T_{CASE} ≦ 85 ℃		t_{REFW}	32	ms
Required number of REFRESH commands (min)		R	4,096	
Average time between REFRESH commands (for reference only) T_{CASE} ≦ 85 ℃	REFab	t_{REFI}	7.8	us
	REFpb	t_{REFIpb}	0.975	us
Refresh Cycle time		t_{RFCab}	130	ns
Per Bank Refresh Cycle time		t_{RFCpb}	60	ns
Burst Refresh Window = 4 x 8 x t_{RFCab}		t_{REFBW}	4.16	us

AC Timing

Table of AC Timing[*1~2]

AC timing parameters must satisfy the t_{CK} minimum conditions (in multiples of t_{CK}) as well as the timing specifications when values for both are indicated.

Parameter	Symbol	Min / Max	Min t_{CK}	LPDDR2		Unit
				1066	800	
Max. Frequency[*4]		~		533	400	MHz
Clock Timing						
Average Clock Period	$t_{CK(avg)}$	min		1.875	2.5	ns
		max		100		ns
Average HIGH Pulse Width	$t_{CH(avg)}$	min		0.45		$t_{CK(avg)}$
		max		0.55		$t_{CK(avg)}$
Average LOW Pulse Width	$t_{CL(avg)}$	min		0.45		$t_{CK(avg)}$
		max		0.55		$t_{CK(avg)}$
Absolute Clock Period	$t_{CK(abs)}$	min		$t_{CK(avg),\ min} + t_{JIT(per),\ min}$		ps
Absolute Clock HIGH Pulse Width (with allowed jitter)	$t_{CH(abs),\ allowed}$	min		0.43		$t_{CK(avg)}$
		max		0.57		$t_{CK(avg)}$
Absolute Clock LOW Pulse Width (with allowed jitter)	$t_{CL(abs),\ allowed}$	min		0.43		$t_{CK(avg)}$
		max		0.57		$t_{CK(avg)}$
Clock Period Jitter (with allowed jitter)	$t_{JIT(per),\ allowed}$	min		-90	-100	ps
		max		90	100	ps
Maximum Clock Jitter between Two Consecutive Clock Cycles (with allowed jitter)	$t_{JIT(cc),\ allowed}$	max		180	200	ps
Duty Clock Jitter (with allowed jitter)	$t_{JIT(duty),\ allowed}$	min		$\min((t_{CH(abs),min} - t_{CH(avg),min}), (t_{CL(abs),min} - t_{CL(avg),min})) \times t_{CK(avg)}$		ps
		max		$\max((t_{CH(abs),max} - t_{CH(avg),max}), (t_{CL(abs),max} - t_{CL(avg),max})) \times t_{CK(avg)}$		ps
Cumulative Error Across 2 Cycles	$t_{ERR(2per),\ allowed}$	min		-132	-147	ps
		max		132	147	ps
Cumulative Error Across 3 Cycles	$t_{ERR(3per),\ allowed}$	min		-157	-175	ps
		max		157	175	ps
Cumulative Error Across 4 Cycles	$t_{ERR(4per),\ allowed}$	min		-175	-194	ps
		max		175	194	ps
Cumulative Error Across 5 Cycles	$t_{ERR(5per),\ allowed}$	min		-188	-209	ps
		max		188	209	ps

Parameter	Symbol	Min / Max	Min t_{CK}	LPDDR2		Unit
				1066	800	
Cumulative Error Across 6 Cycles	$t_{ERR(6per),allowed}$	min		-200	-222	ps
		max		200	222	ps
Cumulative Error Across 7 Cycles	$t_{ERR(7per),allowed}$	min		-209	-232	ps
		max		209	232	ps
Cumulative Error Across 8 Cycles	$t_{ERR(8per),allowed}$	min		-217	-241	ps
		max		217	241	ps
Cumulative Error Across 9 Cycles	$t_{ERR(9per),allowed}$	min		-224	-249	ps
		max		224	249	ps
Cumulative Error Across 10 Cycles	$t_{ERR(10per),allowed}$	min		-231	-257	ps
		max		231	257	ps
Cumulative Error Across 11 Cycles	$t_{ERR(11per),allowed}$	min		-237	-263	ps
		max		237	263	ps
Cumulative Error Across 12 Cycles	$t_{ERR(12per),allowed}$	min		-242	-269	ps
		max		242	269	ps
Cumulative Error Across *n* = 13, 14,…, 49, 50 Cycles	$t_{ERR(nper),allowed}$	min		$t_{ERR(nper),allowed,\ min} = (1 + 0.68\ln(n)) \times t_{JIT(per),allowed,\ min}$		ps
		max		$t_{ERR(nper),allowed,\ max} = (1 + 0.68\ln(n)) \times t_{JIT(per),allowed\ ,\ max}$		ps
ZQ Calibration Parameters						
Initialization Caibration Time	t_{ZQINIT}	min		1		us
Long Calibration Time	t_{ZQCL}	min	6	360		ns
Short Calibration Time	t_{ZQCS}	min	6	90		ns
Calibration Reset Time	$t_{ZQRESET}$	min	3	50		ns
Read Parameters*14						
DQS Output Access Time from CK_t, CK_c	t_{DQSCK}	min		2500		ps
		max		5500		ps
DQSCK Delta Short*18	$t_{DQSCKDS}$	max		330	450	ps
DQSCK Delta Medium*19	$t_{DQSCKDM}$	max		680	900	ps
DQSCK Delta Long*20	$t_{DQSCKDL}$	max		920	1200	ps
DQS-DQ Skew	t_{DQSQ}	max		200	240	ps
Data Hold Skew Factor	t_{QHS}	max		230	280	ps

Parameter	Symbol	Min / Max	Min t_{CK}	LPDDR2		Unit
				1066	800	
DQS Output HIGH Pulse Width	t_{QSH}	min		$t_{CH(abs)}$ - 0.05		$t_{CK(avg)}$
DQS Output LOW Pulse Width	t_{QSL}	min		$t_{CL(abs)}$ - 0.05		$t_{CK(avg)}$
Data Half Period	t_{QHP}	min		min(t_{QSH}, t_{QSL})		$t_{CK(avg)}$
DQ / DQS Output Hold Time from DQS	t_{QH}	min		t_{QHP} - t_{QHS}		ps
READ Preamble*15~16	t_{RPRE}	min		0.9		$t_{CK(avg)}$
READ Postamble*15,17	t_{RPST}	min		$t_{CL(abs)}$ - 0.05		$t_{CK(avg)}$
DQS Low-Z from Clock*15	$t_{LZ(DQS)}$	min		$t_{DQSCK, min}$ - 300		ps
DQ Low-Z from Clock*15	$t_{LZ(DQ)}$	min		$t_{DQSCK, min}$ - (1.4 x $t_{QHS, max}$)		ps
DQS High-Z from Clock*15	$t_{HZ(DQS)}$	max		$t_{DQSCK, max}$ - 100		ps
DQ High-Z from Clock*15	$t_{HZ(DQ)}$	max		$t_{DQSCK, max}$ + (1.4 x $t_{DQSQ, max}$)		ps
Write Parameters*14						
DQ and DM Input Hold Time (V_{REF} based)	t_{DH}	min		210	270	ps
DQ and DM Input Setup Time (V_{REF} based)	t_{DS}	min		210	270	ps
DQ and DM Input Pulse Width	t_{DIPW}	min		0.35		$t_{CK(avg)}$
Write Command to 1st DQS Latching Transition	t_{DQSS}	min		0.75		$t_{CK(avg)}$
		max		1.25		$t_{CK(avg)}$
DQS Input High-Level Width	t_{DQSH}	min		0.4		$t_{CK(avg)}$
DQS Input Low-Level Width	t_{DQSL}	min		0.4		$t_{CK(avg)}$
DQS Falling Edge to CK Setup Time	t_{DSS}	min		0.2		$t_{CK(avg)}$
DQS Falling Edge Hold Time from CK	t_{DSH}	min		0.2		$t_{CK(avg)}$
Write Postamble	t_{WPST}	min		0.4		$t_{CK(avg)}$
Write Preamble	t_{WPRE}	min		0.35		$t_{CK(avg)}$
CKE Input Parameters						
CKE Min. Pulse Width (high and low pulse width)	t_{CKE}	min	3	3		$t_{CK(avg)}$
CKE Input Setup Time	t_{ISCKE}*2	min		0.25		$t_{CK(avg)}$
CKE Input Hold Time	t_{IHCKE}*3	min		0.25		$t_{CK(avg)}$
Command / Address Input Parameters*14						
Address and Control Input Hold Time (V_{REF} based)	t_{IH}*1	min		220	290	ps
Address and Control Input Setup Time (V_{REF} based)	t_{IS}*1	min		220	290	ps
Address and Control Input Pulse Width	t_{IPW}	min		0.4		$t_{CK(avg)}$

Parameter	Symbol	Min / Max	Min t_{CK}	LPDDR2		Unit
				1066	800	
Boot Parameters (10 MHz - 55 MHz) *8,10,11						
Clock Cycle Time	t_{CKb}	max		100		ns
		min		18		ns
CKE Input Setup Time	t_{ISCKEb}	min		2.5		ns
CKE Input Hold Time	t_{IHCKEb}	min		2.5		ns
Address & Control Input Setup Time	t_{ISb}	min		1150		ps
Address & Control Input Hold Time	t_{IHb}	min		1150		ps
DQS Output Data Access Time from CK_t/ CK_c	t_{DQSCKb}	min		2.0		ns
		max		10.0		ns
Data Strobe Edge to Output Data Edge t_{DQSQb}-1.2	t_{DQSQb}	max		1.2		ns
Data Hold Skew Factor	t_{QHSb}	max		1.2		ns
Mode Register Parameters						
Mode Register Read Command Period	t_{MRR}	min	2	2		$t_{CK(avg)}$
Mode Register Write Command Period	t_{MRW}	min	5	5		$t_{CK(avg)}$
SDRAM Core Parameters[*12]						
Read Latency	RL	min		8	6	$t_{CK(avg)}$
Write Latency	WL	min		4	3	$t_{CK(avg)}$
Active to Active Command Period	t_{RC}	min		t_{RAS} + t_{RPab} (with all-bank Precharge) t_{RAS} + t_{RPpb} (with per-bank Precharge)		ns
CKE Minimum Pulse Width during Self Refresh (Low Pulse Width during Self Refresh)	t_{CKESR}	min	3	15		ns
Self Refresh Exit to Next Valid Command Delay	t_{XSR}	min	2	t_{RFCab} +10		ns
Exit Power Down to Next Valid Command Delay	t_{XP}	min	2	7.5		ns
CAS to CAS Delay	t_{CCD}	min	2	2		$t_{CK(avg)}$
Internal Read to Precharge Command Delay	t_{RTP}	min	2	7.5		ns
RAS to CAS Delay	t_{RCD}	Fast	3	15		ns
		Typ	3	18		ns
		Slow	3	24		ns

Parameter	Symbol	Min / Max	Min t_{CK}	LPDDR2		Unit
				1066	800	
Row Precharge Time (single bank)	t_{RPpb}	Fast	3	15		ns
		Typ	3	18		ns
		Slow	3	24		ns
Row Precharge Time (all bank)	t_{RPab}	Fast	3	18		ns
		Typ	3	21		ns
		Slow	3	27		ns
Row Active Time	t_{RAS}	min	3	42		ns
		max		70		us
Write Recovery Time	t_{WR}	min	3	15		ns
Internal Write to Read Command Delay	t_{WTR}	min	2	7.5		ns
Active *Bank A* to Active *Bank B C*ommand	t_{RRD}	min	2	10		ns
Four Bank Activate Window	t_{FAW}	min	8	50		ns
Minimum Deep Power Down Time	t_{DPD}	min		500		us
Temperature Derating						
t_{DQSCK} Derating	t_{DQSCK} (Derated)	max		5620	6000	ps
Core Timings Temperature Derating	t_{RCD} (Derated)	min		t_{RCD} + 1.875		ns
	t_{RC} (Derated)	min		t_{RC} + 1.875		ns
	t_{RAS} (Derated)	min		t_{RAS} + 1.875		ns
	t_{RP} (Derated)	min		t_{RP} + 1.875		ns
	t_{RRD} (Derated)	min		t_{RRD} + 1.875		ns

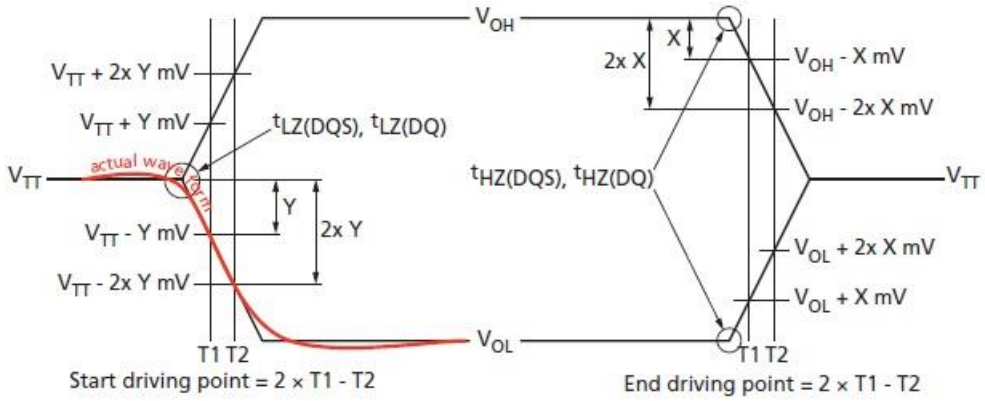
Notes:

1. Frequency values are for reference only. Clock cycle time (t_{CK}) shall be used to determine device capabilities.
2. All AC timings assume an input slew rate of 1V/ns.
3. Read, Write, and input setup and hold values are referenced to V_{REF}.
4. $t_{DQSCKDS}$ is the absolute value of the difference between any two t_{DQSCK} measurements (in a byte lane) within a contiguous sequence of bursts in a 160ns rolling window. $t_{DQSCKDS}$ is not tested and is guaranteed by design. Temperature drift in the system is < 10℃/s. Values do not include clock jitter.
5. $t_{DQSCKDM}$ is the absolute value of the difference between any two t_{DQSCK} measurements (in a byte lane) within a 1.6us rolling window. $t_{DQSCKDM}$ is not tested and is guaranteed by design. Temperature drift in the system is < 10℃/s. Values do not include clock jitter.
6. $t_{DQSCKDL}$ is the absolute value of the difference between any two t_{DQSCK} measurements (in a byte lane) within a 32ms rolling window. $t_{DQSCKDL}$ is not tested and is guaranteed by design. Temperature drift in the system is < 10℃/s. Values do not include clock jitter.

   For Low-to-High and High-to-Low transitions, the timing reference is at the point when the signal crosses V_{TT}. t_{HZ} and t_{LZ} transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for t_{RPST}, $t_{HZ(DQS)}$ and $t_{HZ(DQ)}$),

or begins driving (for t_{RPRE}, $t_{LZ(DQS)}$, $t_{LZ(DQ)}$). The figure below shows a method to calculate the point when device is no longer driving $t_{HZ(DQS)}$ and $t_{HZ(DQ)}$, or begins driving $t_{LZ(DQS)}$ and $t_{LZ(DQ)}$ by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters $t_{LZ(DQS)}$, $t_{LZ(DQ)}$, $t_{HZ(DQS)}$, and $t_{HZ(DQ)}$ are defined as single-ended. The timing parameters t_{RPRE} and t_{RPST} are determined from the differential signal DQS_t / DQS_c.

Output Transition Timing



7. Measured from the start driving of DQS_t / DQS_c to the start driving the first rising strobe edge.
8. Measured from the start driving the last falling strobe edge to the stop driving DQS_t / DQS_c.
9. CKE input setup time is measured from CKE reaching High/Low voltage level to CK_t / CK_c crossing.
10. CKE input hold time is measured from CK_t/CK_c crossing to CKE reaching High/Low voltage level.
11. Input setup/hold time for signal (CA0 ~ 9, CS_n).
12. To ensure device operation before the device is configured a number of AC boot timing parameters are defined in this table. Boot parameter symbols have the letter **b** appended, e.g., t_{CK} during boot is t_{CKb}.
13. The LPDDR2 devices set some mode register default values upon receiving a RESET (MRW) command as specified in "Mode Register Definition" section.
14. The output skew parameters are measured with R_{ON} default settings into the reference load.
15. The min t_{CK} column applies only when t_{CK} is greater than 6ns.
16. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime.

CA and CS_n Setup, Hold and Derating

For all input signals (CA and CS_n) the total t_{IS} (setup time) and t_{IH} (hold time) is calculated by adding the data sheet $t_{IS(base)}$ and $t_{IH(base)}$ value to the $\triangle t_{IS}$ and $\triangle t_{IH}$ derating value respectively (see the series of tables following this section). Example: t_{IS} (total setup time) = $t_{IS(base)}$ + $\triangle t_{IS}$.

Setup (t_{IS}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC),\,min}$. Setup (t_{IS}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC),\,max}$. If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(DC)}$ to AC region', use nominal slew rate for derating value (see the Figure of "Illustration of nominal slew rate and t_{VAC} for setup time t_{IS} for CA and CS_n with respect to clock"). If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(DC)}$ to AC region', the slew rate of a tangent line to the actual signal from the AC level to DC level is used for derating value (see the Figure of "Illustration of tangent line for setup time t_{IS} for CA and CS_n with respect to clock").

Hold (t_{IH}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC),\,max}$ and the first crossing of $V_{REF(DC)}$. Hold (t_{IH}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC),min}$ and the first crossing of $V_{REF(DC)}$. If the actual signal is always later than the nominal slew rate line between shaded 'DC to $V_{REF(DC)}$ region', use nominal slew rate for derating value (see the Figure of "Illustration of nominal slew rate for hold time t_{IH} for CA and CS_n with respect to clock"). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'DC to $V_{REF(DC)}$ region', the slew rate of a tangent line to the actual signal from the DC level to $V_{REF(DC)}$ level is used for derating value (see the Figure of "Illustration of tangent line for hold time t_{IH} for CA and CS_n with respect to clock").

For a valid transition, the input signal has to remain above/below $V_{IH}/V_{IL(AC)}$ for some time t_{VAC} (see the Table of "Required time t_{VAC} above $V_{IH(AC)}$ {below $V_{IL(AC)}$} for valid transition"). Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH}/V_{IL(AC)}$ at the time of the rising clock transition). A valid input signal is still required to complete the transition and reach $V_{IH}/V_{IL(AC)}$.

For slew rates between the values listed in the tables, the derating values are obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization.

Table of CA and CS_n Setup and Hold Base-Values for 1V/ns

Unit [ps]	LPDDR2		Reference
	1066	800	
$t_{IS(base)}$	0	70	$V_{IH}/V_{IL(AC)} = V_{REF(DC)} \pm 220mV$
$t_{IH(base)}$	90	160	$V_{IH}/V_{IL(DC)} = V_{REF(DC)} \pm 130mV$

Note: AC/DC referenced for 1V/ns CA and CS_n slew rate and 2V/ns differential CK_t / CK_c slew rate.

Table of Derating values LPDDR2 t_{IS}/t_{IH} - AC/DC based AC220

$\triangle t_{IS}$, $\triangle t_{IH}$ derating in [ps] AC/DC based AC220 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 220mV$, $V_{IL(AC)} = V_{REF(DC)} - 220mV$ DC130 Threshold -> $V_{IH(DC)} = V_{REF(DC)} + 130mV$, $V_{IL(DC)} = V_{REF(DC)} - 130mV$																	
		CK_t, CK_c Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		$\triangle t_{IS}$	$\triangle t_{IH}$	$\triangle t_{IS}$	$\triangle t_{IH}$	$\triangle t_{IS}$	$\triangle t_{IH}$	$\triangle t_{IS}$	$\triangle t_{IH}$	$\triangle t_{IS}$	$\triangle t_{IH}$	$\triangle t_{IS}$	$\triangle t_{IH}$	$\triangle t_{IS}$	$\triangle t_{IH}$	$\triangle t_{IS}$	$\triangle t_{IH}$
CA, CS_n Slew rate V/ns	2.0	110	65	110	65	110	65										
	1.5	74	43	73	43	73	43	89	59								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-3	-5	-3	-5	13	11	29	27	45	43				
	0.8					-8	-13	8	3	24	19	40	35	56	55		
	0.7							2	-6	18	10	34	26	50	46	66	78
	0.6									10	-3	26	13	42	33	58	65
	0.5											4	-4	20	16	36	48
	0.4													-7	2	17	34

Note: Cell contents shaded in blue are defined as ‘not supported’.

Table of Derating values LPDDR2 t_{IS}/t_{IH} - AC/DC based - AC300

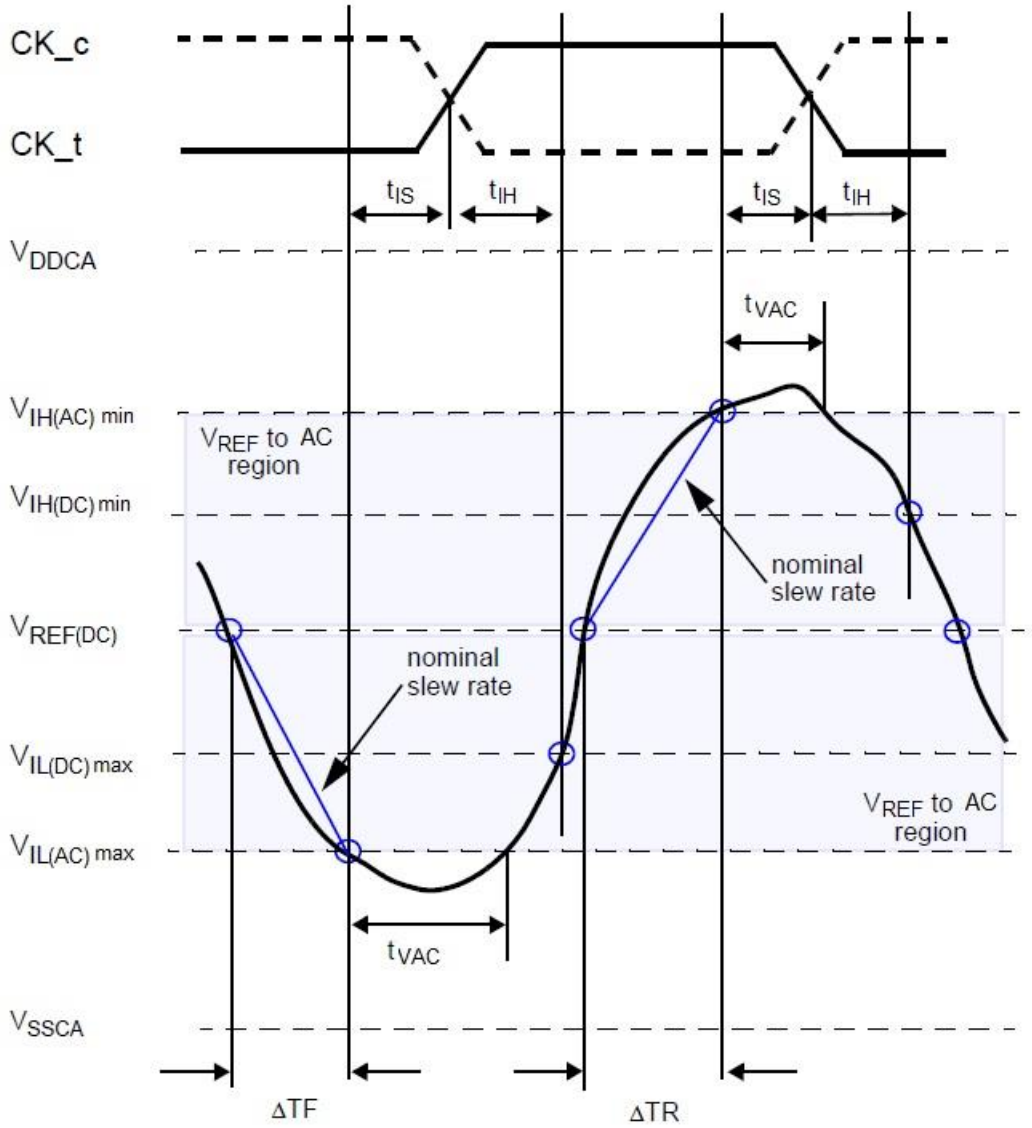
$\triangle t_{IS}$, $\triangle t_{IH}$ derating in [ps] AC/DC based AC300 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 300mV$, $V_{IL(AC)} = V_{REF(DC)} - 300mV$ DC200 Threshold -> $V_{IH(DC)} = V_{REF(DC)} + 200mV$, $V_{IL(DC)} = V_{REF(DC)} - 200mV$																	
		CK_t, CK_c Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		$\triangle t_{IS}$	$\triangle t_{IH}$	$\triangle t_{IS}$	$\triangle t_{IH}$	$\triangle t_{IS}$	$\triangle t_{IH}$	$\triangle t_{IS}$	$\triangle t_{IH}$	$\triangle t_{IS}$	$\triangle t_{IH}$	$\triangle t_{IS}$	$\triangle t_{IH}$	$\triangle t_{IS}$	$\triangle t_{IH}$	$\triangle t_{IS}$	$\triangle t_{IH}$
CA, CS_n Slew rate V/ns	2.0	150	100	150	100	150	100										
	1.5	100	67	100	67	100	67	116	83								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-4	-8	-4	-8	12	8	28	24	44	40				
	0.8					-12	-20	4	-4	20	12	36	28	52	48		
	0.7							-3	-18	13	-2	29	14	45	34	61	66
	0.6									2	-21	18	-5	34	15	50	47
	0.5											-12	-32	4	-12	20	20
	0.4													-35	-40	-11	-8

Note: Cell contents shaded in blue are defined as ‘not supported’.

Table of Required time t_{VAC} above $V_{IH(AC)}$ {below $V_{IL(AC)}$} for valid transition

Slew Rate [V/ns]	t_{VAC} @ 300mV [ps]		t_{VAC} @ 220mV [ps]	
	min	max	min	max
> 2.0	75	-	175	-
2.0	57	-	170	-
1.5	50	-	167	-
1.0	38	-	163	-
0.9	34	-	162	-
0.8	29	-	161	-
0.7	22	-	159	-
0.6	13	-	155	-
0.5	0	-	150	-
< 0.5	0	-	150	-

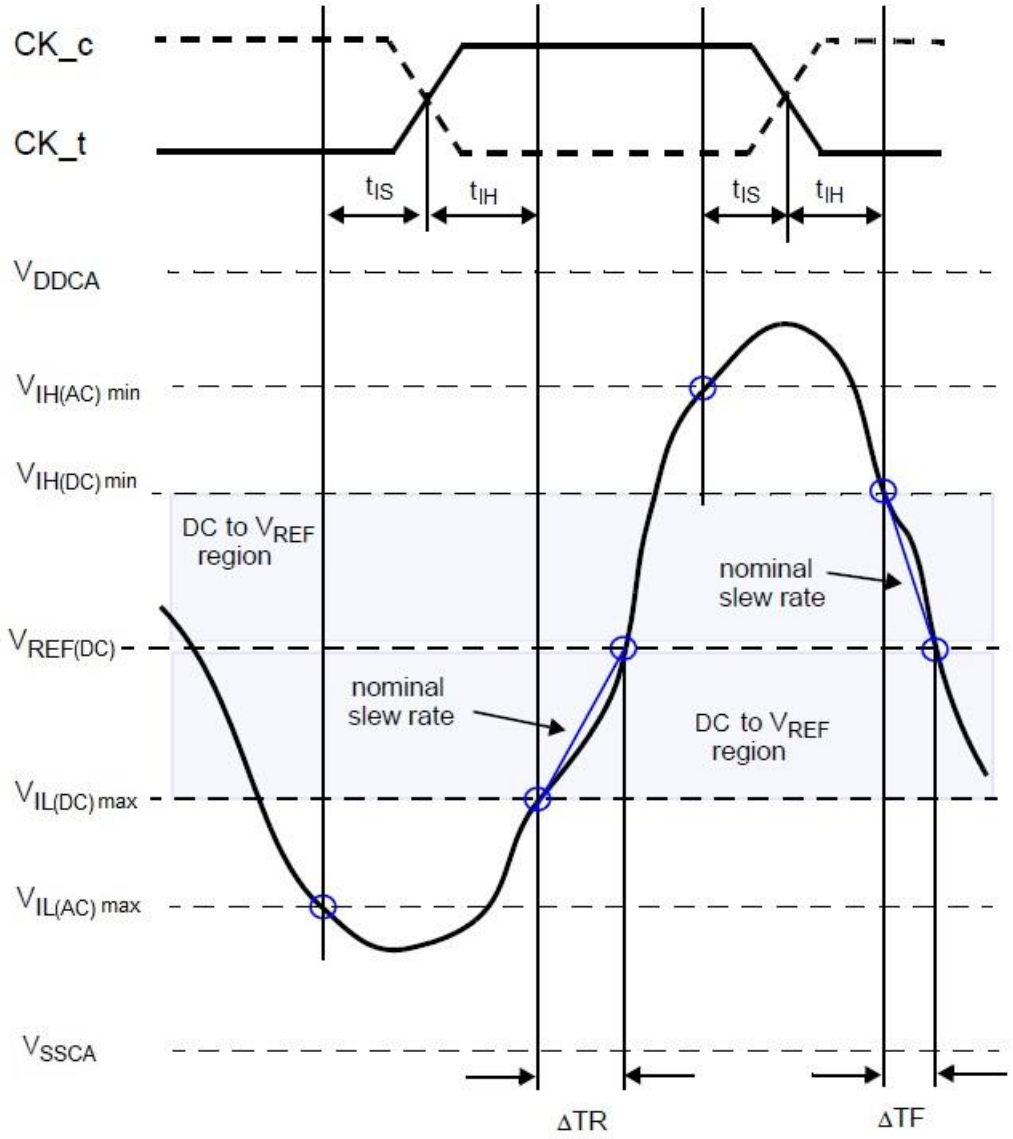
Figure of Illustration of nominal slew rate and t_{VAC} for setup time t_{IS} for CA and CS_n with respect to clock



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(DC)} - V_{IL(AC)\ max}}{\triangle TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH(AC)\ min} - V_{REF(DC)}}{\triangle TR}$$

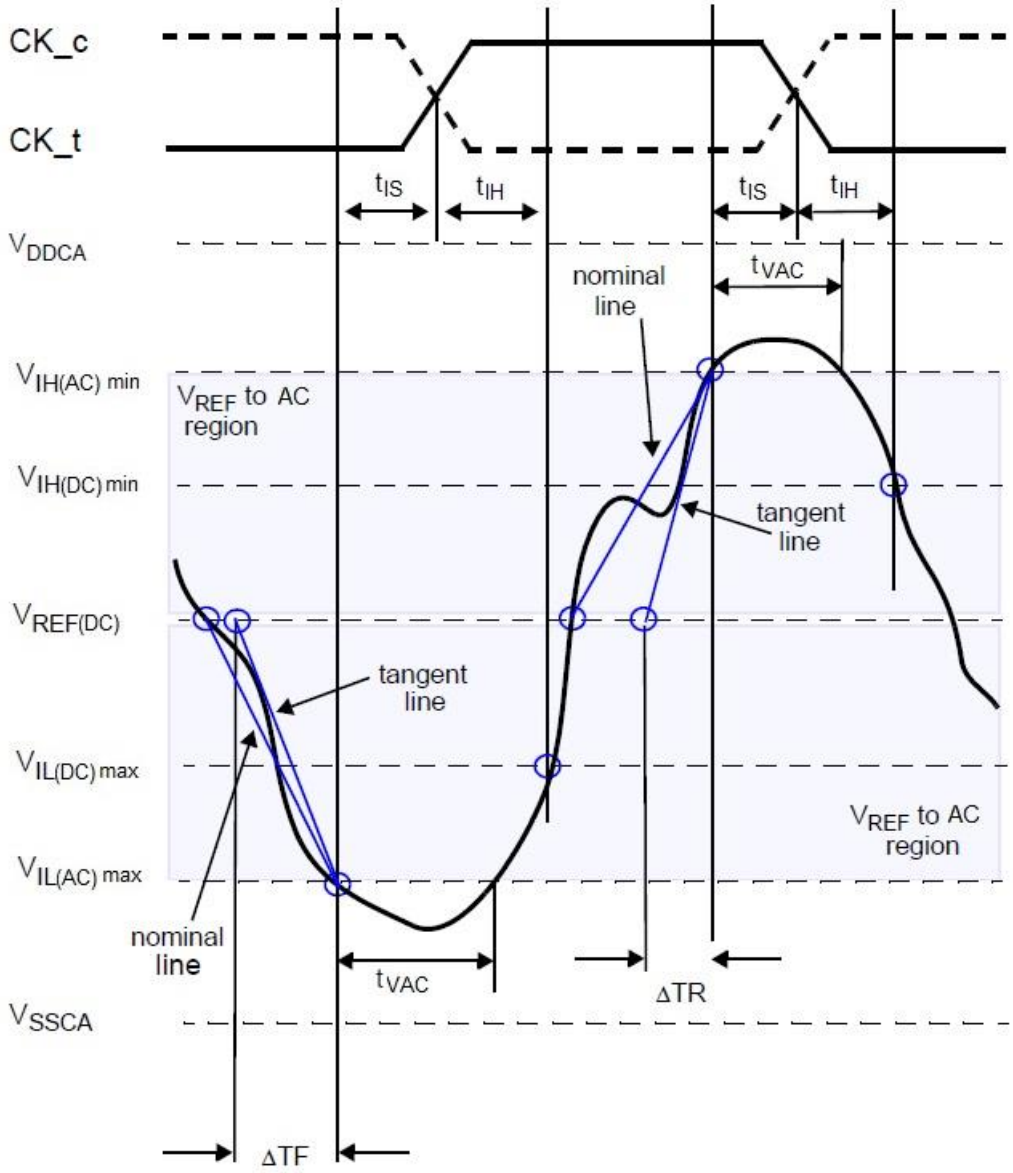
Figure of Illustration of nominal slew rate for hold time t_{IH} for CA and CS_n with respect to clock



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(DC)} - V_{IL(DC)\ max}}{\triangle TR}$$

$$\text{Hold Slew Rate Fallng Signal} = \frac{V_{IH(DC)\ min} - V_{REF(DC)}}{\triangle TF}$$

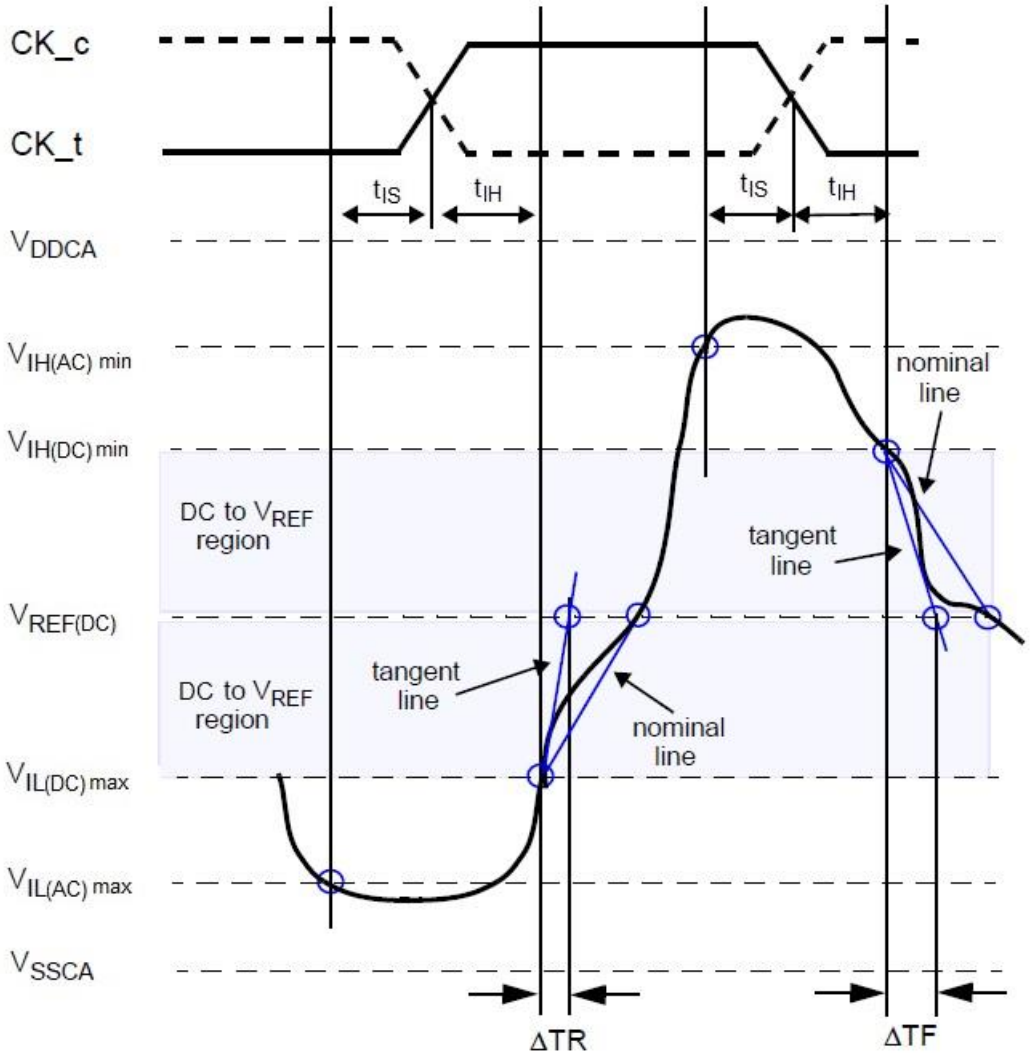
Figure of Illustration of tangent line for setup time t_{IS} for CA and CS_n with respect to clock



$$\text{Setup Slew Rate Rising Signal} = \frac{\text{tangent line } [\, V_{IH(AC)\ min} - V_{REF(DC)} \,]}{\triangle TR}$$

$$\text{Setup Slew Rate Fallng Signal} = \frac{\text{tangent line } [\, V_{REF(DC)} - V_{IL(AC)\ max} \,]}{\triangle TF}$$

Figure of Illustration of tangent line for for hold time t_{IH} for CA and CS_n with respect to clock



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line } [\, V_{REF(DC)} - V_{IL(DC)\ max} \,]}{\triangle TR}$$

$$\text{Hold Slew Rate Fallng Signal} = \frac{\text{tangent line } [\, V_{IH(DC)\ min} - V_{REF(DC)} \,]}{\triangle TF}$$

Data Setup, Hold and Slew Rate Derating

For all input signals (DQ, DM), the total t_{DS} (setup time) and t_{DH} (hold time) required is calculated by adding the data sheet $t_{DS(base)}$ and $t_{DH(base)}$ value to the $\triangle t_{DS}$ and $\triangle t_{DH}$ derating value respectively(see the series of tables following this section). Example: t_{DS} (total setup time) = $t_{DS(base)}$ + $\triangle t_{DS}$.

Setup (t_{DS}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC),\,min}$. Setup (t_{DS}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC),\,max}$ (see the Figure of "Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} for DQ with respect to strobe").

If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(DC)}$ to AC region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(DC)}$ to AC region', the slew rate of a tangent line to the actual signal from the AC level to DC level is used for derating value (see the Figure of "Illustration of tangent line for setup time t_{DS} for DQ with respect to strobe").

Hold (t_{DH}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC),\,max}$ and the first crossing of $V_{REF(DC)}$. Hold (t_{DH}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC),min}$ and the first crossing of $V_{REF(DC)}$ (see the Figure of "Illustration of nominal slew rate for hold time t_{DH} for DQ with respect to strobe").

If the actual signal is always later than the nominal slew rate line between shaded 'DC level to $V_{REF(DC)}$ region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'DC to $V_{REF(DC)}$ region', the slew rate of a tangent line to the actual signal from the DC level to $V_{REF(DC)}$ level is used for derating value (see the Figure of "Illustration of tangent line for hold time t_{DH} for DQ with respect to strobe").

For a valid transition the input signal has to remain above/below $V_{IH}/V_{IL(AC)}$ for some time t_{VAC} (see the Table of "Required time t_{VAC} above $V_{IH(AC)}$ {below $V_{IL(AC)}$} for valid transition").

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH}/V_{IL(AC)}$ at the time of the rising clock transition), a valid input signal is still required to complete the transition and reach $V_{IH}/V_{IL(AC)}$.

For slew rates between the values listed in the tables, the derating values can be obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization.

Table of Data Setup and Hold Base-Values for 1V/ns

Unit [ps]	LPDDR2		Reference
	1066	800	
$t_{DS(base)}$	-10	50	$V_{IH}/V_{IL(AC)} = V_{REF(DC)} \pm 220mV$
$t_{DH(base)}$	80	140	$V_{IH}/V_{IL(DC)} = V_{REF(DC)} \pm 130mV$

Note: AC/DC referenced for 1V/ns DQ, DM slew rate and 2V/ns differential DQS_t / DQS_c slew rate.

Table of Derating values LPDDR2 t_{DS}/t_{DH} - AC/DC based AC220

$\triangle t_{DS}$, $\triangle t_{DH}$ derating in [ps] AC/DC based AC220 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 220mV$, $V_{IL(AC)} = V_{REF(DC)} - 220mV$ DC130 Threshold -> $V_{IH(DC)} = V_{REF(DC)} + 130mV$, $V_{IL(DC)} = V_{REF(DC)} - 130mV$																	
		DQS_t, DQS_c Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		$\triangle t_{DS}$	$\triangle t_{DH}$	$\triangle t_{DS}$	$\triangle t_{DH}$	$\triangle t_{DS}$	$\triangle t_{DH}$	$\triangle t_{DS}$	$\triangle t_{DH}$	$\triangle t_{DS}$	$\triangle t_{DH}$	$\triangle t_{DS}$	$\triangle t_{DH}$	$\triangle t_{DS}$	$\triangle t_{DH}$	$\triangle t_{DS}$	$\triangle t_{DH}$
DQ, DM Slew rate V/ns	2.0	110	65	110	65	110	65										
	1.5	74	43	73	43	73	43	89	59								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-3	-5	-3	-5	13	11	29	27	45	43				
	0.8					-8	-13	8	3	24	19	40	35	56	55		
	0.7							2	-6	18	10	34	26	50	46	66	78
	0.6									10	-3	26	13	42	33	58	65
	0.5											4	-4	20	16	36	48
	0.4													-7	2	17	34

Note: Cell contents shaded in blue are defined as 'not supported'.

Table of Derating values LPDDR2 t_{DS}/t_{DH} - AC/DC based - AC300

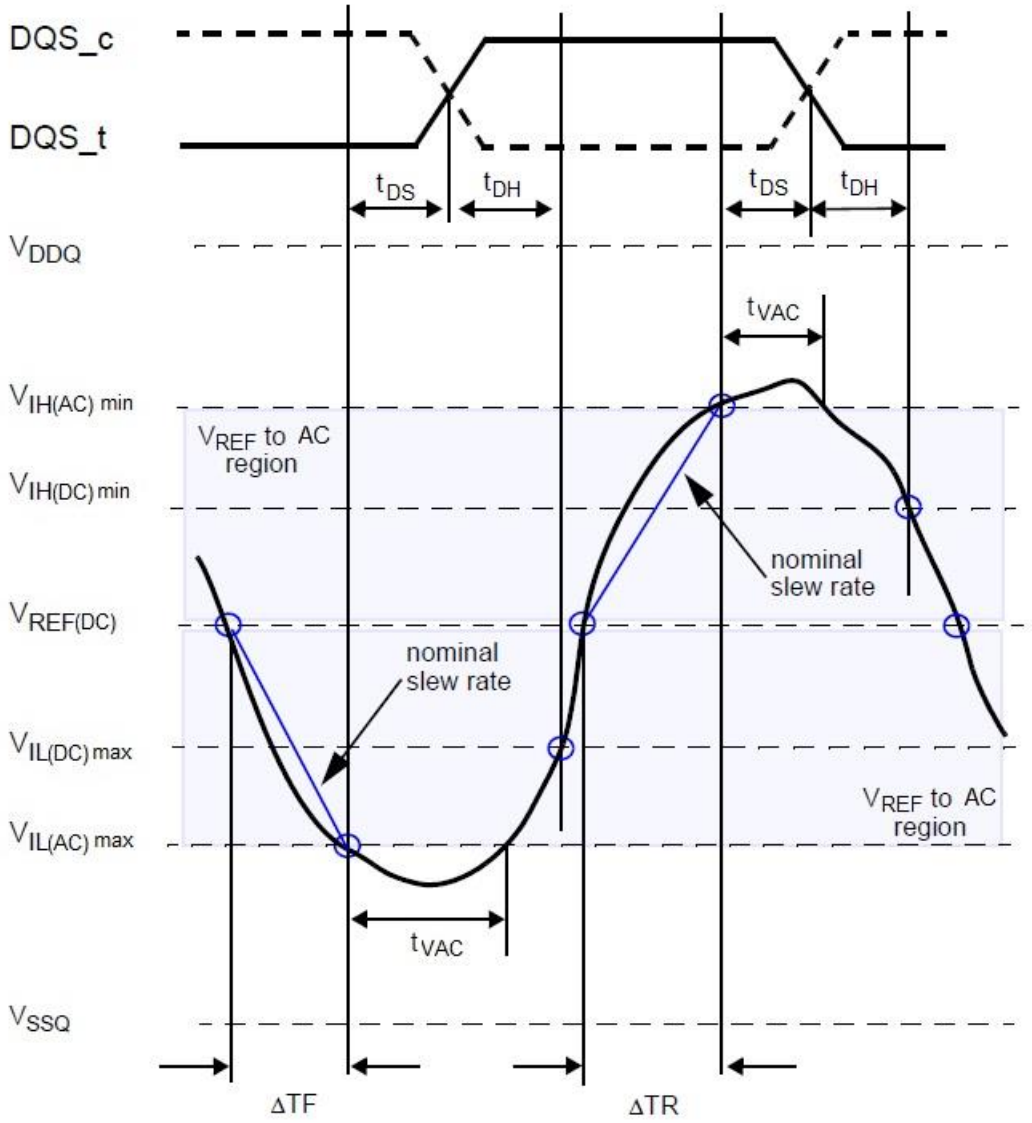
$\triangle t_{DS}$, $\triangle t_{DH}$ derating in [ps] AC/DC based AC300 Threshold -> $V_{IH(AC)} = V_{REF(DC)} + 300mV$, $V_{IL(AC)} = V_{REF(DC)} - 300mV$ DC200 Threshold -> $V_{IH(DC)} = V_{REF(DC)} + 200mV$, $V_{IL(DC)} = V_{REF(DC)} - 200mV$																	
		DQS_t, DQS_c Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		$\triangle t_{IS}$	$\triangle t_{IH}$	$\triangle t_{IS}$	$\triangle t_{IH}$	$\triangle t_{IS}$	$\triangle t_{IH}$	$\triangle t_{IS}$	$\triangle t_{IH}$	$\triangle t_{IS}$	$\triangle t_{IH}$	$\triangle t_{IS}$	$\triangle t_{IH}$	$\triangle t_{IS}$	$\triangle t_{IH}$	$\triangle t_{IS}$	$\triangle t_{IH}$
DQ, DM Slew rate V/ns	2.0	150	100	150	100	150	100										
	1.5	100	67	100	67	100	67	116	83								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-4	-8	-4	-8	12	8	28	24	44	40				
	0.8					-12	-20	4	-4	20	12	36	28	52	48		
	0.7							-3	-18	13	-2	29	14	45	34	61	66
	0.6									2	-21	18	-5	34	15	50	47
	0.5											-12	-32	4	-12	20	20
	0.4													-35	-40	-11	-8

Note: Cell contents shaded in blue are defined as 'not supported'.

Table of Required time t_{VAC} above $V_{IH(AC)}$ {below $V_{IL(AC)}$} for valid transition

Slew Rate [V/ns]	t_{VAC} @ 300mV [ps]		t_{VAC} @ 220mV [ps]	
	min	max	min	max
> 2.0	75	-	175	-
2.0	57	-	170	-
1.5	50	-	167	-
1.0	38	-	163	-
0.9	34	-	162	-
0.8	29	-	161	-
0.7	22	-	159	-
0.6	13	-	155	-
0.5	0	-	150	-
< 0.5	0	-	150	-

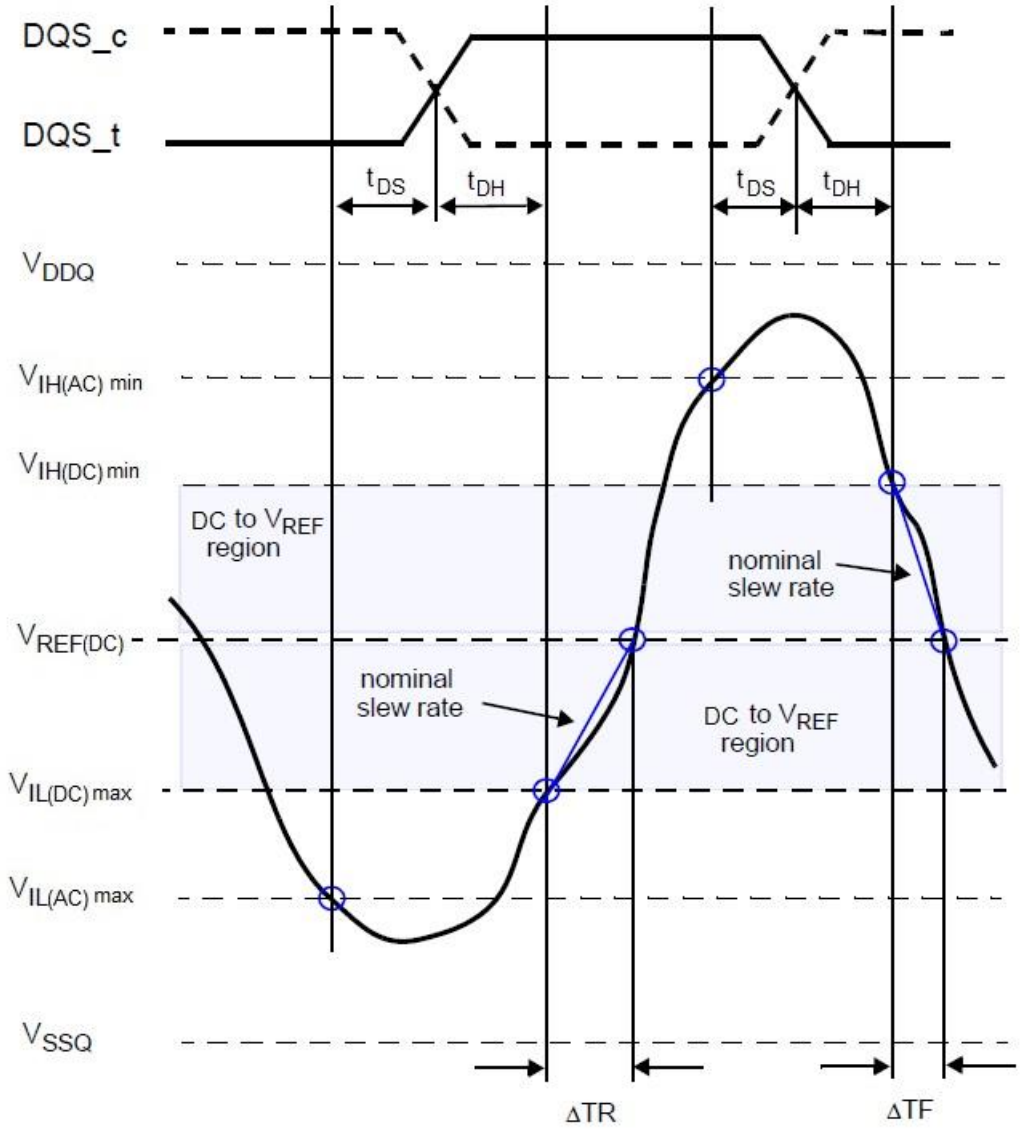
Figure of Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} for DQ with respect to strobe



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(DC)} - V_{IL(AC)\ max}}{\triangle TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH(AC)\ min} - V_{REF(DC)}}{\triangle TR}$$

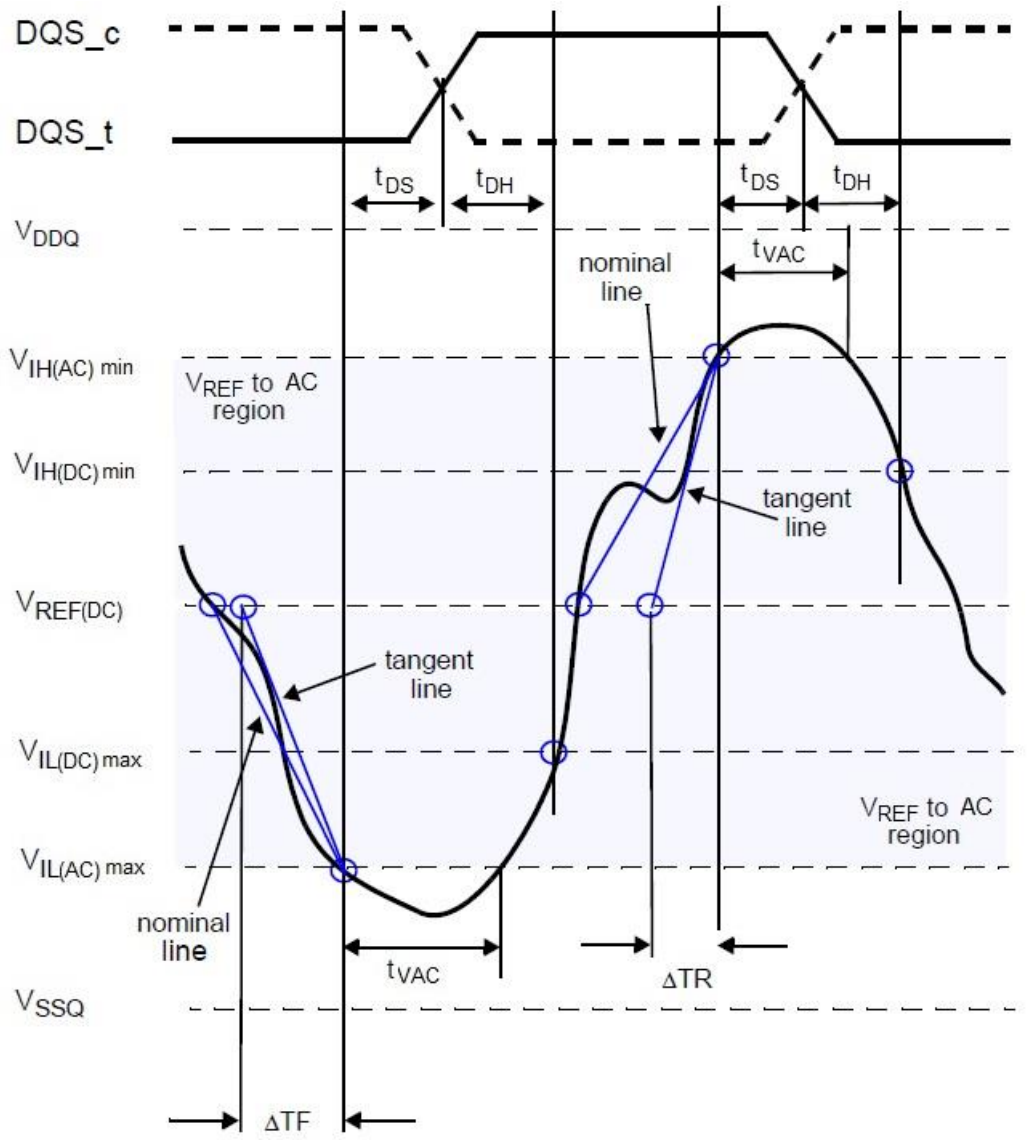
Figure of Illustration of nominal slew rate for hold time t_{DH} for DQ with respect to strobe



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(DC)} - V_{IL(DC)\ max}}{\triangle TR}$$

$$\text{Hold Slew Rate Fallng Signal} = \frac{V_{IH(DC)\ min} - V_{REF(DC)}}{\triangle TF}$$

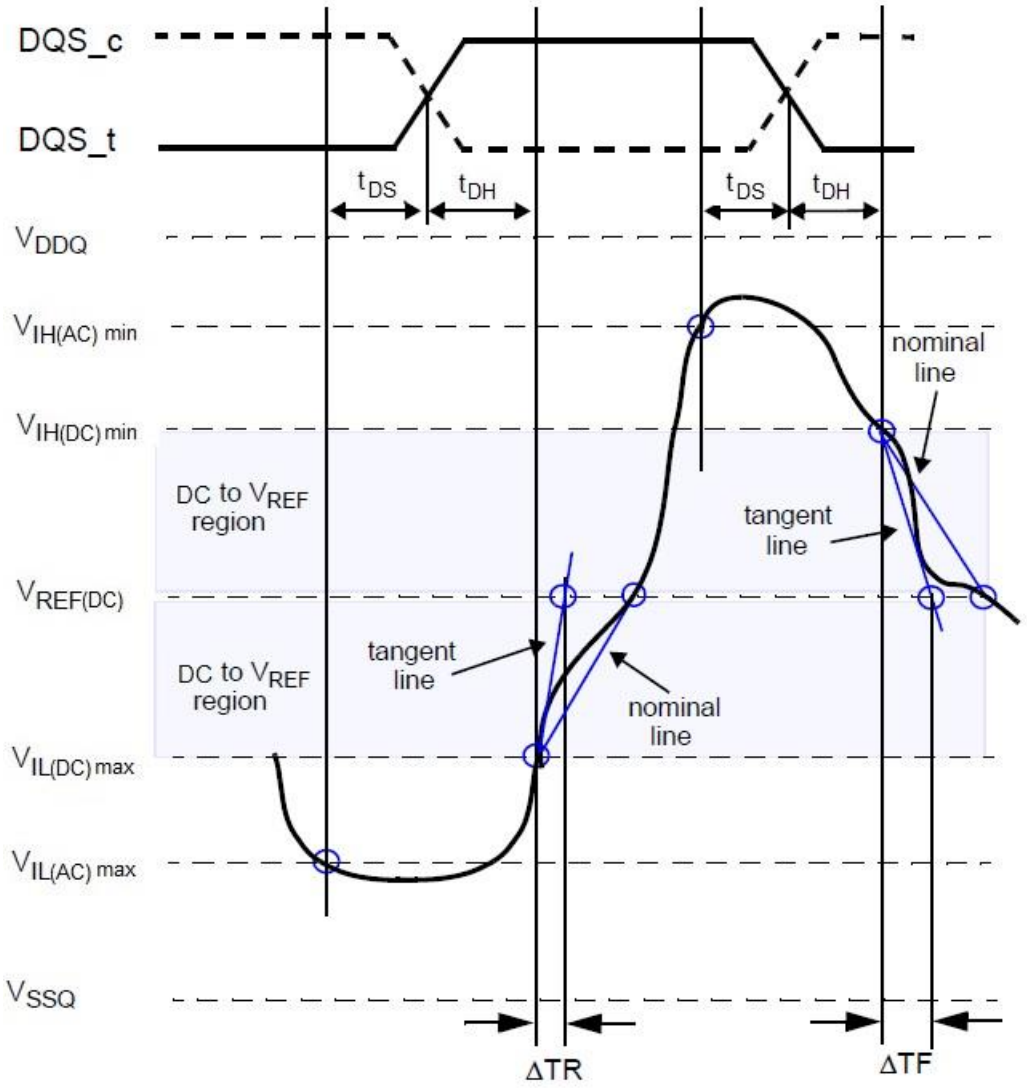
Figure of Illustration of tangent line for setup time t_{DS} for DQ with respect to strobe



$$\text{Setup Slew Rate Rising Signal} = \frac{\text{tangent line } [\ V_{IH(AC)\ min} - V_{REF(DC)}\ ]}{\triangle TR}$$

$$\text{Setup Slew Rate Fallng Signal} = \frac{\text{tangent line } [\ V_{REF(DC)} - V_{IL(AC)\ max}\ ]}{\triangle TF}$$

Figure of Illustration of tangent line for for hold time t_{DH} for DQ with respect to strobe



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line } [\, V_{REF(DC)} - V_{IL(DC)\ max} \,]}{\triangle TR}$$

$$\text{Hold Slew Rate Fallng Signal} = \frac{\text{tangent line } [\, V_{IH(DC)\ min} - V_{REF(DC)} \,]}{\triangle TF}$$

Functional Description

LPDDR2 devices use double data rate archiecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and bank information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.

LPDDR2-S4 devices use double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially a 4n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2-S4 effectively consists of a single 4n-bit-wide, one-clock-cycle data transfer at the internal SDRAM core and four corresponding n-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

For LPDDR2-S4 devices, accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.

Prior to normal operation, the LPDDR2 device must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

Power Up, Initialization, and Power Off

The LPDDR2 Devices must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

Power Ramp and Device Initialization

The following sequence shall be used to power up an LPDDR2 device. Unless specified otherwise, these steps are mandatory.

1. Power Ramp

While applying power (after Ta), CKE shall be held at a logic low level (=<0.2 x V_{DDCA}), all other inputs shall be between $V_{IL\ min}$ and V_{IHmax}. The device will only guarantee that outputs are in a high impedance state while CKE is held low.

On or before the completion of the power ramp (Tb), CKE must be held low. DQ, DM, DQS_t and DQS_c voltage levels must be between V_{SSQ} and V_{DDQ} during voltage ramp to avoid latchup. CK_t, CK_c, CS_n, and CA input levels must be between V_{SSCA} and V_{DDCA} during voltage ramp to avoid latchup.

The following conditions apply:

- Ta is the point when any power supply first reaches 300mV.
- Noted conditions apply between Ta and power down (controlled or uncontrolled).
- Tb is the point at which all supply and reference voltages are within their defined operating ranges.
- Power ramp duration t_{INIT0} (Tb - Ta) must not exceed 20ms.
- For supply and reference voltage operating conditions, see the Table of “Recommended DC Operating Conditions”.
- The voltage difference between any of V_{SS}, V_{SSQ}, and V_{SSCA} pins must not exceed 100mV.

Power Ramp Completion

After Ta is reached:

- V_{DD1} must be greater than V_{DD2} - 200mV.
- V_{DD1} and V_{DD2} must be greater than V_{DDCA} - 200mV.
- V_{DD1} and V_{DD2} must be greater than V_{DDQ} - 200mV.
- V_{REF} must always be less than all other supply voltages.

2. CKE and Clock

Beginning at Tb, CKE must remain low for at least t_{INIT1} = 100 ns, after which it may be asserted high. Clock must be stable at least t_{INIT2} = 5 x t_{CK} prior to the first low to high transition of CKE (Tc). CKE, CS_n and CA inputs must observe setup and hold time (t_{IS}, t_{IH}) requirements with respect to the first rising clock edge (as well as to the subsequent falling and rising edges).

The clock period shall be within the range defined for t_{CKb} (18ns to 100ns), if any Mode Register Reads are performed. Mode Register Writes can be sent at normal clock operating frequencies so long as all AC Timings are met. Furthermore, some AC parameters (e.g. t_{DQSCK}) may have relaxed timings (e.g. t_{DQSCKb}) before the system is appropriately configured.

While keeping CKE high, issue NOP commands for at least t_{INIT3} = 200us. (Td).

3. Reset command

After t_{INIT3} is satisfied, a MRW (Reset) command shall be issued (Td). The memory controller may optionally issue a Precharge-All command prior to the MRW Reset command. Wait for at least t_{INIT4} = 1us while keeping CKE asserted and issuing NOP commands.

4. Mode Registers Reads and Device Auto-Initialization (DAI) polling

After t_{INIT4} is satisfied (Te), only MRR commands and power down entry/exit commands are allowed. Therefore, after Te, CKE may go low in accordance to power down entry and exit specification. (See “Power Down” section)

The MRR command may be used to poll the DAI bit to acknowledge when device auto-Initialization is complete or the memory controller shall wait a minimum of t_{INIT5} before proceeding.

As the memory output buffers are not properly configured yet, some AC parameters may have relaxed timings before the system is appropriately configured.

After the DAI bit (MR0, “DAI”) is set to zero ”DAI complete” by the memory device, the device is in idle state (Tf). The state of the DAI status bit can be determined by an MRR command to MR0.

The device will set the DAI bit no later than t_{INIT5} after the RESET command. The memory controller shall wait a minimum of t_{INIT5} or until the DAI bit is set before proceeding.

After the DAI bit is set, it is recommended to determine the device type and other device characteristics by issuing MRR commands (MR0 “Device Information” etc.).

5. ZQ Calibration

After t_{INIT5} (Tf), an MRW ZQ Initialization Calibration command may be issued to the memory (MR10).

This command is used to calibrate the LPDDR2 output drivers (R_{ON}) over process, voltage, and temperature variations. Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate R_{ZQ} pin connection. In systems in which more than one LPDDR2 device exists on the same bus, the controller must not overlap ZQ Calibration commands. The device is ready for normal operation after t_{ZQINIT}.

6. Normal Operation

After t_{ZQINIT} (Tg), MRW commands may be used to properly configure the memory (for example the output buffer driver strength, latencies, etc). Specifically, MR1, MR2, and MR3 shall be set to configure the memory for the target frequency and memory configuration.

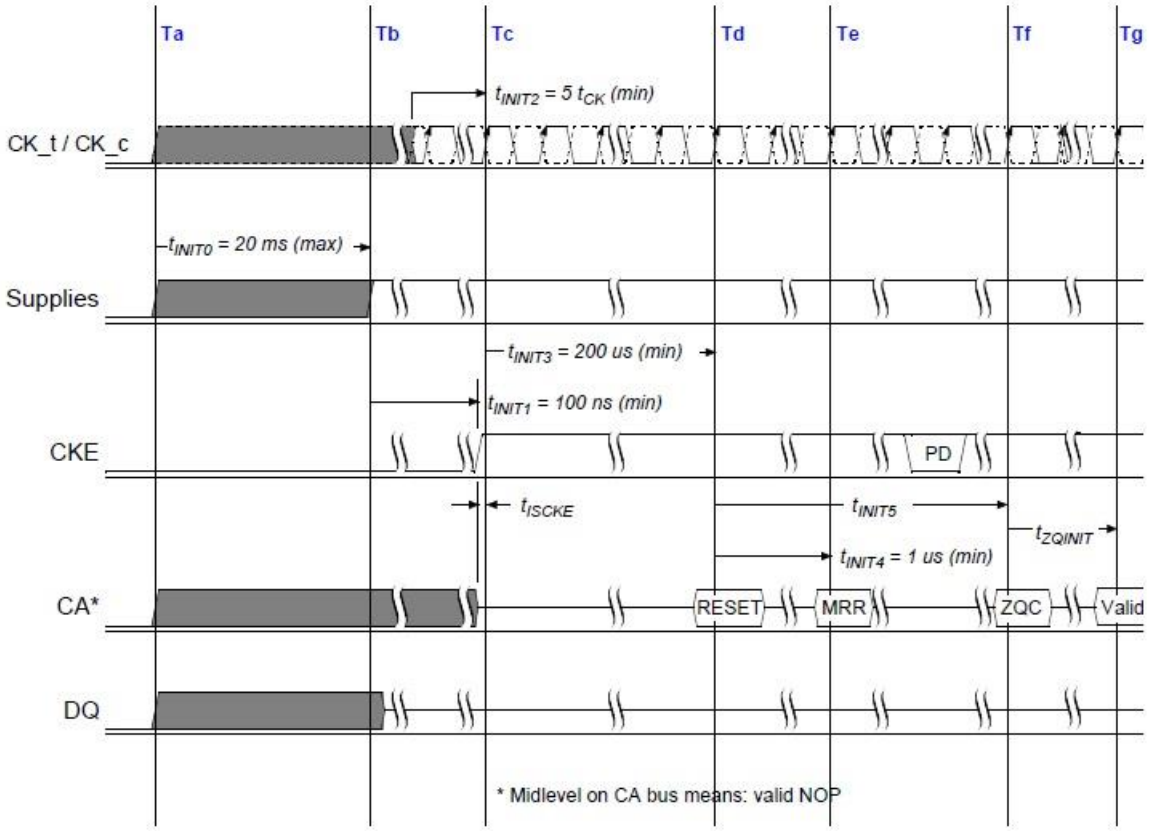
The LPDDR2 device will now be in IDLE state and ready for any valid command.

After Tg, the clock frequency may be changed according to the clock frequency change procedure described in “Input clock stop and frequency change” section.

Table of Timing Parameters for initialization

Symbol	Value		Unit	Comment
	min	max		
t_{INIT0}		20	ms	Maximum Power Ramp Time
t_{INIT1}	100		ns	Minimum CKE low time after completion of power ramp
t_{INIT2}	5		t_{CK}	Minimum stable clock before first CKE high
t_{INIT3}	200		us	Minimum Idle time after first CKE assertion
t_{INIT4}	1		us	Minimum Idle time after Reset command
t_{INIT5}		10	us	Maximum duration of Device Auto-Initialization
t_{ZQINIT}	1		us	ZQ Initial Calibration for LPDDR2-S4
t_{CKb}	18	100	ns	Clock cycle time during boot

Figure of Power Ramp and Initialization Sequence



Initialization after Reset (without Power ramp)

If the RESET command is issued outside the power up initialization sequence, the reinitialization procedure shall begin with step 3 (Td).

Power Off Sequence

While removing power, CKE shall be held at a logic low level (=< 0.2 x V_{DDCA}), all other inputs shall be between $V_{IL\ min}$ and $V_{IH\ max}$. The device will only guarantee that outputs are in a high impedance state while CKE is held low.

DQ, DM, DQS_t and DQS_c voltage levels must be between V_{SSQ} and V_{DDQ} during power off sequence to avoid latchup. CK_t, CK_c, CS_n and CA input levels must be between V_{SSCA} and V_{DDCA} during power off sequence to avoid latchup.

Tx is the point where any power supply decreases under its minimum value specified in the Table of "Recommended DC Operating Conditions".

Tz is the point where all power supplies are below 300 mV. After Tz, the device is powered off.

The time between Tx and Tz (t_{POFF}) shall be less than 2s.

The following conditions apply between Tx and Tz:

- V_{DD1} must be greater than V_{DD2} - 200 mV.
- V_{DD1} and V_{DD2} must be greater than V_{DDCA} - 200 mV.
- V_{DD1} and V_{DD2} must be greater than V_{DDQ} - 200 mV.
- V_{REF} must always be less than all other supply voltages.

The voltage difference between any of V_{SS}, V_{SSQ}, and V_{SSCA} pins may not exceed 100 mV.

For supply and reference voltage operating conditions, see the Table of "Recommended DC Operating Conditions".

Table of Timing Parameters Power Off

Symbol	Value		Unit	Comment
	min	max		
t_{POFF}		2	s	Maximum power off ramp time

Uncontrolled Power Off Sequence

The following sequence shall be used to power off the LPDDR2 device under uncontrolled condition.

- Tx is the point where any power supply decreases under its minimum value specified in the DC operating condition table. After turning off all power supplies, any power supply current capacity must be zero, except for any static charge remaining in the system.
- Tz is the point where all power supply first reaches 300 mV. After Tz, the device is powered off. The time between Tx and Tz shall be less than t_{POFF}. The relative voltage between supply voltages is uncontrolled during this period. V_{DD1} and V_{DD2} shall decrease with a slope lower than 0.5 V/us between Tx and Tz.

Uncontrolled power off sequence can be applied only up to 400 times in the life of the device.

Mode Register Definition

Mode Register Assignment and Definition

Each register is denoted as “R” if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written.

Mode Register Read command is used to read a register. Mode Register Write command is used to write a register.

Table of Mode Register Assignment [*1~5]

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
0	00h	Device Info.	R	(RFU)			RZQI		DNVI	DI	DAI	go to MR0
1	01h	Device Feature 1	W	nWR (for AP)			WC	BT	BL			go to MR1
2	02h	Device Feature 2	W	(RFU)				RL & WL				go to MR2
3	03h	I/O Config-1	W	(RFU)				DS				go to MR3
4	04h	SDRAM Refresh Rate	R	TUF	(RFU)				Refresh Rate			go to MR4
5	05h	Basic Config-1	R	LPDDR2 Manufacturer ID								go to MR5
6	06h	Basic Config-2	R	Revision ID1								go to MR6
7	07h	Basic Config-3	R	Revision ID2								go to MR7
8	08h	Basic Config-4	R	I/O width		Density				Type		go to MR8
9	09h	Test Mode	W	Vendor-Specific Test Mode								go to MR9
10	0Ah	I/O Calibration	W	Calibration Code								go to MR10
11~15	0Bh~0Fh	(Reserved)		(RFU)								go to MR11
16	10h	PASR_Bank	W	Bank Mask								go to MR16
17	11h	PASR_Seg	W	Segment Mask								go to MR17
18~19	12h~13h	(Reserved)		(RFU)								go to MR18
20~31	14h~1Fh	Reserved for NVM										MR20~MR30
32	20h	DQ Calibration Pattern A	R	See “DQ Calibration” section								go to MR32
33:39	21h~27h	(Do Not Use)										go to MR33
40	28h	DQ Calibration Pattern B	R	See “DQ Calibration” section								go to MR40
41:47	29h~2Fh	(Do Not Use)										go to MR41
48:62	30h~3Eh	(Reserved)		(RFU)								go to MR48
63	3Fh	Reset	W	X								go to MR63
64:126	40h~7Eh	(Reserved)		(RFU)								go to MR64
127	7Fh	(Do Not Use)										go to MR127
128:190	80h~BEh	(Reserved for vendor use)		(RFU)								go to MR128
191	BFh	(Do Not Use)										go to MR191
192:254	C0h~FEh	(Reserved for vendor use)		(RFU)								go to MR192
255	FFh	(Do Not Use)										go to MR255

Notes:

1. RFU bits must be set to '0' during Mode Register Write.
2. RFU bits must be read as '0' during Mode Register Read.
3. All Mode Registers that are specified as RFU or write-only shall return undefined data when read and DQS_t, DQS_c shall be toggled.
4. All Mode Registers that are specified as RFU shall not be written.
5. Writes to read-only registers shall have no impact on the functionality of the device.

MR0_Device Information (MA[7:0] = 00h) *1~4

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)			RZQI		DNVI	DI	DAI

DAI (Device Auto-Initialization Status)	Read-only	OP0	**0b:** DAI complete **1b:** DAI still in progress
DI (Device Information)	Read-only	OP1	**0b:** S2 or S4 SDRAM **1b:** NVM
DNVI (Data Not Valid Information)	Read-only	OP2	**0b**: DNVI not supported
RZQI (Built in Self Test for R_{ZQ} Information)	Read-only	OP[4:3]	**00b:** R_{ZQ} self test not supported **01b:** ZQ pin may connect to V_{DDCA} or float **10b:** ZQ pin may short to GND **11b:** ZQ pin self test completed, no error condition detected (ZQ pin may not connect to V_{DDCA} or float nor short to GND)

Notes:

1. If RZQI is supported, it will be set upon completion of the MRW ZQ Initialization Calibration command.
2. If ZQ is connected to V_{DDCA} to set default calibration, OP[4:3] must be set to 01. If ZQ is not connected to V_{DDCA}, either OP[4:3]=01 or OP[4:3]=10 might indicate a ZQ pin assembly error. It is recommended that the assembly error is corrected.
3. In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10 as defined above), the device will default to factory trim settings for R_{ON} and will ignore ZQ calibration commands. In either case, the system may not function as intended.
4. In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e. 240ohm +/-1%).

MR1_Device Feature 1 (MA[7:0] = 01h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR (for AP)			WC	BT	BL		

BL (Burst Length)	Write-only	OP[2:0]	**010b:** BL4 (default) **011b:** BL8 **100b:** BL16 **All others:** reserved
BT (Burst Type)	Write-only	OP3	**0b:** Sequential (default) **1b:** Interleaved
WC (Wrap Control)	Write-only	OP4	**0b:** Wrap (default) **1b:** No wrap
nWR (Number of t_{WR} Clock Cycles) *1	Write-only	OP[7:5]	**001b:** nWR=3 (default) **010b:** nWR=4 **011b:** nWR=5 **100b:** nWR=6 **101b:** nWR=7 **110b:** nWR=8 **All others:** reserved

Notes:

1. Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(t_{WR}/t_{CK}).

Table of Burst Sequence by Burst Length (BL), Burst Type (BT), and Warp Control (WC)[*1~5]

BL	BT	C3	C2	C1	C0	WC	Burst Cycle Number and Burst Address Sequence															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
4	any	X	X	0b	0b	wrap	0	1	2	3												
		X	X	1b	0b		2	3	0	1												
		X	X	X	0b	nw	y	y+1	y+2	y+3												
8	seq	X	0b	0b	0b	wrap	0	1	2	3	4	5	6	7								
		X	0b	1b	0b		2	3	4	5	6	7	0	1								
		X	1b	0b	0b		4	5	6	7	0	1	2	3								
		X	1b	1b	0b		6	7	0	1	2	3	4	5								
	int	X	0b	0b	0b		0	1	2	3	4	5	6	7								
		X	0b	1b	0b		2	3	0	1	6	7	4	5								
		X	1b	0b	0b		4	5	6	7	0	1	2	3								
		X	1b	1b	0b		6	7	4	5	2	3	0	1								
	any	X	X	X	0b	nw	**illegal (not allowed)**															
16	seq	0b	0b	0b	0b	wrap	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		0b	0b	1b	0b		2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1
		0b	1b	0b	0b		4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
		0b	1b	1b	0b		6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5
		1b	0b	0b	0b		8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
		1b	0b	1b	0b		A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9
		1b	1b	0b	0b		C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
		1b	1b	1b	0b		E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D
	int	X	X	X	0b		**illegal (not allowed)**															
	any	X	X	X	0b	nw	**illegal (not allowed)**															

Notes:

1. C0 input is not present on CA bus. It is implied zero.
2. For BL=4, the burst address represents C[1: 0].
3. For BL=8, the burst address represents C[2:0].
4. For BL=16, the burst address represents C[3:0].
5. For no-wrap (nw), BL4, the burst must not cross the page boundary or sub-page boundary. The variable y may start at any address with C0 equal to 0 and must not start at any address in table below for the respective density and bus width combinations.

Table of Non Wrap Restrictions

	1Gb
Not across full page boundary	
x32	1FE, 1FF, 000, 001
Not across sub-page boundary	
x32	None

Note: Non-wrap BL=4 data orders shown above are prohibited.

MR2_Device Feature 2 (MA[7:0] = 02h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				RL & WL			

RL & WL	Write-only	OP[3:0]	**0001b:** RL = 3 / WL = 1 (default) **0010b:** RL = 4 / WL = 2 **0011b:** RL = 5 / WL = 2 **0100b:** RL = 6 / WL = 3 **0101b:** RL = 7 / WL = 4 **0110b:** RL = 8 / WL = 4 **All others:** reserved

MR3_I/O Configuration 1 (MA[7:0] = 03h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				DS			

DS	Write-only	OP[3:0]	**0000b:** reserved **0001b:** 34.3 ohm typical **0010b:** 40 ohm typical (default) **0011b:** 48 ohm typical **0100b:** 60 ohm typical **0101b:** reserved **0110b:** 80-ohm typical **0111b:** 120-ohm typical (optional) **All others:** reserved

MR4_Device Temperature (MA[7:0] = 04h) [*1~8]

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	(RFU)				SDRAM Refresh Rate		

SDRAM Refresh Rate	Read-only	OP[2:0]	**000b:** SDRAM Low temperature operating limit exceeded **001b:** 4x t_{REFI}, 4x t_{REFIpb}, 4x t_{REFW} **010b:** 2x t_{REFI}, 2x t_{REFIpb}, 2x t_{REFW} **011b:** 1x t_{REFI}, 1x t_{REFIpb}, 1x t_{REFW} (<=85 ℃) **100b:** Reserved **101b:** 0.25x t_{REFI}, 0.25x t_{REFIpb}, 0.25x t_{REFW}, do not derate SDRAM AC timing **110b:** 0.25x t_{REFI}, 0.25x t_{REFIpb}, 0.25x t_{REFW}, derate SDRAM AC timing **111b:** SDRAM High temperature operating limit exceeded
Temperature Update Flag (TUF)	Read-only	OP[7]	**0b:** OP[2:0] value has not changed since last read of MR4. **1b:** OP[2:0] value has changed since last read of MR4.

Notes:

1. A Mode Register Read from MR4 will reset OP7 to '0'.
2. OP7 is reset to '0' at power up. OP[2:0] bits are undefined after power up.
3. If OP2 equals '1', the device temperature is greater than 85 ℃.
4. OP7 is set to '1' if OP[2:0] has changed at any time since the last read of MR4.
5. The device might not operate properly when OP[2:0] = 000b or 111b.
6. For specified operating temperature range and maximum operating temperature refer to the Table of "Operating Temperature Range".
7. The devices shall be derated by adding 1.875 ns to the following core timing parameters: t_{RCD}, t_{RC}, t_{RAS}, t_{RP}, and t_{RRD}. t_{DQSCK} must be derated according to the t_{DQSCK} derating in the Table of "AC timing". Prevailing clock frequency specifications and related setup and hold timings shall remain unchanged.
8. The recommended frequency for reading MR4 is provided in "Temperature Sensor" section.

MR5_Basic Configuration 1 (MA[7:0] = 05h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
LPDDR2 Manufacturer ID							

LPDDR2 Manufacturer ID	Read-only	OP[7:0]	**0000 1001b**

MR6_Basic Configuration 2 (MA[7:0] = 06h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1							

Revision ID1	Read-only	OP[7:0]	**0000 0000b:** A-version

Note: MR6 is vendor-specific.

MR7_Basic Configuration 3 (MA[7:0] = 07h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2							

Revision ID2	Read-only	OP[7:0]	**0000 0000b:** A-version

Note: MR7 is vendor-specific.

MR8_Basic Configuration 4 (MA[7:0] = 08h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Type	Read-only	OP[1:0]	**00b:** S4 SDRAM
Density	Read-only	OP[5:2]	**0100b:** 1Gb
I/O width	Read-only	OP[7:6]	**00b:** x32 **01b:** x16

MR9_Test Mode (MA[7:0] = 09h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specific Test Mode							

MR10_Calibration (MA[7:0] = 0Ah) *1~4

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							

Calibration Code	Write-only	OP[7:0]	**0xFF:** Calibration command after initialization **0xAB:** Long calibration **0x56:** Short calibration **0xC3:** ZQ Reset **others:** Reserved

Notes:

1. Host processor must not write MR10 with “Reserved” values.
2. The device ignores calibration commands when a “Reserved” value is written into MR10.
3. See the Table of “AC timing” for the calibration latency.
4. If ZQ is connected to V_{SSCA} through R_{ZQ}, either the ZQ calibration function (see “Mode Register Write ZQ Calibration Command” section) or default calibration (through the ZQreset command) is supported. If ZQ is connected to V_{DDCA}, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection must not change after power is applied to the device.

MR16_PASR_Bank Mask (MA[7:0] = 10h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank Mask (8-bank)							

Bank [7:0] Mask	Write-only	OP[7:0]	**0b:** refresh enable to the bank (=unmasked, default) **1b:** refresh blocked (=masked)

OP	Bank Mask	8-Bank SDRAM
0	XXXXXXX1	**Bank 0**
1	XXXXXX1X	**Bank 1**
2	XXXXX1XX	**Bank 2**
3	XXXX1XXX	**Bank 3**
4	XXX1XXXX	**Bank 4**
5	XX1XXXXX	**Bank 5**
6	X1XXXXXX	**Bank 6**
7	1XXXXXXX	**Bank 7**

MR17_PASR_Segment Mask (MA[7:0] = 11h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment mask							

Segment [7:0] Mask	Write-only	OP[7:0]	**0b:** refresh enable to the segment (=unmasked, default) **1b:** refresh blocked (=masked)

Segment	OP	Segment Mask	R12:10
0	0	XXXXXXX1	000b
1	1	XXXXXX1X	001b
2	2	XXXXX1XX	010b
3	3	XXXX1XXX	011b
4	4	XXX1XXXX	100b
5	5	XX1XXXXX	101b
6	6	X1XXXXXX	110b
7	7	1XXXXXXX	111b

Note: X is “Don’t Care” for the designated segment.

MR32_DQ Calibration Pattern A (MA[7:0] = 20h)

Reads to MR32 return DQ Calibration Pattern “A”. See “DQ Calibration” section.

MR40_DQ Calibration Pattern B (MA[7:0] = 28h)

Reads to MR40 return DQ Calibration Pattern “B”. See “DQ Calibration” section.

MR63_Reset (MA[7:0] = 3Fh): MRW only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
X							

Note: For additional information on MRW RESET, see “Mode Register Write Command” section.

Table of Reserved Mode Registers

Mode Register	MA	Address	Restriction	OP[7:0]
MR[11:15]	MA[7:0]	0Bh-0Fh	RFU	Reserved
MR[18:19]		12h–13h	RFU	
MR[20:31]		14h–1Fh	NVM (DNU)	
MR[33:39]		21h–27h	DNU	
MR[41:47]		29h–2Fh	DNU	
MR[48:62]		30h–3Eh	RFU	
MR[64:126]		40h–7Eh	RFU	
MR127		7Fh	DNU	
MR[128:190]		80h–BEh	RVU	
MR191		BFh	DNU	
MR[192:254]		C0h–FEh	RVU	
MR255		FFh	DNU	

Note: NVM = nonvolatile memory use only; DNU = Do not use; RVU = Reserved for vendor use.

Command Definitions and Timing Diagram

Activate Command

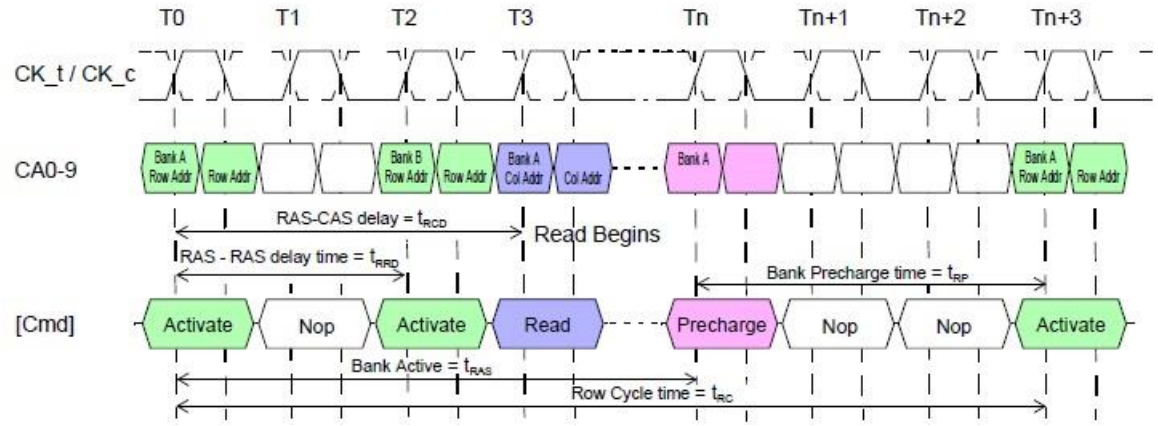
The Activate command is issued by holding CS_n LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses are used to select the desired bank. The row addresses are used to determine which row to activate in the selected bank. The Activate command must be applied before any Read or Write operation can be executed. The device can accept a read or write command at time t_{RCD} after the activate command is sent. Once a bank has been activated it must be precharged before another Activate command can be applied to the same bank. The bank active and precharge times are defined as t_{RAS} and t_{RP}, respectively. The minimum time interval between successive Activate commands to the same bank is determined by the RAS cycle time of the device (t_{RC}). The minimum time interval between Activate commands to different banks is t_{RRD}.

Certain restrictions on operation of the 8-bank devices must be observed. There are two rules. One for restricting the number of sequential Activate commands that can be issued and another for allowing more time for RAS precharge for a Precharge All command. The rules are as follows:

- 8-bank device Sequential Bank Activation Restriction: No more than 4 banks may be activated (or refreshed, in the case of REFpb) in a rolling t_{FAW} window. Converting to clocks is done by dividing t_{FAW} [ns] by t_{CK} [ns], and rounding up to next integer value. As an example of the rolling window, if RU{ (t_{FAW} / t_{CK}) } is 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued at or between clock N+1 and N+9. REFpb also counts as bank-activation for the purposes of t_{FAW}.

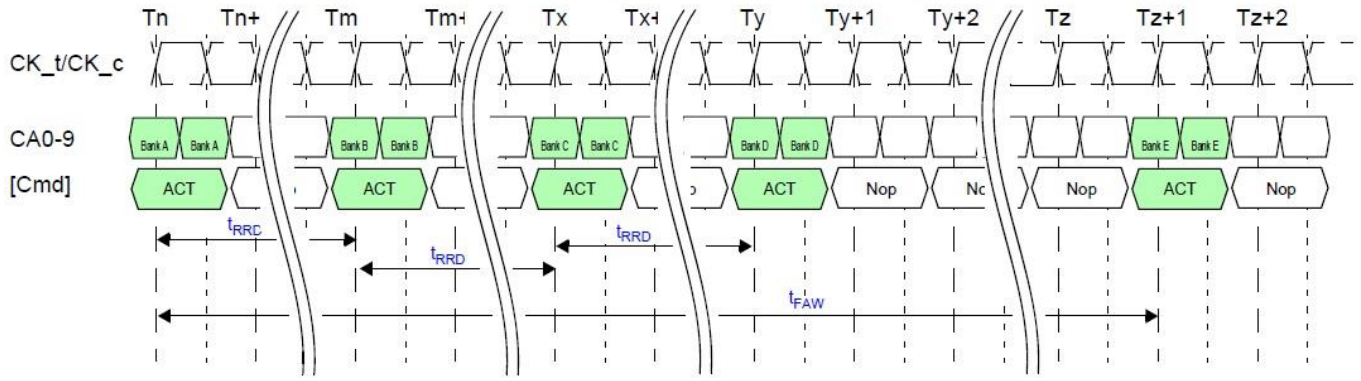
- 8-bank device Precharge All Allowance: t_{RP} for a Precharge All command for an 8-bank device shall equal t_{RPab}, which is greater than t_{RPpb}.

Figure of Activate command cycle: t_{RCD}=3, t_{RP}=3, t_{RRD}=2



Note: A Precharge-All command uses t_{RPab} timing, while a Single Bank Precharge command uses t_{RPpb} timing. In this figure, t_{RP} is used to denote either an All-bank Precharge or a Single Bank Precharge

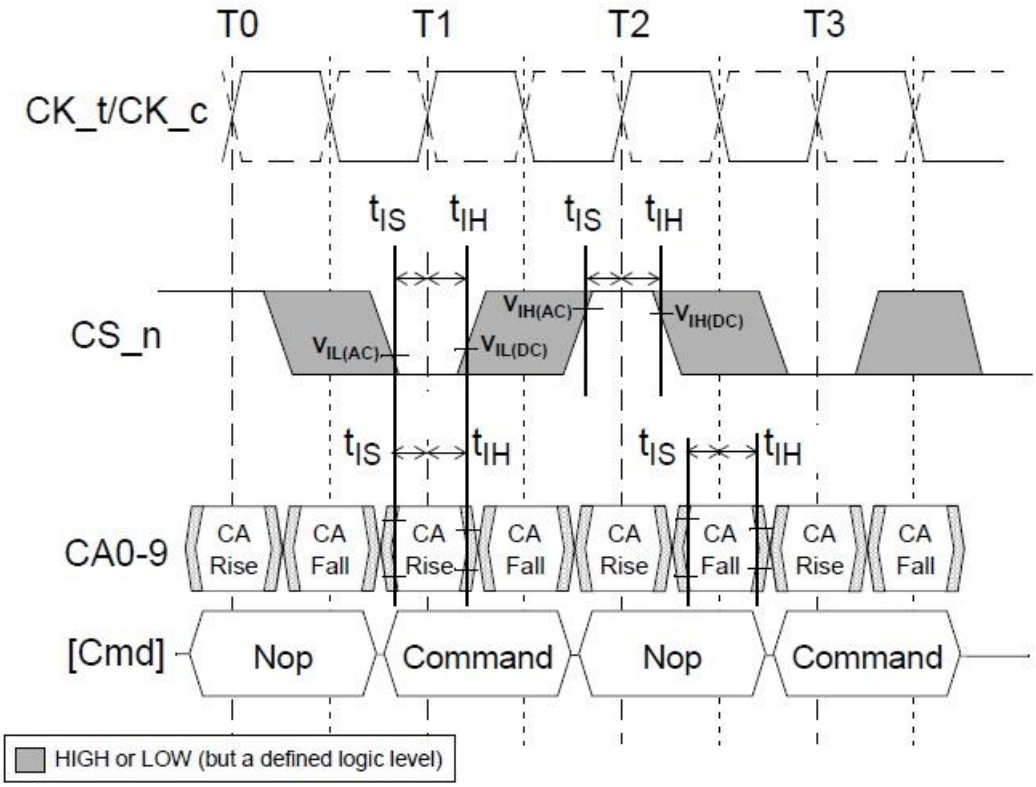
Figure of t_{FAW} timing



Note: For 8-bank devices only.

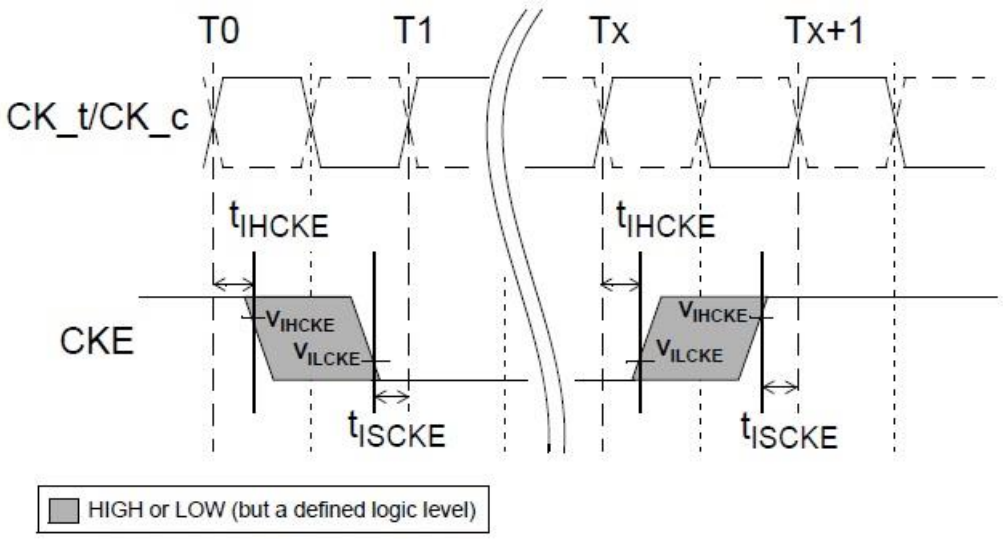
Command Input Signal Timing Definition

Figure of Command Input Setup and Hold Timing



Note: Setup and hold conditions also apply to the CKE pin. See section related to power down for timing diagrams related to the CKE pin.

Figure of CKE Input Setup and Hold Timing



Notes:

1. After CKE is registered LOW, CKE signal level must be maintained below V_{ILCKE} for t_{CKE} specification (LOW pulse width).
2. After CKE is registered HIGH, CKE signal level must be maintained above V_{IHCKE} for t_{CKE} specification (HIGH pulse width)

Read and Write access modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting CS_n LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a READ operation (CA2 HIGH) or a WRITE operation (CA2 LOW).

The device provides a fast column access operation. A single Read or Write Command initiates a burst read or write operation on successive clock cycles.

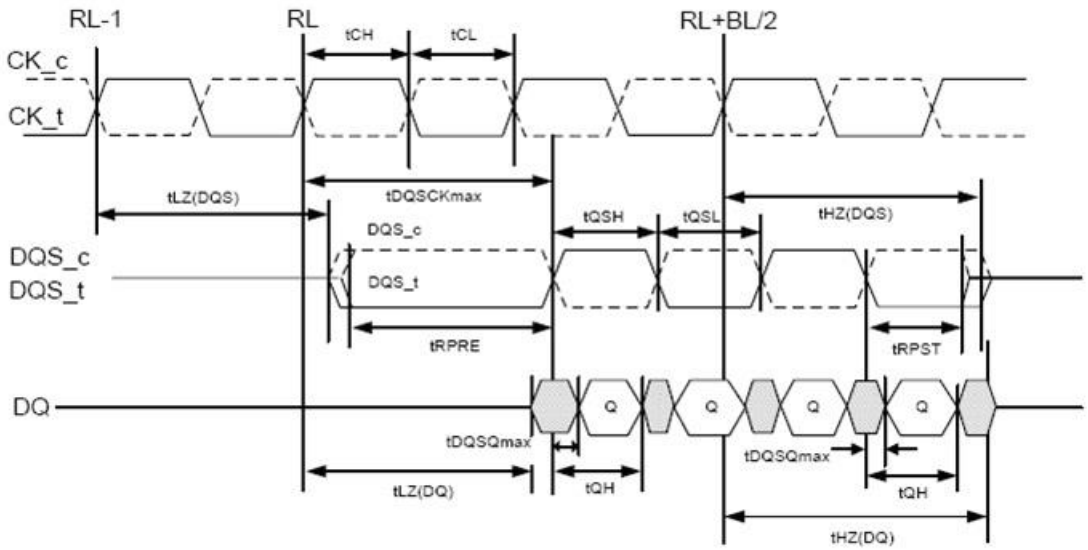
A new burst access must not interrupt the previous 4-bit burst operation in case of BL = 4 setting. In case of BL = 8 and BL = 16 settings, Reads may be interrupted by Reads and Writes may be interrupted by Writes, provided that this occurs on even clock cycles after the Read or Write command and t_{CCD} is met.

Burst Read command

The Burst Read command is initiated by having CS_n LOW, CA0 HIGH, CA1 LOW and CA2 HIGH at the rising edge of the clock. The command address bus inputs, CA5r-CA6r and CA1f-CA9f, determine the starting column address for the burst. The Read Latency (RL) is defined from the rising edge of the clock on which the Read Command is issued to the rising edge of the clock from which the t_{DQSCK} delay is measured. The first valid datum is available RL * t_{CK} + t_{DQSCK} + t_{DQSQ} after the rising edge of the clock where the Read Command is issued. The data strobe output is driven LOW t_{RPRE} before the first rising valid strobe edge. The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin edge aligned with the data strobe. The RL is programmed in the mode registers.

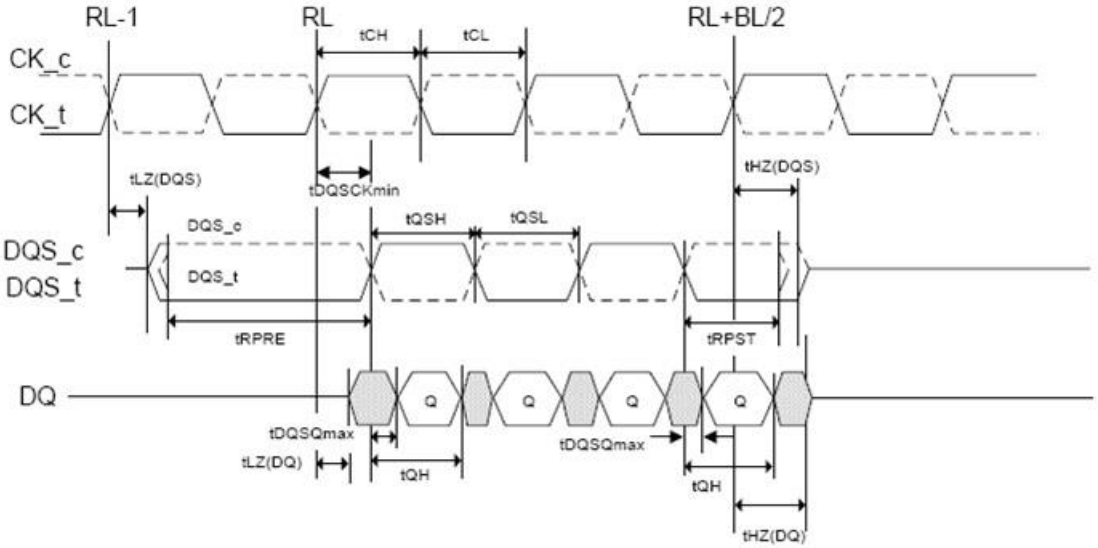
Timings for the data strobe are measured relative to the crosspoint of DQS_t and its complement, DQS_c.

Figure of Data output (read) timing ($t_{DQSCK\ max}$)



Notes:
1. t_{DQSCK} may span multiple clock periods.
2. An effective Burst Length of 4 is shown

Figure of Data output (read) timing ($t_{DQSCK\ min}$)



Note: An effective Burst Length of 4 is shown

Figure of Burst read: RL = 5, BL = 4, $t_{DQSCK} > t_{CK}$

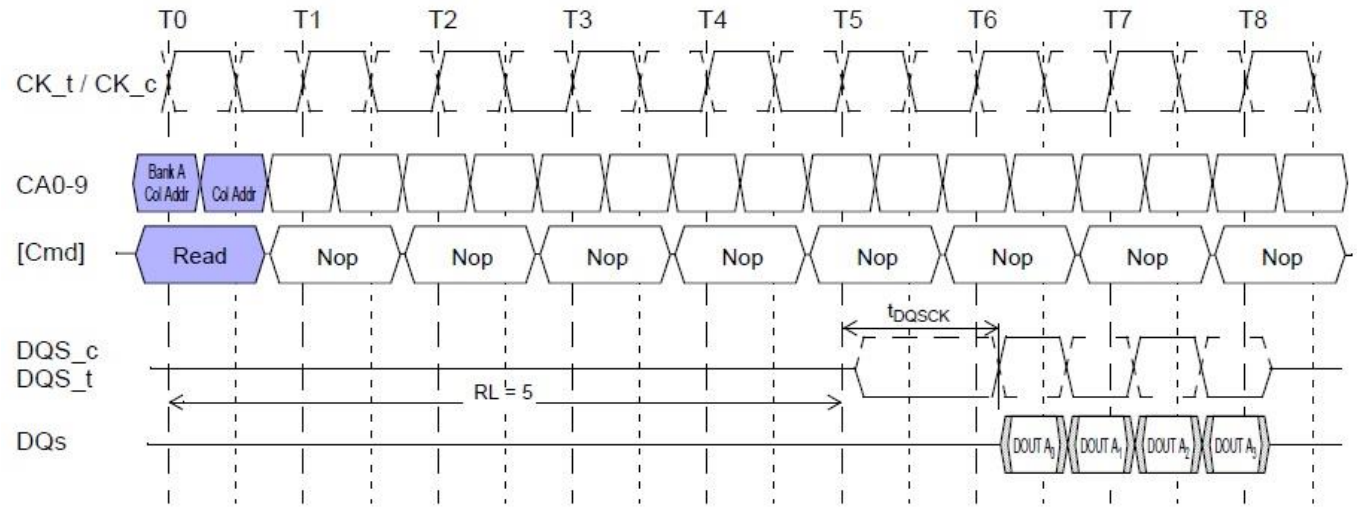


Figure of Burst read: RL = 3, BL = 8, $t_{DQSCK} < t_{CK}$

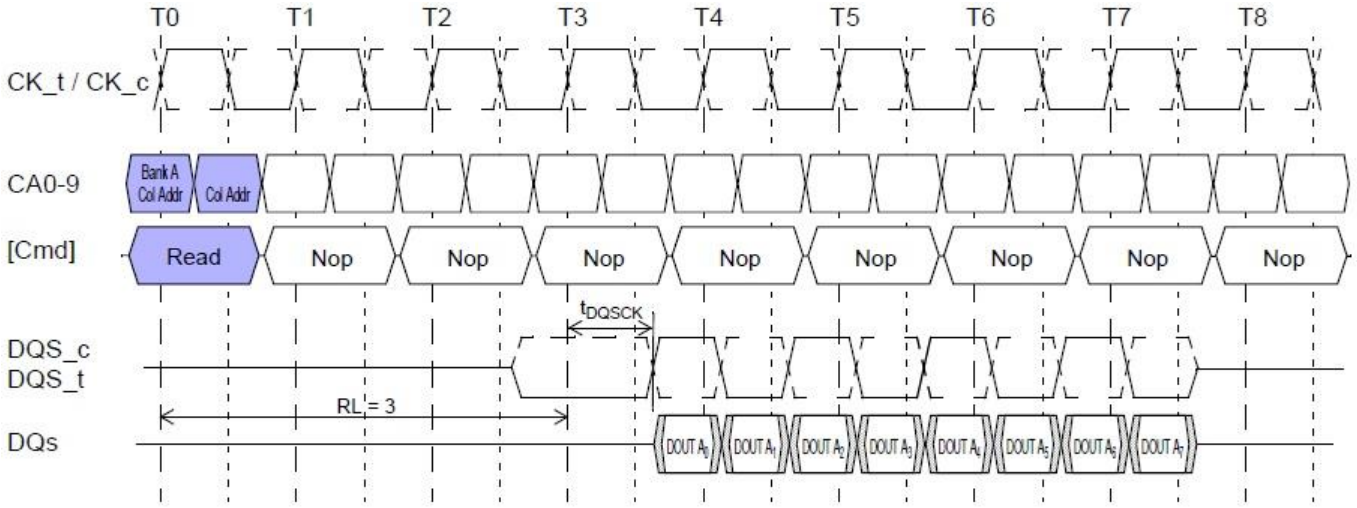
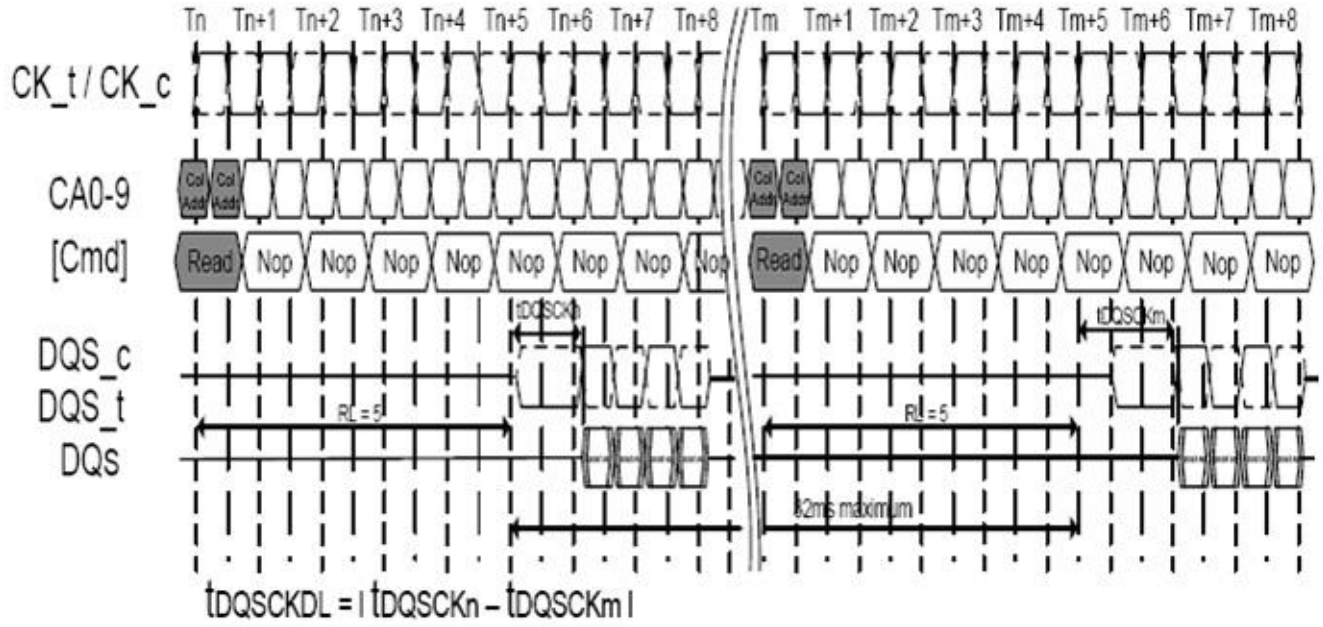
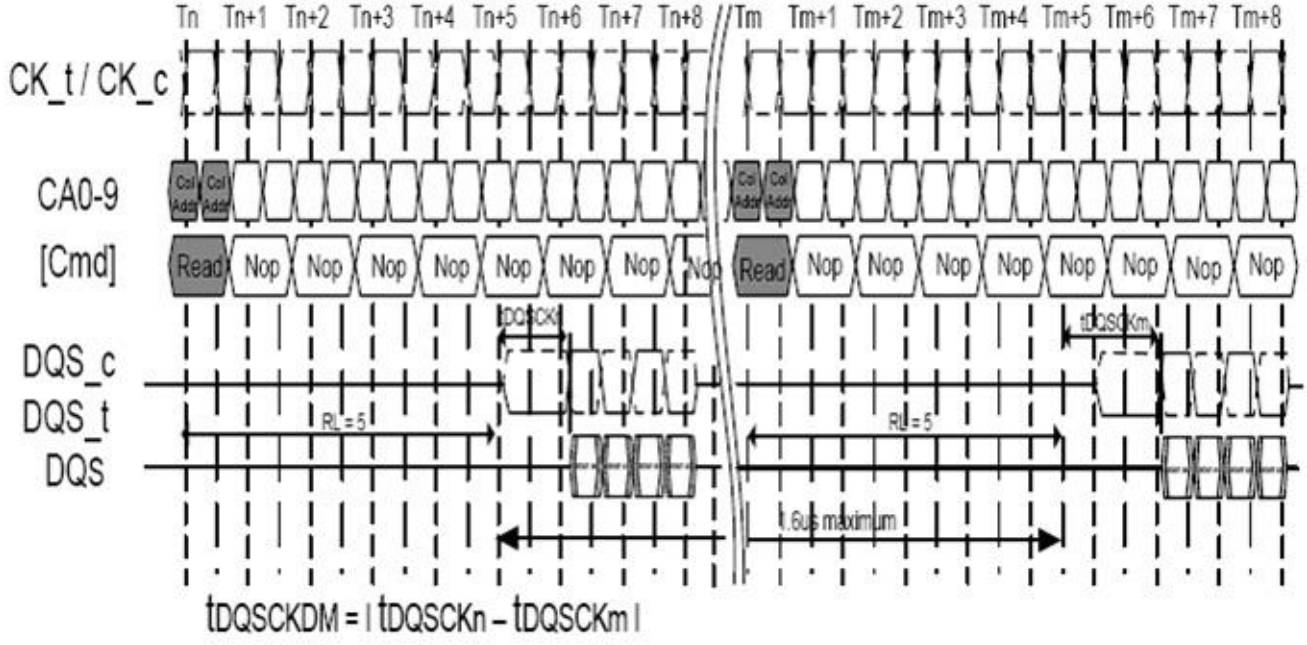


Figure of $t_{DQSCKDL}$ timing



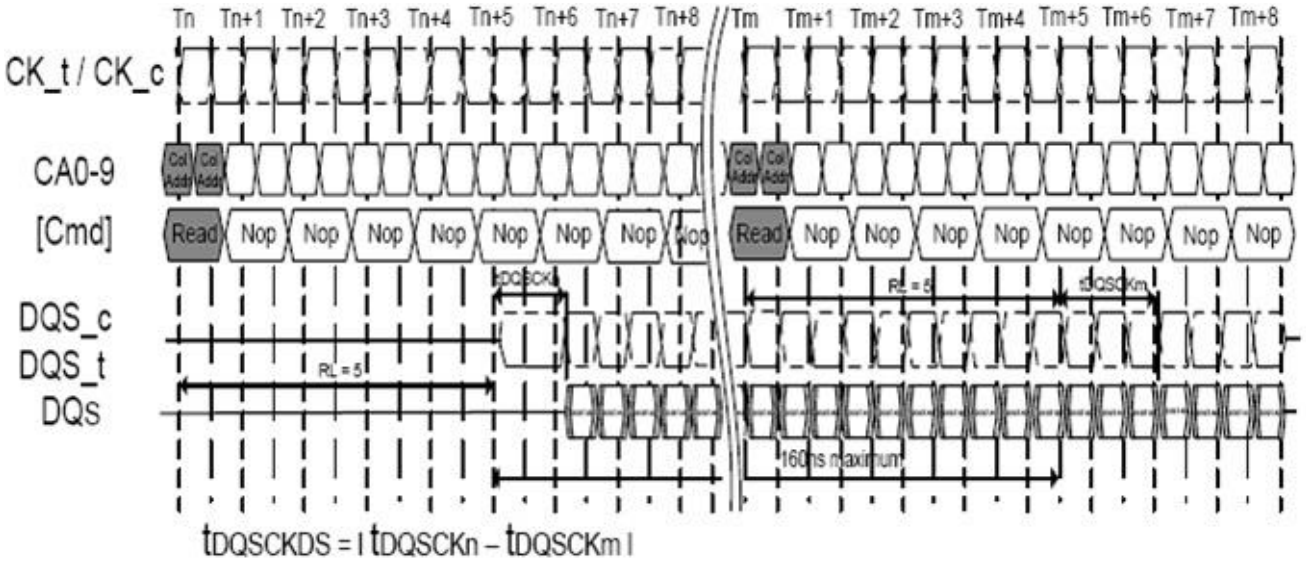
Note: $t_{DQSCKDL, max}$ is defined as the maximum of ABS (t_{DQSCKn} - t_{DQSCKm}) for any {t_{DQSCKn}, t_{DQSCKm}} pair within any 32ms rolling window.

Figure of $t_{DQSCKDM}$ timing



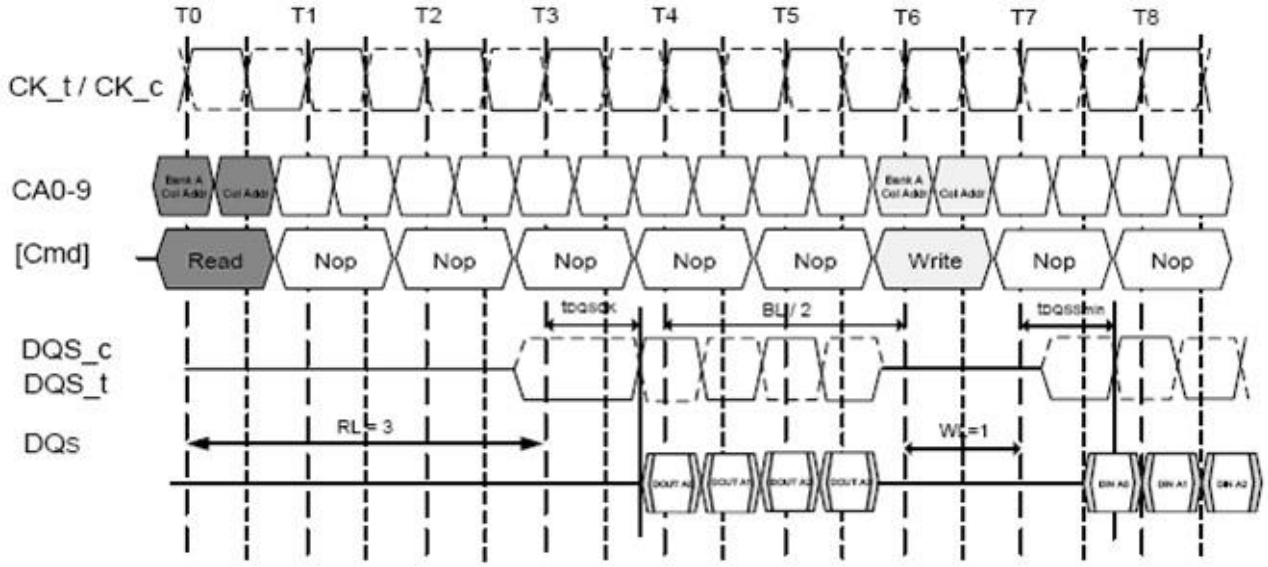
Note: $t_{DQSCKDM, max}$ is defined as the maximum of ABS (t_{DQSCKn} - t_{DQSCKm}) for any {t_{DQSCKn}, t_{DQSCKm}} pair within any 1.6us rolling window.

Figure of $t_{DQSCKDS}$ timing



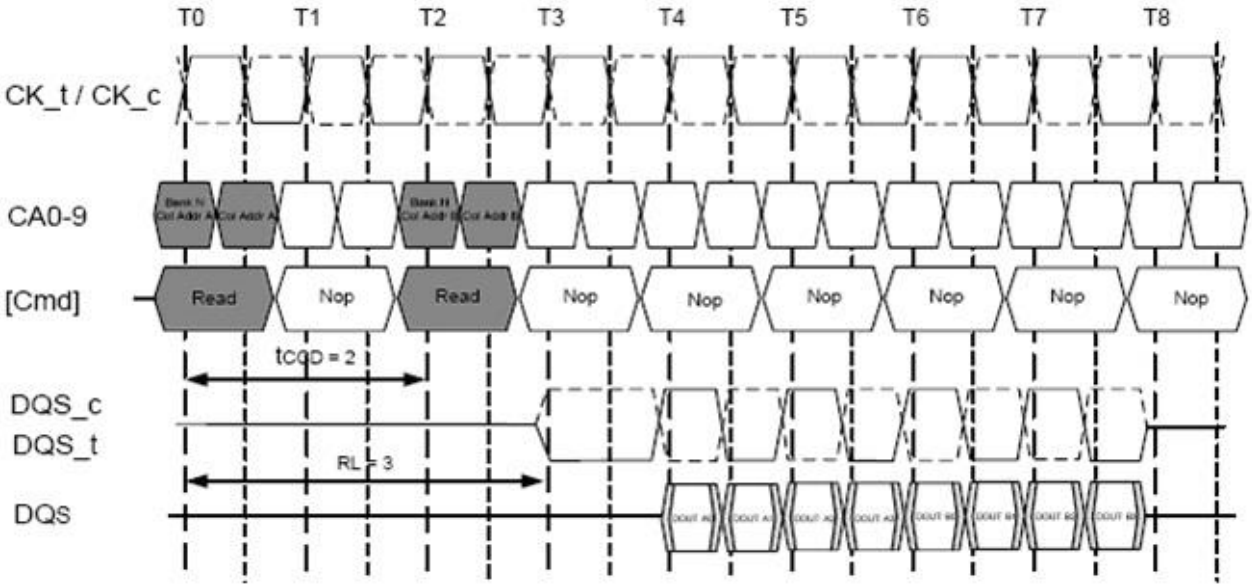
Note: $t_{DQSCKDS, max}$ is defined as the maximum of ABS (t_{DQSCKn} - t_{DQSCKm}) for any {t_{DQSCKn}, t_{DQSCKm}} pair for reads within a consecutive burst within any 160ns rolling window.

Figure of Burst read followed by burst write: RL = 3, WL = 1, BL = 4



The minimum time from the burst read command to the burst write command is defined by the Read Latency (RL) and the Burst Length (BL). Minimum read to write latency is RL + RU ($t_{DQSCK, max}$ / t_{CK}) + BL/2 + 1 - WL clock cycles. Note that if a read burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated read burst should be used as "BL" to calculate the minimum read to write delay.

Figure of Seamless burst read: RL = 3, BL= 4, t_{CCD} = 2

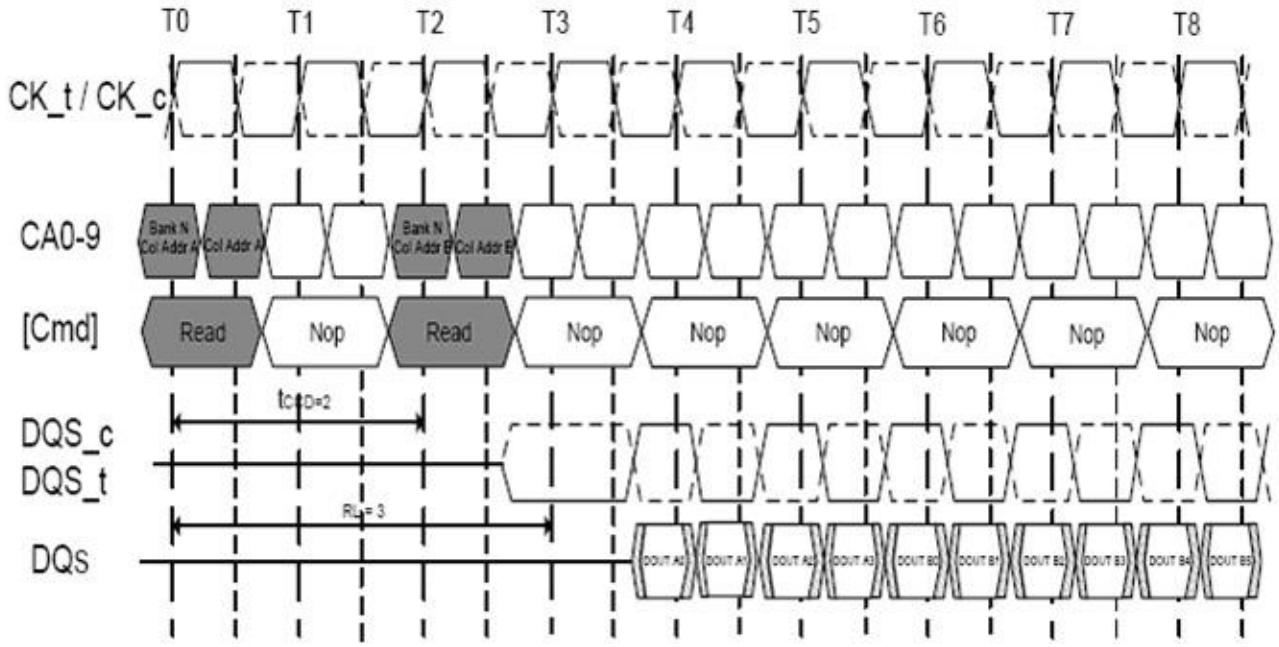


The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, every 4th clocks for BL = 8 operation, and every 8th clocks for BL=16 operation. This operation is allowed regardless of whether the accesses read the same or different banks as long as the banks are activated.

Reads interrupted by a read

A burst read can be interrupted by another read on even clock cycles after the Read command, provided that t_{CCD} is met.

Figure of Read burst interrupt example: RL = 3, BL= 8, t_{CCD} = 2



Notes:

1. Read burst interrupt function is only allowed on burst of 8 and burst of 16.
2. Read burst interrupt may only occur on even clock cycles after the previous commands, provided that t_{CCD} is met.
3. Reads can only be interrupted by other reads or the BST command.
4. Read burst interruption is allowed to any bank inside DRAM.
5. Read burst with Auto-Precharge is not allowed to be interrupted.
6. The effective burst length of the first read equals two times the number of clock cycles between the first read and the interrupting read.

Burst Write operation

The Burst Write command is initiated by having CS_n LOW, CA0 HIGH, CA1 LOW and CA2 LOW at the rising edge of the clock. The command address bus inputs, CA5r-CA6r and CA1f-CA9f, determine the starting column address for the burst. The Write Latency (WL) is defined from the rising edge of the clock on which the Write Command is issued to the rising edge of the clock from which the t_{DQSS} delay is measured. The first valid data must be driven WL * t_{CK} + t_{DQSS} from the rising edge of the clock from which the Write command is issued. The data strobe signal (DQS) must be driven LOW t_{WPRE} prior to the data input. The data bits of the burst cycle must be applied to the DQ pins t_{DS} prior to the respective edge of the DQS and held valid until t_{DH} after that edge. The burst data is sampled on successive edges of the DQS until the burst length is completed, which is 4, 8, or 16 bit burst.

t_{WR} must be satisfied before a precharge command to the same bank may be issued after a burst write operation.
Input timings are measured relative to the crosspoint of DQS_t and its complement, DQS_c.

Figure of Data input (write) timing

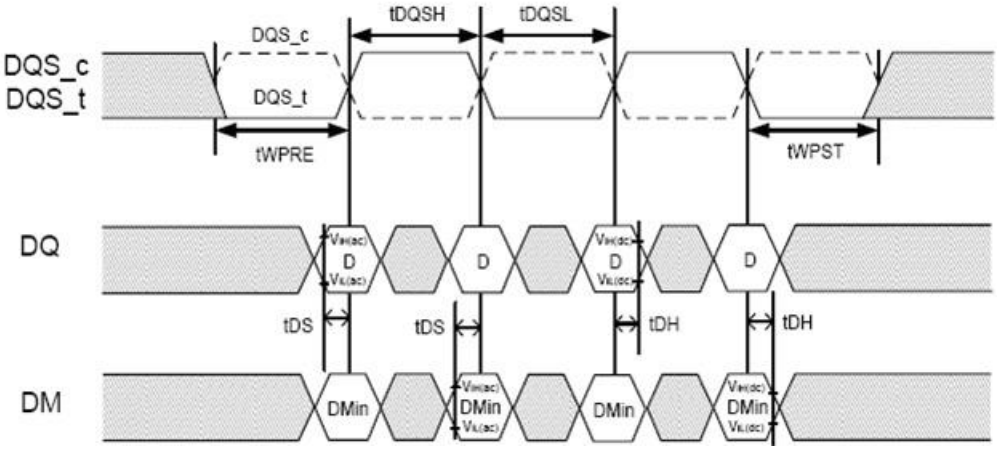


Figure of Burst write: WL = 1, BL= 4

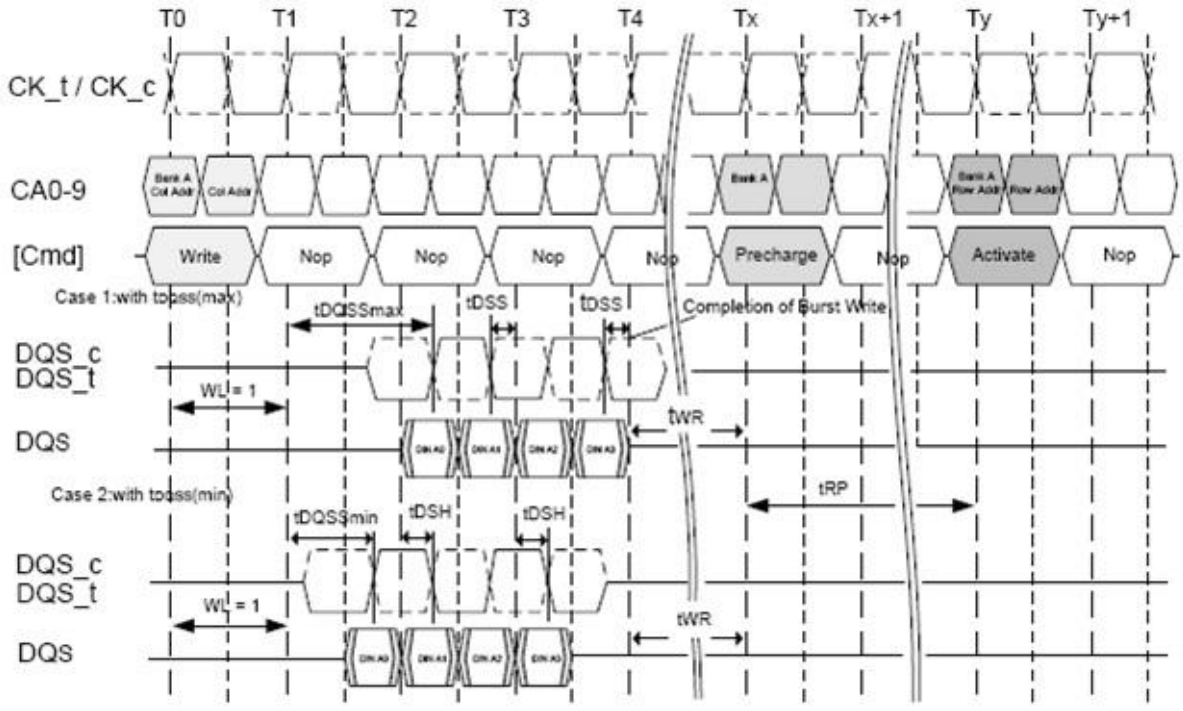
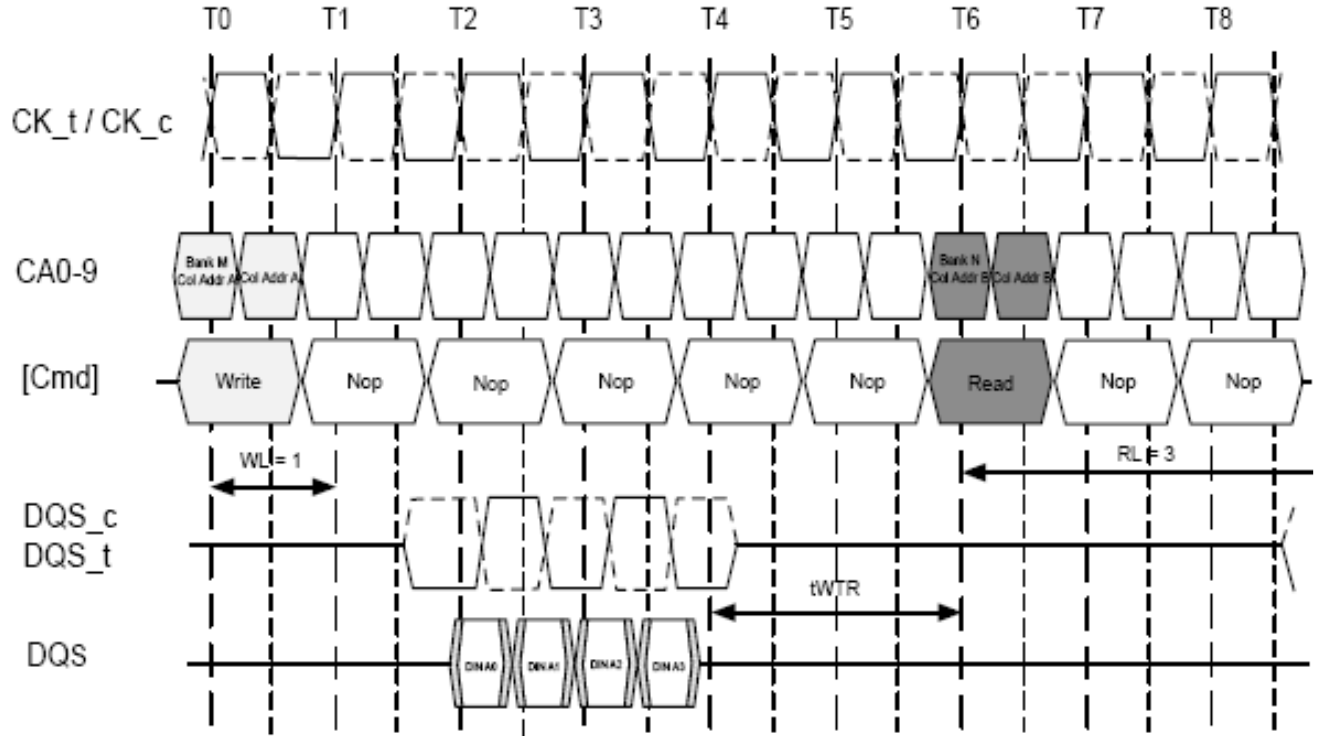


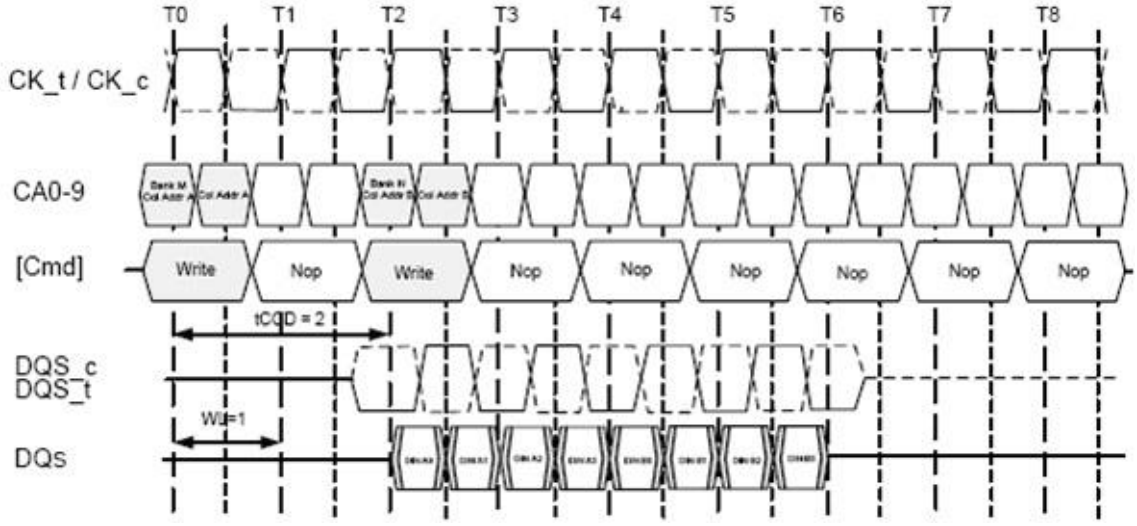
Figure of Burst write followed by burst read: RL = 3, WL= 1, BL=4



Notes:

1. The minimum number of clock cycles from the burst write command to the burst read command for any bank is [WL + 1 + BL/2 + RU(t_{WTR} / t_{CK})].
2. t_{WTR} starts at the rising edge of the clock after the last valid input datum.
3. If a write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated write burst should be used as “BL” to calculate the minimum write to read delay.

Figure of Seamless burst write: WL= 1, BL=4, t_{CCD}=2

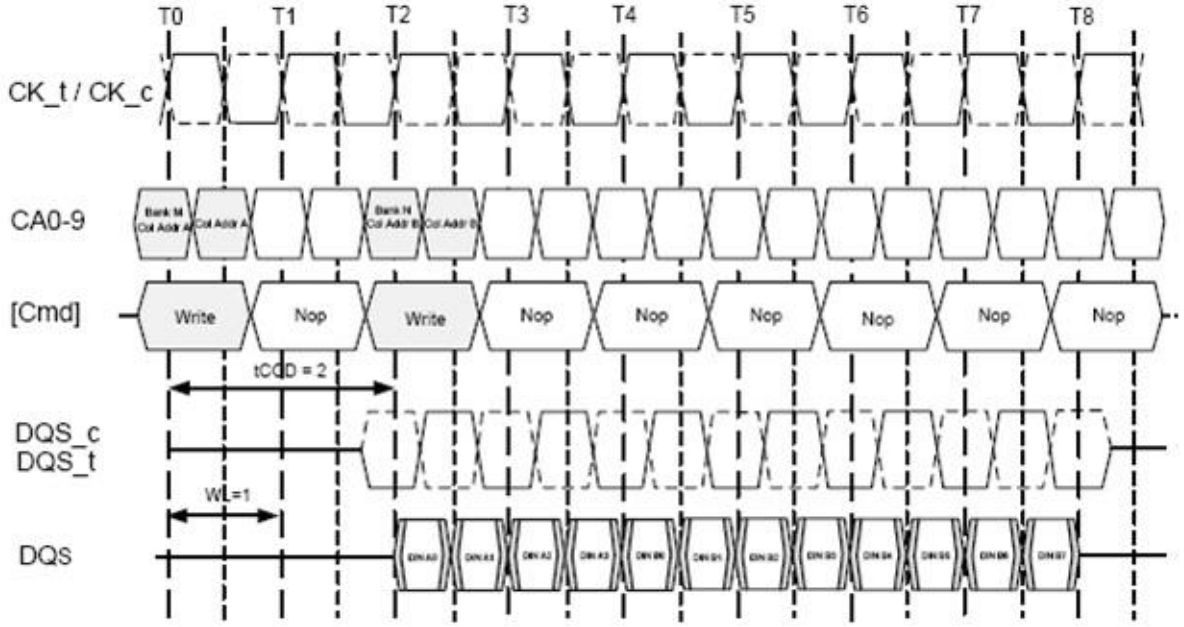


Note: The seamless burst write operation is supported by enabling a write command every other clock for BL = 4 operation, every four clocks for BL = 8 operation, or every eight clocks for BL=16 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Writes interrupted by a write

A burst writes can only be interrupted by another write on even clock cycles after the write command, provided that $t_{CCD(min)}$ is met.

Figure of Write burst interrupt timing: WL= 1, BL= 8, t_{CCD} = 2



Notes:

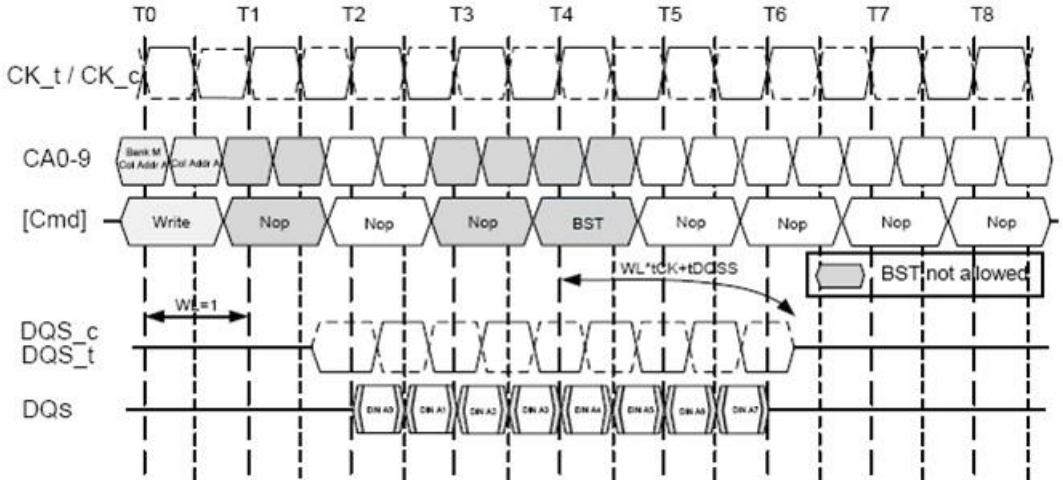
1. Write burst interrupt function is only allowed on burst of 8 and burst of 16.
2. Write burst interrupt may only occur on even clock cycles after the previous write commands, provided that $t_{CCD(min)}$ is met.
3. Writes can only be interrupted by other writes or the BST command.
4. Write burst interruption is allowed to any bank inside DRAM.
5. Write burst with Auto-Precharge is not allowed to be interrupted.
6. The effective burst length of the first write equals two times the number of clock cycles between the first write and the interrupting write.

Burst Terminate

The Burst Terminate (BST) command is initiated by having CS_n LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 LOW at the rising edge of clock. A Burst Teminate command can only be issued to terminate an active Read or Write burst. Therefore, a Burst Terminate command can only be issued up to and including BL/2 - 1 clock cycles after a Read or Write command. The effective burst length of a Read or Write command truncated by a BST command is as follows:

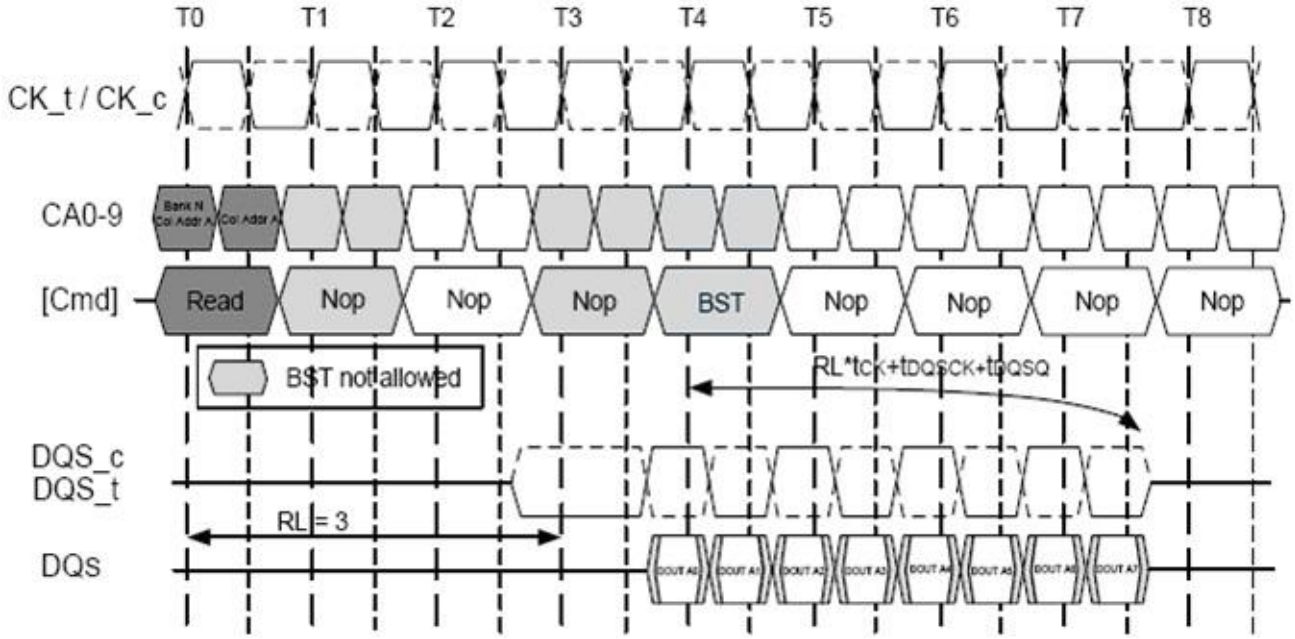
- Effective burst length = 2 x {Number of clock cycles from the Read or Write Command to the BST command}
- If a read or write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated burst should be used as "BL" to calculate the minimum read to write or write to read delay.
- The BST command only affects the most recent read or write command. The BST command truncates an ongoing read burst RL * t_{CK} + t_{DQSCK} + t_{DQSQ} after the rising edge of the clock where the Burst Terminate command is issued. The BST command truncates an on going write burst WL * t_{CK} + t_{DQSS} after the rising edge of the clock where the Burst Terminate command is issued.
- The 4-bit prefetch architecture allows the BST command to be issued on an even number of clock cycles after a Write or Read command. Therefore, the effective burst length of a Read or Write command truncated by a BST command is an integer multiple of 4.

Figure of Write burst truncated by BST: WL= 1, BL = 16



Notes:
1. The BST command truncates an ongoing write burst WL * t_{CK} + t_{DQSS} after the rising edge of the clock where the Burst Terminate command is issued.
2. Additional BST commands are not allowed after T4 and must not be issued until after the next Read or Write command.

Figure of Burst Read truncated by BST: RL= 3, BL=16



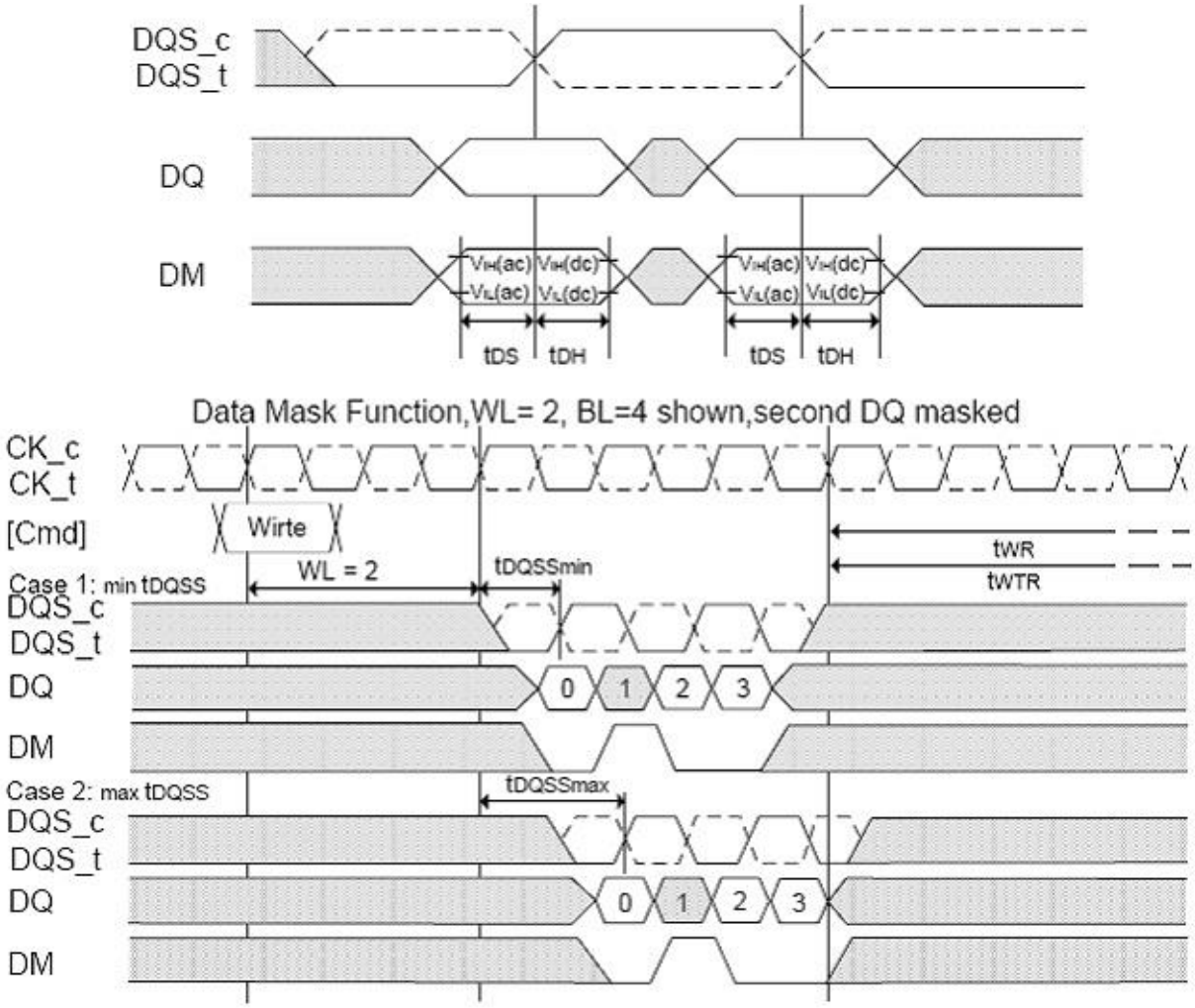
Notes:

1. The BST command truncates an ongoing read burst RL * t_{CK} + t_{DQSCK} + t_{DQSQ} after the rising edge of the clock where the Burst Terminate command is issued.
2. BST can only be issued at even number of clock cycles after the Read command.
3. Additional BST commands are not allowed after T4 and may not be issued until after the next Read or Write command.

Write data mask

One write data mask (DM) pin for each data byte (DQ) is supported on LPDDR2 devices, consistent with the implementation on LPDDR SDRAMs. Each data mask (DM) can mask its respective data byte (DQ) for any given cycle of the burst. Data mask has identical timings on write operations as the data bits, though used as input only, is internally loaded identically to data bits to ensure matched system timing.

Figure of Write data mask



Precharge operation

The Precharge command is used to precharge or close a bank that has been activated. The Precharge command is initiated by having CS_n LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. For 8-bank devices, the AB flag and the bank address bits, BA0, BA1, and BA2, are used to determine which bank(s) to precharge. The bank(s) will be available for a subsequent row access t_{RPab} after an All-Bank Precharge command is issued and t_{RPpb} after a Single-Bank Precharge command is issued.

In order to ensure that 8-bank devices do not exceed the instantaneous current supplying capability of 4-bank devices, the Row Precharge time (t_{RP}) for an All-Bank Precharge for 8-bank devices (t_{RPab}) will be longer than the Row Precharge time for a Single-Bank Precharge (t_{RPpb}).

Figure of "Activate command cycle: t_{RCD}=3, t_{RP}=3, t_{RRD}=2" shows Activate to Precharge timing.

Table of Bank selection for Precharge by address bits

AB (CA4r)	BA2 (CA9r)	BA1 (CA8r)	BA0 (CA7r)	Precharged Bank(s) 8-bank device
0	0	0	0	Bank 0 only
0	0	0	1	Bank 1 only
0	0	1	0	Bank 2 only
0	0	1	1	Bank 3 only
0	1	0	0	Bank 4 only
0	1	0	1	Bank 5 only
0	1	1	0	Bank 6 only
0	1	1	1	Bank 7 only
1	DON'T CARE	DON'T CARE	DON'T CARE	All Banks

Burst Read operation followed by Precharge

For the earliest possible precharge, the precharge command may be issued BL/2 clock cycles after a Read command. For an untruncated burst, BL is the value from the Mode Register. For a truncated burst, BL is the effective burst length. A new bank active command can be issued to the same bank after the Row Precharge time (t_{RP}). A precharge command cannot be issued until after t_{RAS} is satisfied.

The minimum Read to Precharge timing (t_{RTP}) must also satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a Read command.

t_{RTP} begins BL/2 - 2 clock cycles after the Read command. If the burst is truncated by a BST command or a Read command to a different bank, the effective BL is used to calculate when t_{RTP} begins.

Figure of Burst read followed by Precharge: RL= 3, BL=8, RU($t_{RTP(min)}$ / t_{CK}) = 2

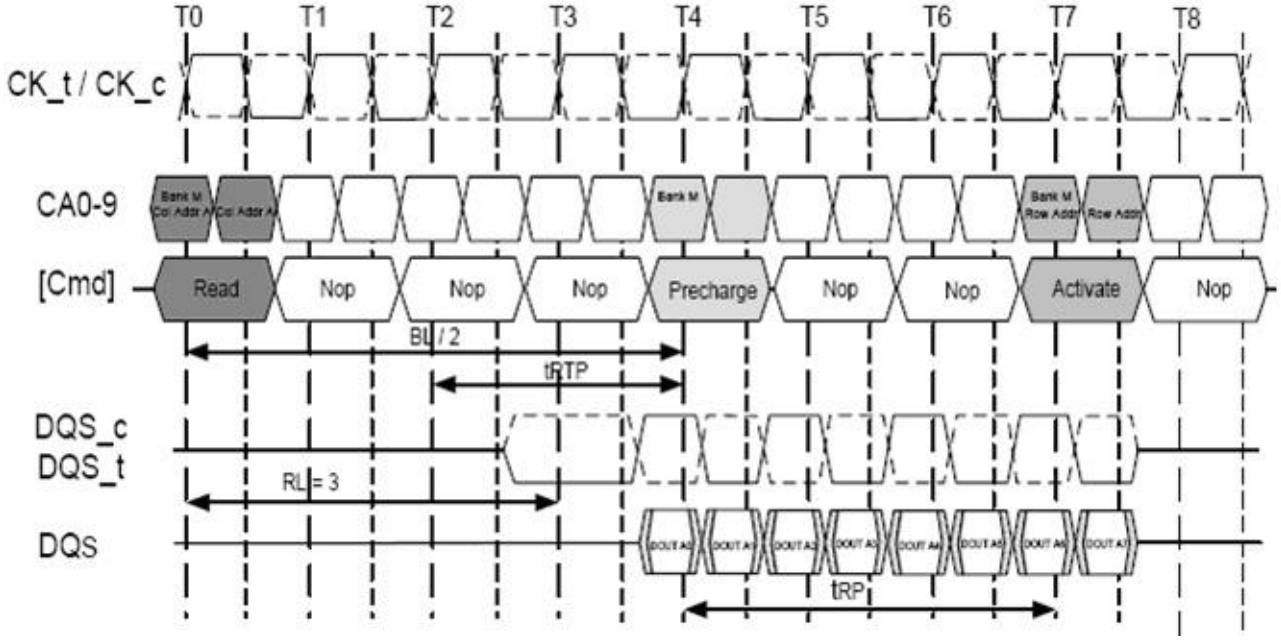
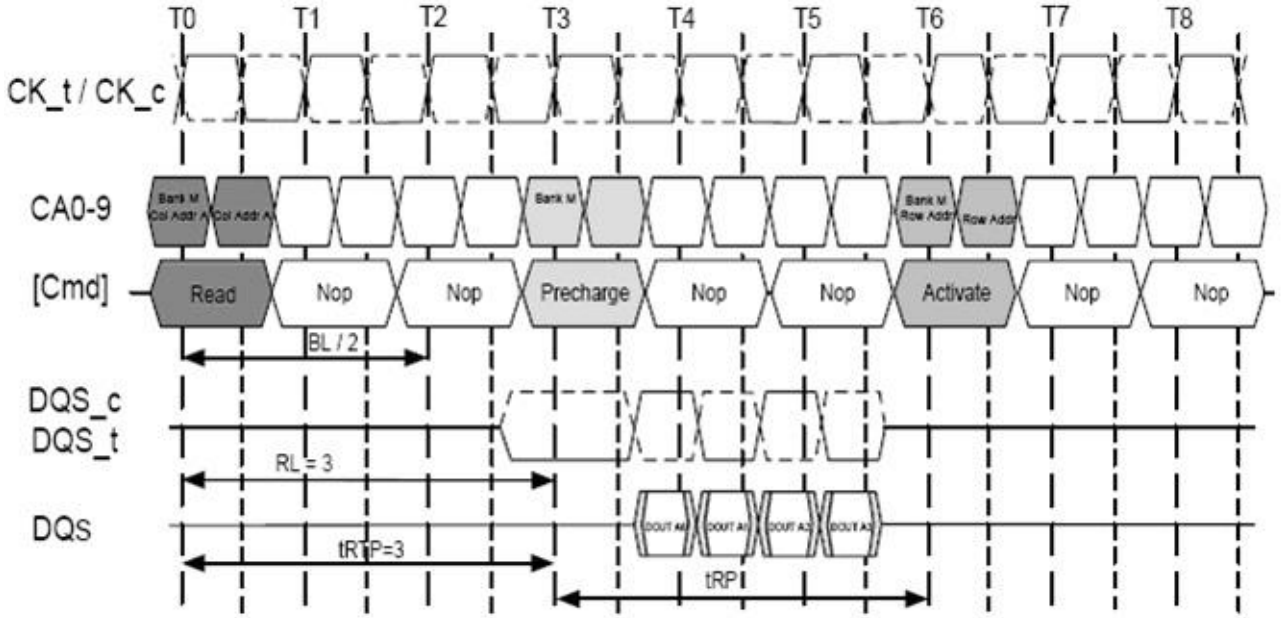


Figure of Burst read followed by Precharge: RL= 3, BL=4, RU($t_{RTP(min)}$ / t_{CK})=3



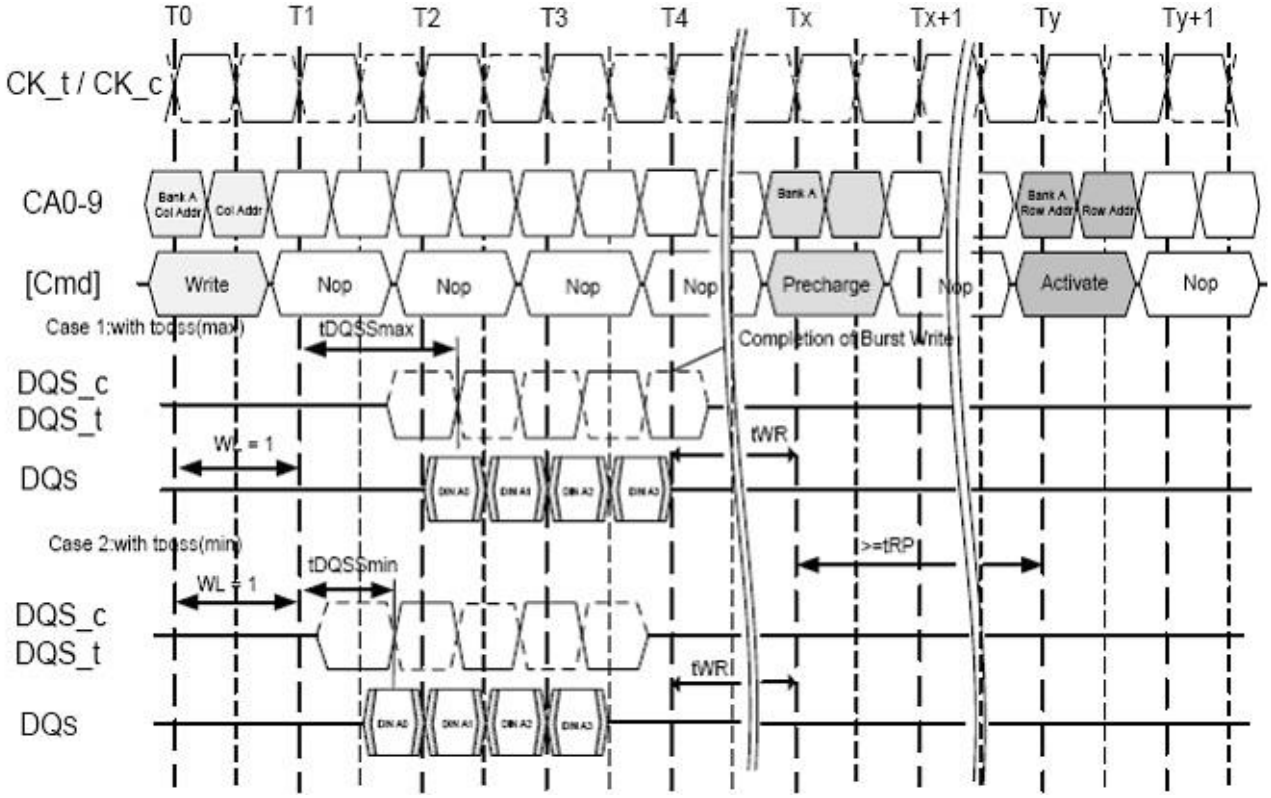
Burst Write followed by Precharge

For write cycles, a delay must be satisfied from the time of the last valid burst input data until the Precharge command may be issued. This delay is known as the write recovery time (t_{WR}) referenced from the completion of the burst write to the precharge command. No Precharge command can be issued prior to the t_{WR} delay.

These devices write data to the array in prefetch quadruples (prefetch = 4). The beginning of an internal write operation may only begin after a prefetch group has been latched completely.

The minimum Write to Precharge time for command to the same bank is WL + BL/2 + 1 + RU(t_{WR} / t_{CK}) clock cycles. For an untruncated burst, BL is the value from the Mode Register. For a truncated burst, BL is the effective burst length.

Figure of Burst write followed by precharge: WL = 1, BL= 4



Auto Precharge operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge command or the auto-precharge function. When a Read or a Write command is given to the device, the AP bit (CA0f) may be set to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle.

If AP is LOW when the Read or Write command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst.

If AP is HIGH when the Read or Write command is issued, then the auto-precharge function is engaged. This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon Read or Write latency), thus improving system performance for random data access.

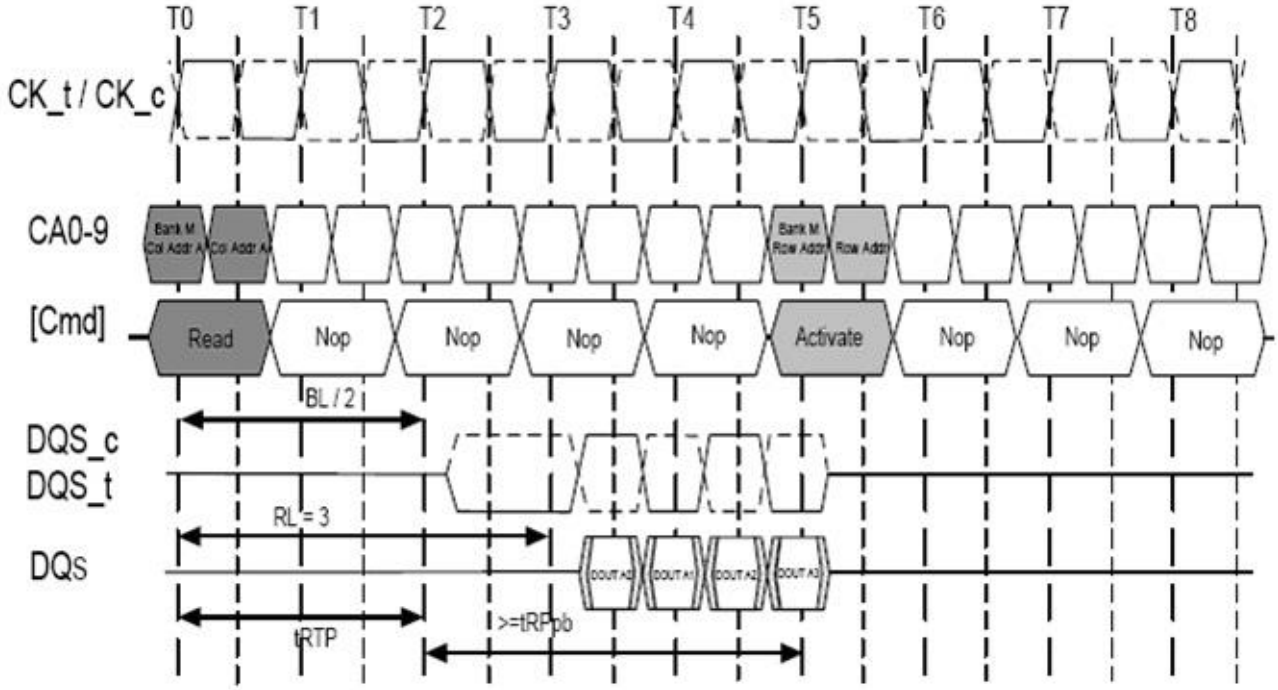
Burst Read with Auto-Precharge

If AP (CA0f) is HIGH when a Read Command is issued, the Read with Auto-Precharge function is engaged. The devices start an Auto-Precharge operation on the rising edge of the clock BL/2 or BL/2 - 2 + RU(t_{RTP} / t_{CK}) clock cycles later than the Read with AP command.

A new bank Activate command can be issued to the same bank if both of the following two conditions are satisfied simultaneously.

- The RAS precharge time (t_{RP}) has been satisfied from the clock at which the auto precharge begins.
- The RAS cycle time (t_{RC}) from the previous bank activation has been satisfied.

Figure of Burst read with Auto-Precharge: RL= 3, BL=4, RU($t_{RTP(min)}$/t_{CK})=2



Burst write with Auto-Precharge

If AP (CA0f) is HIGH when a Write Command is issued, the Write with Auto-Precharge function is engaged. The device starts an Auto Precharge operation on the rising edge which is t_{WR} cycles after the completion of the burst write.

A new bank activate command can be issued to the same bank if both of the following two conditions are satisfied.

- The RAS precharge time (t_{RP}) has been satisfied from the clock at which the auto precharge begins.
- RAS cycle time (t_{RC}) from the previous bank activation has been satisfied.

Figure of Burst write with Auto precharge: WL = 1, BL= 4

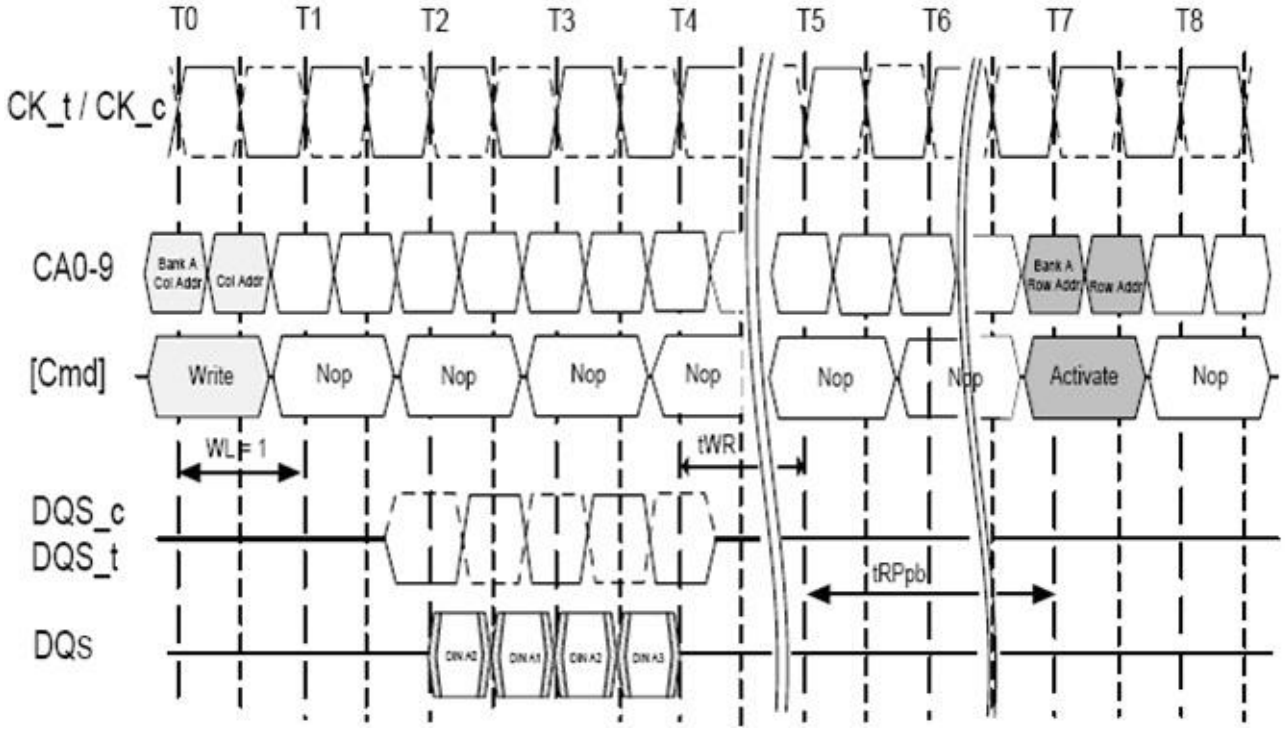


Table of Precharge & Auto Precharge Clarification

From Command	To Command	Minimum Delay Between Commands	Unit	Notes
Read	Precharge (to same Bank as Read)	BL/2 + max(2, RU(t_{RTP} / t_{CK})) - 2	CLK	1
	Precharge All	BL/2 + max(2, RU(t_{RTP} / t_{CK})) - 2	CLK	1
BST (for Reads)	Precharge (to same Bank as Read)	1	CLK	1
	Precharge All	1	CLK	1
Read w/AP	Precharge (to same Bank as Read w/AP)	BL/2 + max(2, RU(t_{RTP} / t_{CK})) - 2	CLK	1,2
	Precharge All	BL/2 + max(2, RU(t_{RTP} / t_{CK})) - 2	CLK	1
	Activate (to same Bank as Read w/AP)	BL/2 + max(2, RU(t_{RTP} / t_{CK})) - 2 + RU(t_{RPpb} / t_{CK})	CLK	1
	Write or Write w/AP (same bank)	Illegal	CLK	3
	Write or Write w/AP (different bank)	RL + BL/2 + RU($t_{DQSCKmax}$ / t_{CK}) - WL + 1	CLK	3
	Read or Read w/AP (same bank)	Illegal	CLK	3
	Read or Read w/AP (different bank)	BL/2	CLK	3
Write	Precharge (to same Bank as Write)	WL + BL/2 + RU(t_{WR} / t_{CK}) + 1	CLK	1
	Precharge All	WL + BL/2 + RU(t_{WR} / t_{CK}) + 1	CLK	1
BST (for Writes)	Precharge (to same Bank as Write)	WL + RU(t_{WR} / t_{CK}) + 1	CLK	1
	Precharge All	WL + RU(t_{WR} / t_{CK}) + 1	CLK	1
Writes w/AP	Precharge (to same Bank as Write w/AP)	WL + BL/2 + RU(t_{WR} / t_{CK}) + 1	CLK	1,2
	Precharge All	WL + BL/2 + RU(t_{WR} / t_{CK}) + 1	CLK	1
	Activate (to same Bank as Write w/AP)	WL + BL/2 + RU(t_{WR} / t_{CK}) + 1 + RU(t_{RPpb} / t_{CK})	CLK	1
	Write or Write w/AP (same bank)	Illegal	CLK	3
	Write or Write w/AP (different bank)	BL/2	CLK	3
	Read or Read w/AP (same bank)	Illegal	CLK	3
	Read or Read w/AP (different bank)	WL + BL/2 + RU(t_{WTR} / t_{CK}) + 1	CLK	3
Precharge	Precharge (to same Bank as Precharge)	1	CLK	1
	Precharge All	1	CLK	1
Precharge All	Precharge	1	CLK	1
	Precharge All	1	CLK	1

Notes:

1. For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after t_{RP} depending on the latest precharge command issued to that bank.
2. Any command issued during the minimum delay time is illegal.
3. After Read with AP, seamless read operations to different banks are supported. After Write with AP, seamless write operations to different banks are supported. Read w/AP and Write w/AP must not be interrupted or truncated.

Refresh command

The Refresh command is initiated by having CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of clock. Per Bank Refresh is initiated by having CA3 LOW at the rising edge of clock and All Bank Refresh is initiated by having CA3 HIGH at the rising edge of clock. Per Bank Refresh is only allowed in devices with 8 banks.

A Per Bank Refresh command, REFpb performs a refresh operation to the bank which is scheduled by the bank counter in the memory device. The bank sequence of Per Bank Refresh is fixed to be a sequential round-robin: "0-1-2-3-4-5-6-7-0-1-...". The bank count is synchronized between the controller and the SDRAM upon issuing a RESET command or at every exit from self refresh, by resetting bank count to zero. The bank addressing for the Per Bank Refresh count is the same as established in the single-bank Precharge command. A bank must be idle before it can be refreshed. It is the responsibility of the controller to track the bank being refreshed by the Per Bank Refresh command.

The REFpb command may not be issued to the memory until the following conditions are met:

a) t_{RFCab} has been satisfied after the prior REFab command
b) t_{RFCpb} has been satisfied after the prior REFpb command
c) t_{RP} has been satisfied after the prior Precharge command to that given bank

t_{RRD} has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a different bank than affected by the REFpb command).

The target bank is inaccessable during the Per Bank Refresh cycle time (t_{RFCpb}), however other banks within the device are accessable and can be addressed during the Per Bank Refresh cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in active state or accessed by a read or a write command.

When the Per Bank refresh cycle has completed, the affected bank will be in the Idle state after issuing REFpb:

a) t_{RFCpb} must be satisfied before issuing a REFab command
b) t_{RFCpb} must be satisfied before issuing an ACTIVATE command to the same bank
c) t_{RRD} must be satisfied before issuing an ACTIVATE command to a different bank
d) t_{RFCpb} must be satisfied before issuing another REFpb command

An All Bank Refresh command, REFab performs a refresh operation to all banks. All banks have to be in Idle state when REFab is issued (for instance, by Precharge all-bank command). REFab also synchronizes the bank count between the controller and the SDRAM to zero. The REFab command may not be issued to the memory until the following conditions have been met:

a) t_{RFCab} has been satisfied after the prior REFab command
b) t_{RFCpb} has been satisfied after the prior REFpb command
c) t_{RP} has been satisfied after prior PRECHARGE commands

When the All Bank refresh cycle has completed, all banks will be in the Idle state after issuing REFab:

a) the t_{RFCab} latency must be satisfied before issuing an ACTIVATE command
b) the t_{RFCab} latency must be satisfied before issuing a REFab or REFpb command

Table of Command Scheduling Separations related to Refresh

Symbol	Minimum delay from	To	Note
t_{RFCab}	REFab	REFab	
		Activate command to any bank	
		REFpb	
t_{RFCpb}	REFpb	REFab	
		Activate command to same bank as REFpb	
		REFpb	
t_{RRD}	REFpb	Activate command to different bank than REFpb	
	Activate	REFpb affecting an idle bank (different bank than Activate)	1
		Activate command to different bank than the prior Activate command	

Note:

1. A bank must be in the Idle state before it is refreshed. Therefore, after Activate, REFab is not allowed and REFpb is allowed only if it affects a bank which is in the Idle state.

Refresh Requirements

1. Minimum number of Refresh commands:

The device requires a minimum number, R, of Refresh (REFab) commands within any rolling Refresh Window (t_{REFW} = 32 ms @ MR4[2:0] = “011” or T_{CASE} ≤ 85 °C). See the Table of “Refresh Requirement Parameters” for actual numbers per density. The resulting average refresh interval (t_{REFI}) is given in the Table of “Refresh Requirement Parameters”.

See MR4 for t_{REFW} and t_{REFI} refresh multipliers at different MR4 settings.

For devices supporting Per-Bank-Refresh, a REFab command can be replaced by a full cycle of eight REFpb commands.

2. Burst Refresh limitation:

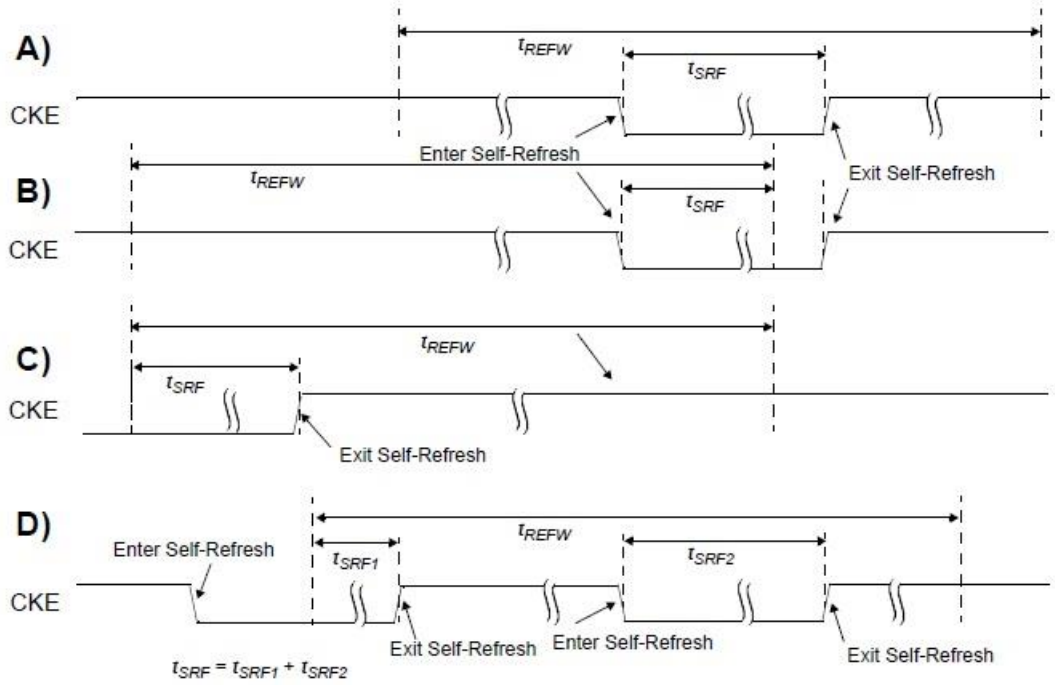
To limit maximum current consumption, a maximum of eight REFab commands can be issued in any rolling t_{REFBW} (t_{REFBW} = 4 x 8 x t_{RFCab}). This condition does not apply if REFpb commands are used.

3. Refresh Requirements and Self Refresh:

If any time within a refresh window is spent in Self Refresh Mode, the number of required Refresh commands in this particular window is reduced to:

R* = R - RU{t_{SRF} / t_{REFI}} = R - RU{R * t_{SRF} / t_{REFW}}; where RU stands for the round-up function

Figure of Definition of t_{SRF}



Several examples on how t_{SRF} is calculated:

A: with the time spent in Self Refresh Mode fully enclosed in the Refresh Window (t_{REFW}).
B: at Self Refresh entry
C: at Self Refresh exit
D: with several different invervals spent in Self Refresh during one t_{REFW} interval

The devices provide significant flexibility in scheduling REFRESH commands, as long as the boundary conditions are met.

In the most straight forward case, a REFRESH command should be scheduled every t_{REFI}. In this case, Self Refresh can be entered at any time.

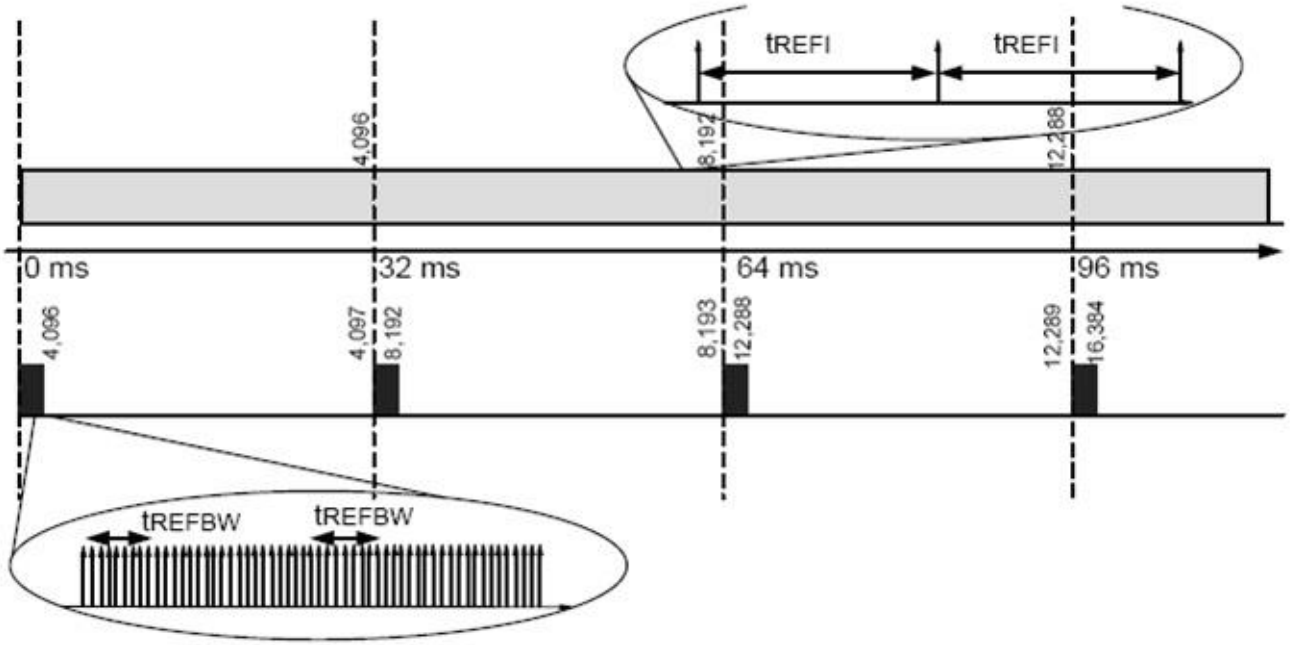
The users may choose to deviate from this regular refresh pattern e.g., to enable a period where no refreshes are required. As an example, using a 1Gb LPDDR2 device, the user can choose to issue a refresh burst of 4096 REFRESH commands with the maximum allowable rate (limited by t_{REFBW}), followed by a long time without any REFRESH commands, until the refresh window is complete, then repeating this sequence. The achieveable time without REFRESH commands is given by t_{REFW} - (R / 8) * t_{REFBW} = t_{REFW} - R * 4 * t_{RFCab}. For example, a 1Gb device at $T_{CASE} \leqq 85℃$can be operation without a refresh for up to 32 ms - 4096 * 4 * 130 ns ~ 30 ms.

While both - the regular and the burst/pause - patterns can satisfy the refresh requirements per rolling refresh interval, if they are repeated in every subsequent 32 ms window, extreme care must be taken when transitioning from one pattern to another to satisfy the refresh requirement in *every* rolling refresh window during the transition. If this transition happens directly after the burst refresh phase, all rolling t_{REFW} intervals will meet the minimum required number of REFRESH commands.

As an example of a non-allowable transition, the regular refresh pattern starts after the completion of the pause-phase of the burst/pause refresh pattern. For several rolling t_{REFW} intervals the minimum number of REFRESH commands is not satisfied.

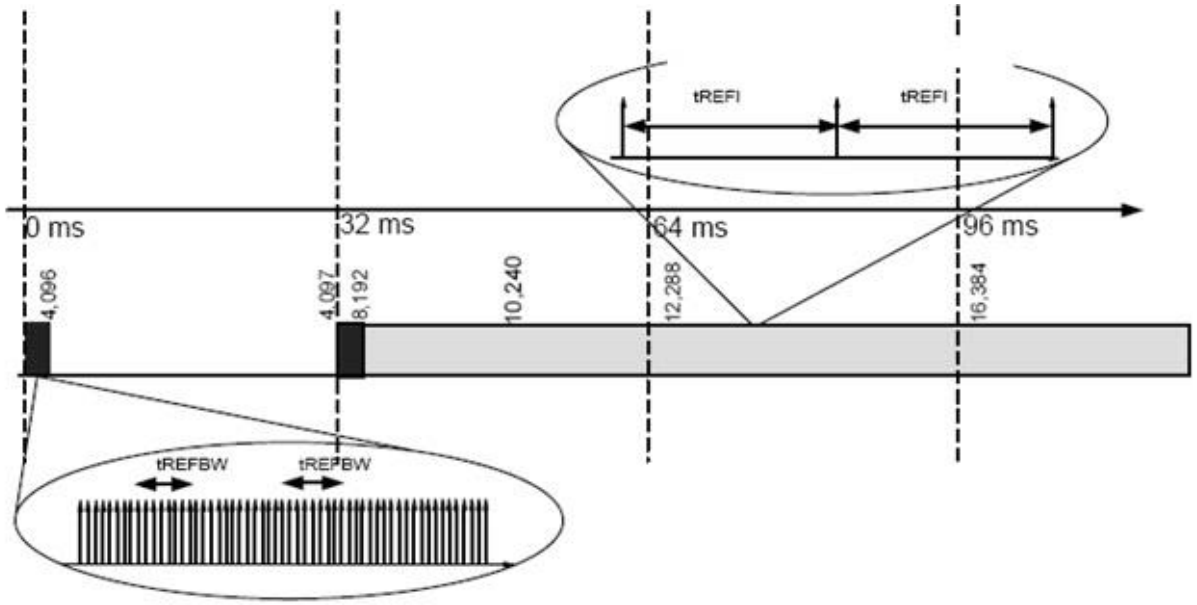
The understanding of the pattern transition is extremely relevant (even if in normal operation only one pattern is employed), as in Self Refresh Mode, a regular distributed refresh pattern must be assumed, which is reflected in the equation for R* above. Therefore it is recommended to enter Self Refresh Mode ONLY directly after the burst-phase of a burst/pause refresh pattern and begin with the burst phase upon exit from Self Refresh.

Figure of Regular, Distributed Refresh Pattern vs. Repetitive Burst Refresh with Subsequent Refresh Pause



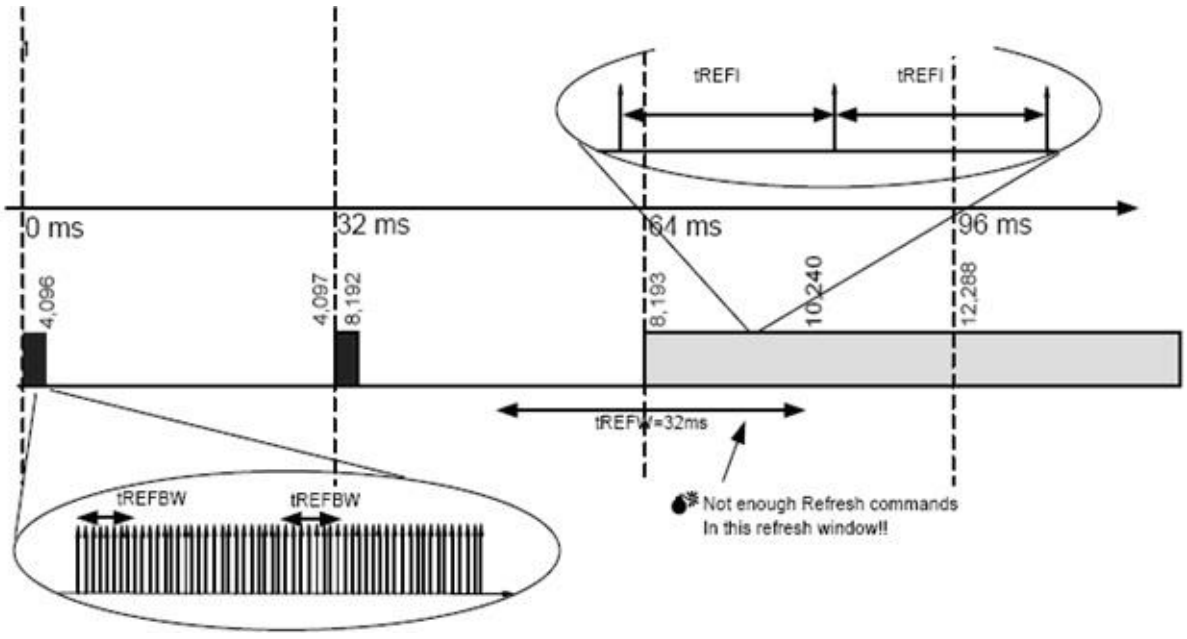
Note: As an example, in a 1Gb device at $T_{CASE} \leqq 85℃$, the distributed refresh pattern has one REFRESH command per 7.8 us; the burst refresh pattern has one REFRESH command per 0.52 us, followed by ~30ms without any REFRESH command.

Figure of Allowable Transition from Repetitive Burst Refresh with Subsequent Refresh Pause to Regular, Distributed Refresh Pattern



Note: As an example, in a 1Gb device at T_{CASE} ≦ 85 ℃, the distributed refresh pattern has one REFRESH command per 7.8 us; the burst refresh pattern has one REFRESH command per 0.52us, followed by ~30ms without any REFRESH command.

Figure of NOT-Allowable Transition from Repetitive Burst Refresh with Subsequent Refresh Pause to Regular, Distributed Refresh Pattern



Note: Only ~2048 REFRESH commands (<R which is 4096) in the indicated t_{REFW} window.

Figure of Recommended Self Refresh entry and exit in conjunction with a Burst/Pause Refresh patterns

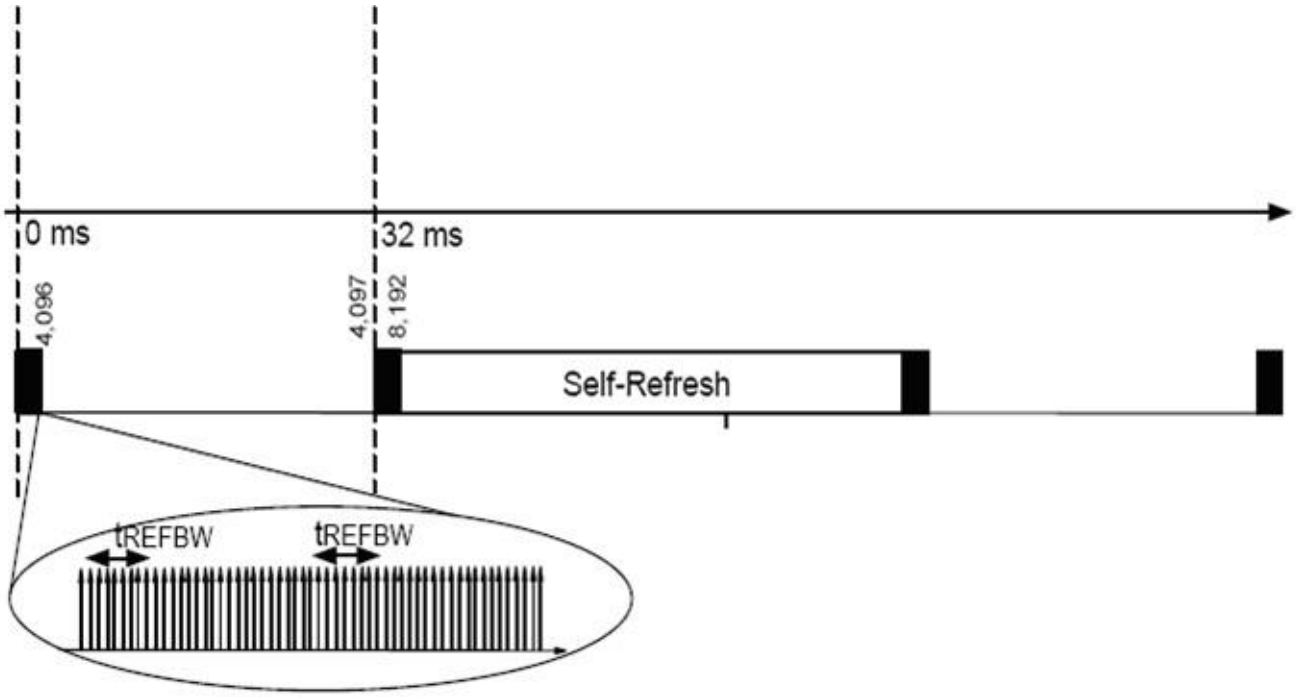


Figure of All Bank Refresh Operation

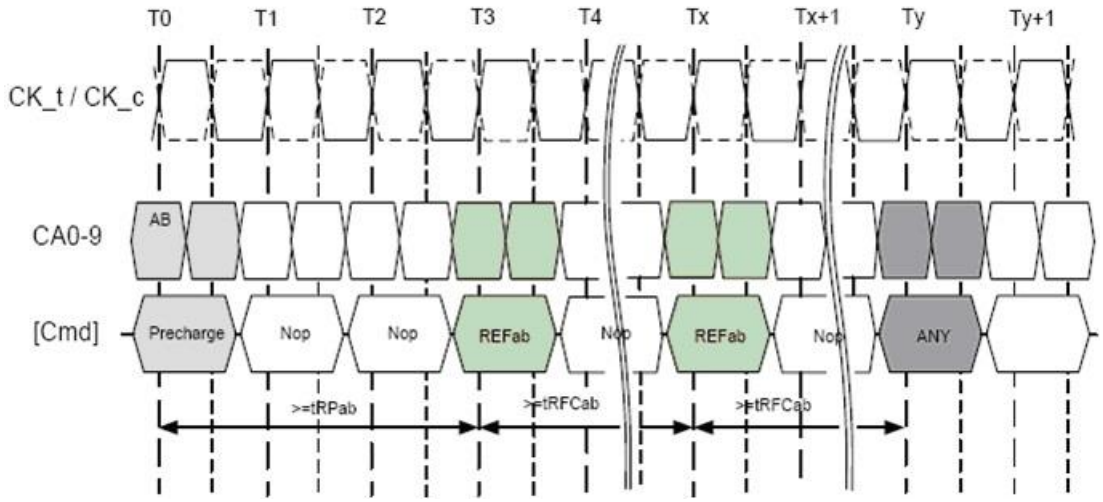
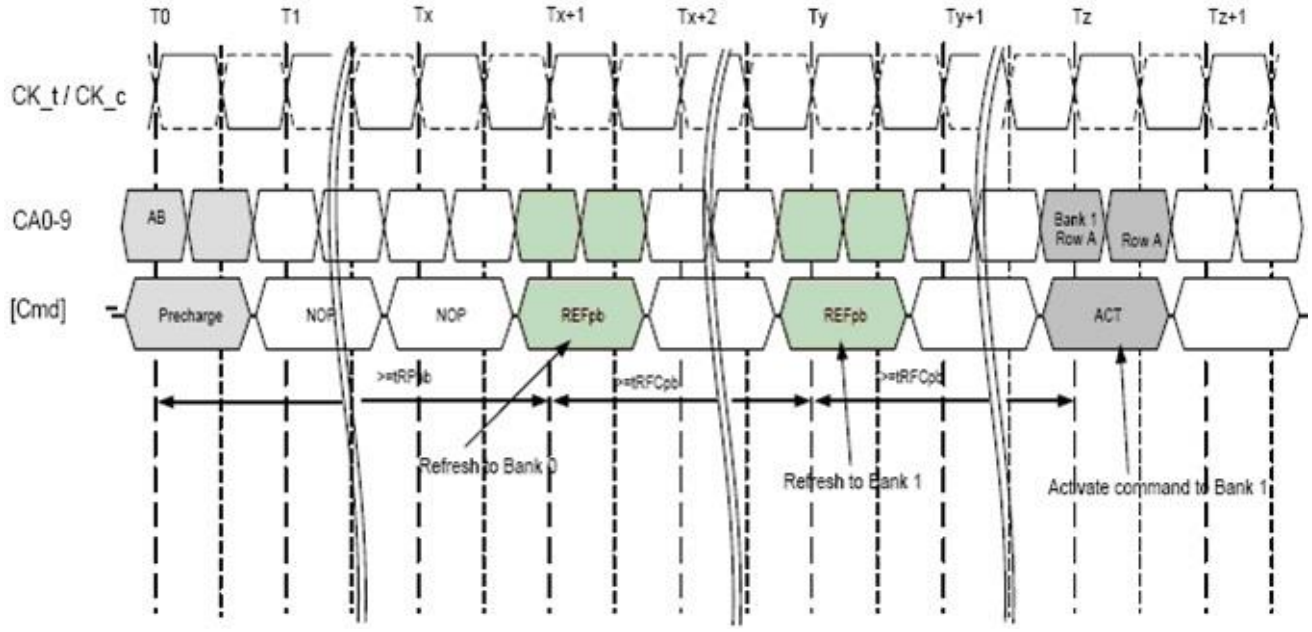


Figure of Per Bank Refresh Operation



Notes:
1. In the beginning of this example, the REFpb bank is pointing to Bank 0.
2. Operations to other banks than the bank being refreshed are allowed during the t_{RFCpb} period.

Self Refresh operation

The Self Refresh command can be used to retain data in the array, even if the rest of the system is powered down. When in the Self Refresh mode, the device retains data without external clocking. The device has a built-in timer to accommodate Self Refresh operation. The Self Refresh command is defined by having CKE LOW, CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. CKE must be HIGH during the previous clock cycle. A NOP command must be driven in the clock cycle following the Self Refresh command. Once the command is registered, CKE must be held LOW to keep the device in Self Refresh mode.

LPDDR2 devices can operate in Self Refresh in both the Standard or Extended Temperature Ranges. The devices will also manage Self Refresh power consumption when the operating temperature changes, lower at low temperatures and higher temperatures. See the Table of "IDD Specification Parameters and Operating Conditions" for details.

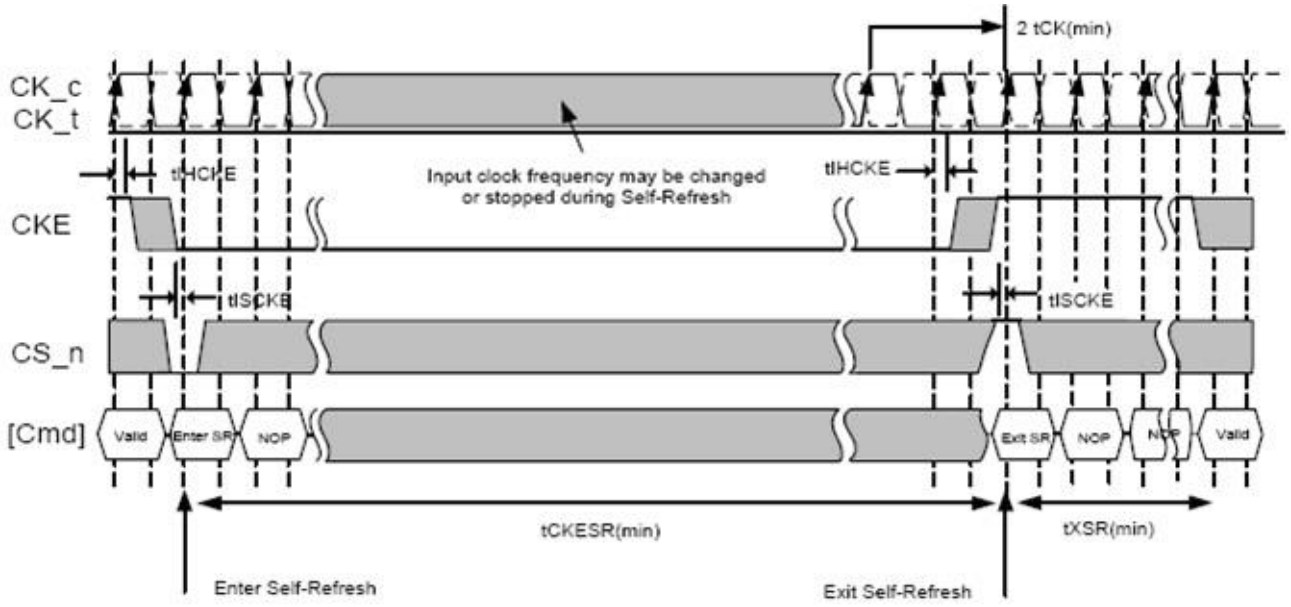
Once the device has entered Self Refresh mode, all of the external signals except CKE, are "don't care". For proper self refresh operation, power supply pins (V_{DD1}, V_{DD2}, V_{DDQ} and V_{DDCA}) must be at valid levels. V_{DDQ} can be turned off during Self Refresh. If V_{DDQ} is turned off, V_{REFDQ} must also be turned off. Prior to exiting Self Refresh, both V_{DDQ} and V_{REFDQ} must be within specified limits (see the Table of "Single-Ended AC and DC Input Levels for DQ and DM").

V_{REFDQ} and V_{REFCA} can be at any level within minimum and maximum levels (see "AC and DC Logic Input Levels for Single-Ended Signals" section). However, prior to exit Self Refresh, V_{REFDQ} and V_{REFCA} must be within specified limits (See 7.1). The device initiates a minimum of one all-bank REFRESH command internally within t_{CKESR} period once it enters Self Refresh mode. The clock is internally disabled during Self Refresh Operation to save power. The minimum time that the device must remain in Self Refresh mode is t_{CKESR}. The user can change the external clock frequency or halt the external clock one clock after Self Refresh entry is registered; however, the clock must be restarted and stable before the device can exit Self Refresh operation.

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock must be stable and within specified limits for a minimum of 2 clock cycles prior to CKE going back HIGH. Once Self Refresh Exit is registered, a delay of at least t_{XSR} must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self Refresh exit period t_{XSR} for proper operation except for self refresh re-entry. NOP commands must be registered on each rising clock edge during t_{XSR}.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is driven HIGH for exit from Self Refresh mode. Upon exit from Self Refresh, it is required that at least one REFRESH command (8 per-bank or 1 all-bank) must be issued before entry into a subsequent Self Refresh command.

Figure of Self Refresh Operation



Notes:

1. Input clock frequency can be changed or stopped during self refresh, provided that upon exiting self refresh, a minimum of two cycles of stable clock are provided, and the clock frequency is between the minimum and maximum frequency for the particular speed grade.
2. The device must be in the “All banks idle” state prior to entering Self Refresh mode.
3. t_{XSR} begins at the rising edge of the clock after CKE is driven HIGH.
4. A valid command can be issued only after t_{XSR} is satisfied. NOPs must be issued during t_{XSR}.

Partial Array Self Refresh: Bank Masking

Each bank can be independently configured whether a self refresh operation is taking place. One mode register unit of 8 bits accessible via MRW command is assigned to program the bank masking status of each bank up to 8 banks. For bank masking bit assignments, see Mode Register 16 (MR16).

The mask bit to the bank controls a refresh operation of entire memory within the bank. If a bank is masked via MRW, a REFRESH operation to the entire bank is blocked and data retention by a bank is not guaranteed in self refresh mode. To enable a REFRESH operation to a bank, a corresponding bank mask bit must be programmed, “unmasked”. When a bank mask bit is unmasked, a refresh to a bank is determined by the programmed status of segment mask bits, which is described in the following chapter.

Partial Array Self Refresh: Segment Masking

Segment masking scheme can be used in place of or in combination with bank masking scheme in the device. The numbers of segment differ from the density and the setting of each segment mask bit is applied across all the banks. For segment masking bit assignments, see Mode Register 17 (MR17).

For those refresh-enabled banks, a refresh operation to the address range which is represented by a segment is blocked when the mask bit to this segment is programmed, “masked”. Programming of segment mask bits is similar to the one of bank mask bits. For 1Gb and larger densities, 8 segments are used as listed in Mode Register 17 (MR17). One mode register unit is used for the programming of segment mask bits up to 8 bits. For densities less than 1Gb, segment masking is not supported.

Table of Bank and Segment Masking Example

	Segment Mask (MR17)	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6	Bank 7
Bank Mask (MR16)		0	1	0	0	0	0	0	1
Segment 0	0	-	M	-	-	-	-	-	M
Segment 1	0	-	M	-	-	-	-	-	M
Segment 2	1	M	M	M	M	M	M	M	M
Segment 3	0	-	M	-	-	-	-	-	M
Segment 4	0	-	M	-	-	-	-	-	M
Segment 5	0	-	M	-	-	-	-	-	M
Segment 6	0	-	M	-	-	-	-	-	M
Segment 7	1	M	M	M	M	M	M	M	M

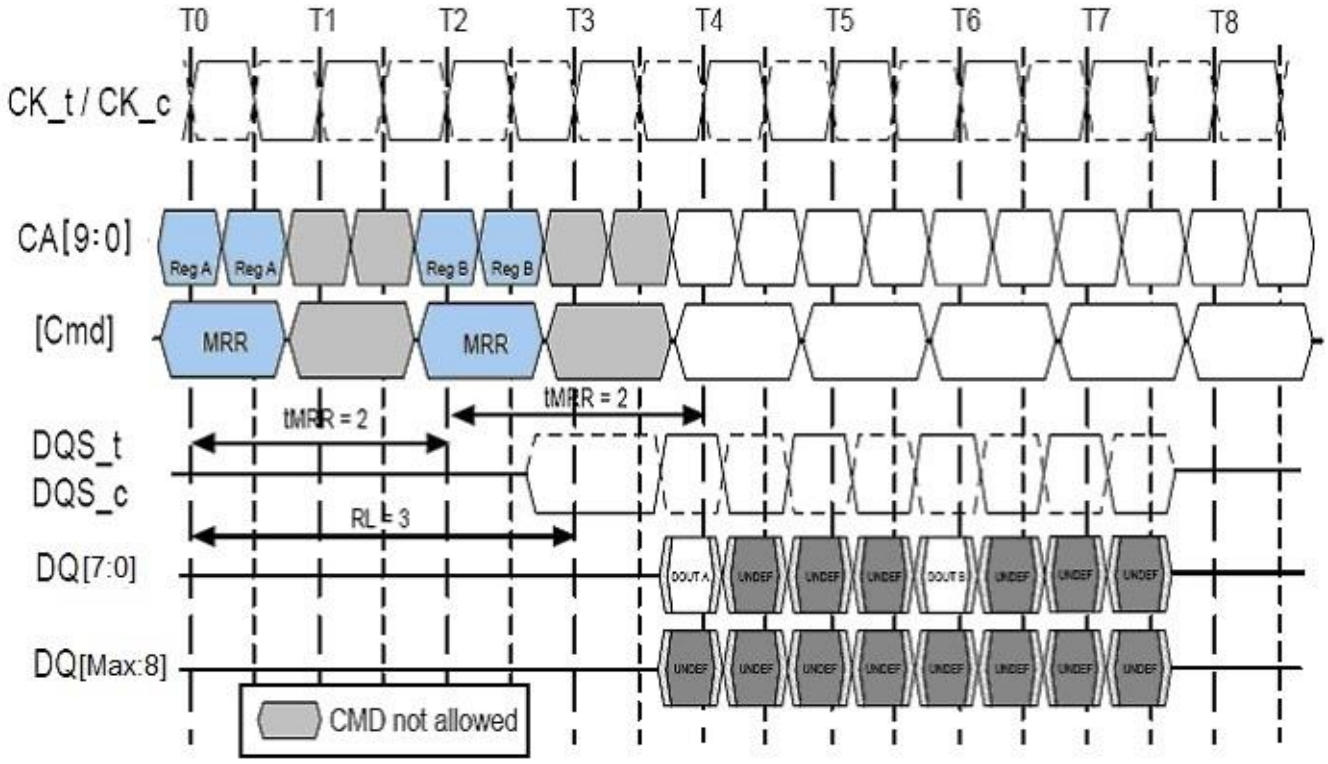
Note: This table illustrates an example of an 8-bank device, when a refresh operation to bank 1 and bank 7, as well as segment 2 and segment 7 are masked.

Mode Register Read Command

The Mode Register Read (MRR) command is used to read configuration and status data from mode registers. The Mode Register Read (MRR) command is initiated by having CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by {CA1f-CA0f, CA9r- CA4r}. The mode register contents are available on the first data beat of DQ[7:0] after RL * t_{CK} + t_{DQSCK} + t_{DQSQ} and following the rising edge of the clock where the Mode Register Read command is issued. Subsequent data beats contain valid, but undefined content, except in the case of the DQ Calibration function, where subsequent data beats contain valid content as described in “DQ Calibration” section. All DQS_t, DQS_c are toggled for the duration of the Mode Register Read burst.

The MRR command has a burst length of four. The Mode Register Read operation (consisting of the MRR command and the corresponding data traffic) must not be interrupted. The MRR command period (t_{MRR}) is 2 clock cycles. Mode Register Reads to reserved and write-only registers shall return valid, but undefined content on all data beats and DQS_t, DQS_c shall be toggled.

Figure of Mode Register Read timing example: RL = 3, t_{MRR} = 2

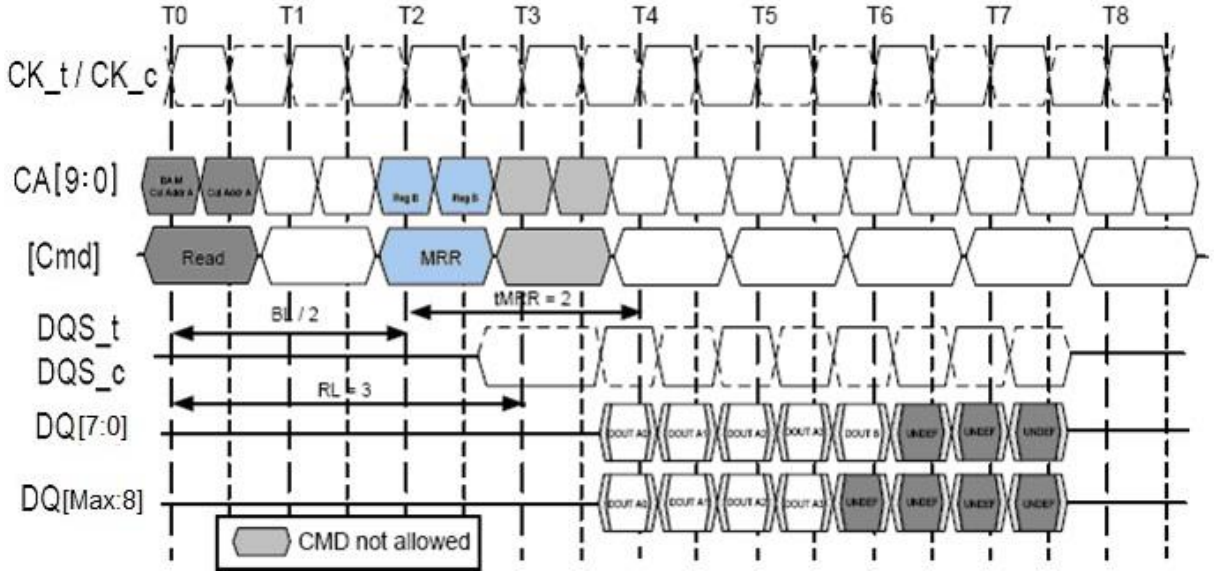


Notes:

1. Mode Register Read has a burst length of four.
2. Mode Register Read operation must not be interrupted.
3. Mode Register data is valid only on DQ[7:0] on the first beat. Subsequent beats contain valid, but undefined data. DQ[Max:8] contain valid, but undefined data for the duration of the MRR burst.
4. The Mode Register Command period is t_{MRR}. No command (other than Nop) is allowed during this period.
5. Mode Register Reads to DQ Calibration registers MR32 and MR40 are described in the section on DQ Calibration.
6. Minimum Mode Register Read to write latency is RL + RU($t_{DQSCK, max}$ / t_{CK}) + 4/2 + 1 - WL clock cycles.
7. Minimum Mode Register Read to Mode Register Write (MRW) latency is RL + RU($t_{DQSCK, max}$ / t_{CK}) + 4/2 + 1 clock cycles.

The MRR command must not be issued earlier than BL/2 clock cycles after a prior Read command and WL + 1 + BL/2 + RU(t_{WTR} /t_{CK}) clock cycles after a prior Write command, because read bursts and write bursts can not be truncated by MRR. Note that if a read or write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated burst should be used as “BL”.

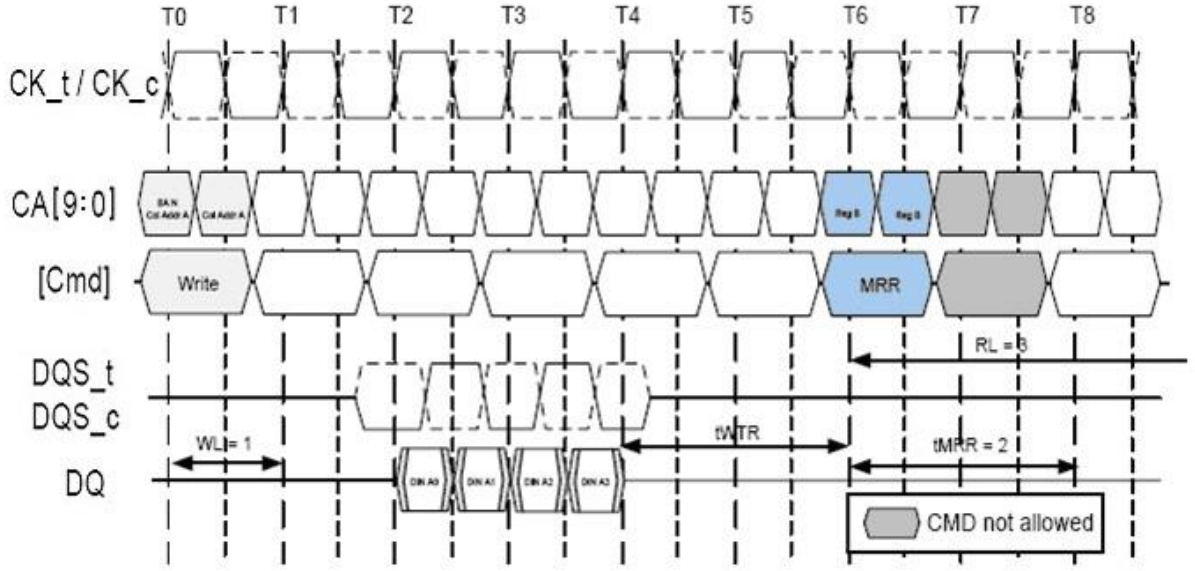
Figure of Read to MRR timing example: RL = 3, t_{MRR} = 2



Notes:

1. The minimum number of clock cycles from the burst read command to the Mode Register Read command is BL/2.
2. The Mode Register Read Command period is t_{MRR}. No command (other than Nop) is allowed during this period

Figure of Burst Write Followed by MRR: RL = 3, WL = 1, BL = 4



Notes:

1. The minimum number of clock cycles from the burst write command to the Mode Register Read command is [WL + 1 + BL/2 + RU(t_{WTR} / t_{CK})].
2. The Mode Register Read command period is t_{MRR}. No command (other than No) is allowed during this period.

Temperature Sensor

LPDDR2 device features a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing derating is required in the Extended Temperature Range and/or monitor the operating temperature. Either the temperature sensor or the device T_{CASE} (See the Table of "Operating Temperature Range") can be used to determine whether operating temperature requirements are being met.

LPDDR2 devices can monitor device temperature and update MR4 according to t_{TSI}. Upon exiting self refresh or power down, the device temperature status bits will be no older than t_{TSI}.

When using the temperature sensor, the actual device temperature may be higher than the T_{CASE} specification (See the Table of "Operating Temperature Range") that applies for the Standard or Extended Temperature Ranges. For example, T_{CASE} may be above 85℃ when MR4[2:0] equals 011b.

To assure proper operation using the temperature sensor, applications must accommodate the parameters in the temperature sensor definitions table.

Table of Temperature Sensor Definitions

Symbol	Parameter	Description	Max/Min	Value	Unit
TempGradient	System Temperature Gradient	Maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2℃	Max	System Dependent	℃/s
ReadInterval	MR4 Read Interval	Time period between MR4 reads from the system	Max	System Dependent	ms
t_{TSI}	Temperature Sensor Interval	Maximum delay between internal updates of MR4	Max	32	ms
SysRespDelay	System Response Delay	Maximum time between a read of MR4 and the response by the system	Max	System Dependent	ms
TempMargin	Device Temperature Margin	Margin between the point at which the device temperature enters the Extended Temperature Range and point at which the controller re-configures the system accordingly	Max	2	℃

To determine the required frequency of polling MR4, the system must use the maximum TempGradient and the maximum response time of the system using the following equation:

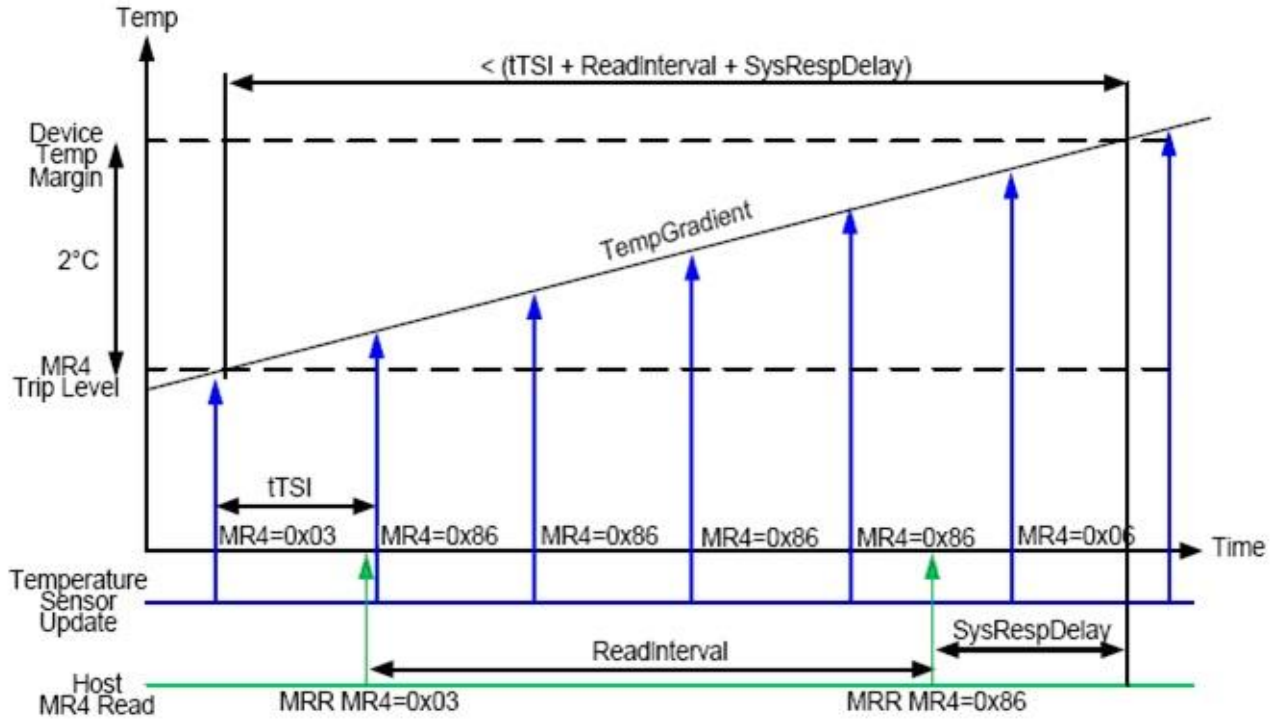
TempGradient x (ReadInterval + t_{TSI} + SysRespDelay) ≤ 2℃

For example, if TempGradient is 10℃/s and the SysRespDelay is 1 ms:

10℃/s * (ReadInterval + 32ms + 1ms) ≤ 2℃

In this case, ReadInterval must be no greater than 167ms.

Figure of Temperature Sensor Timing



DQ Calibration

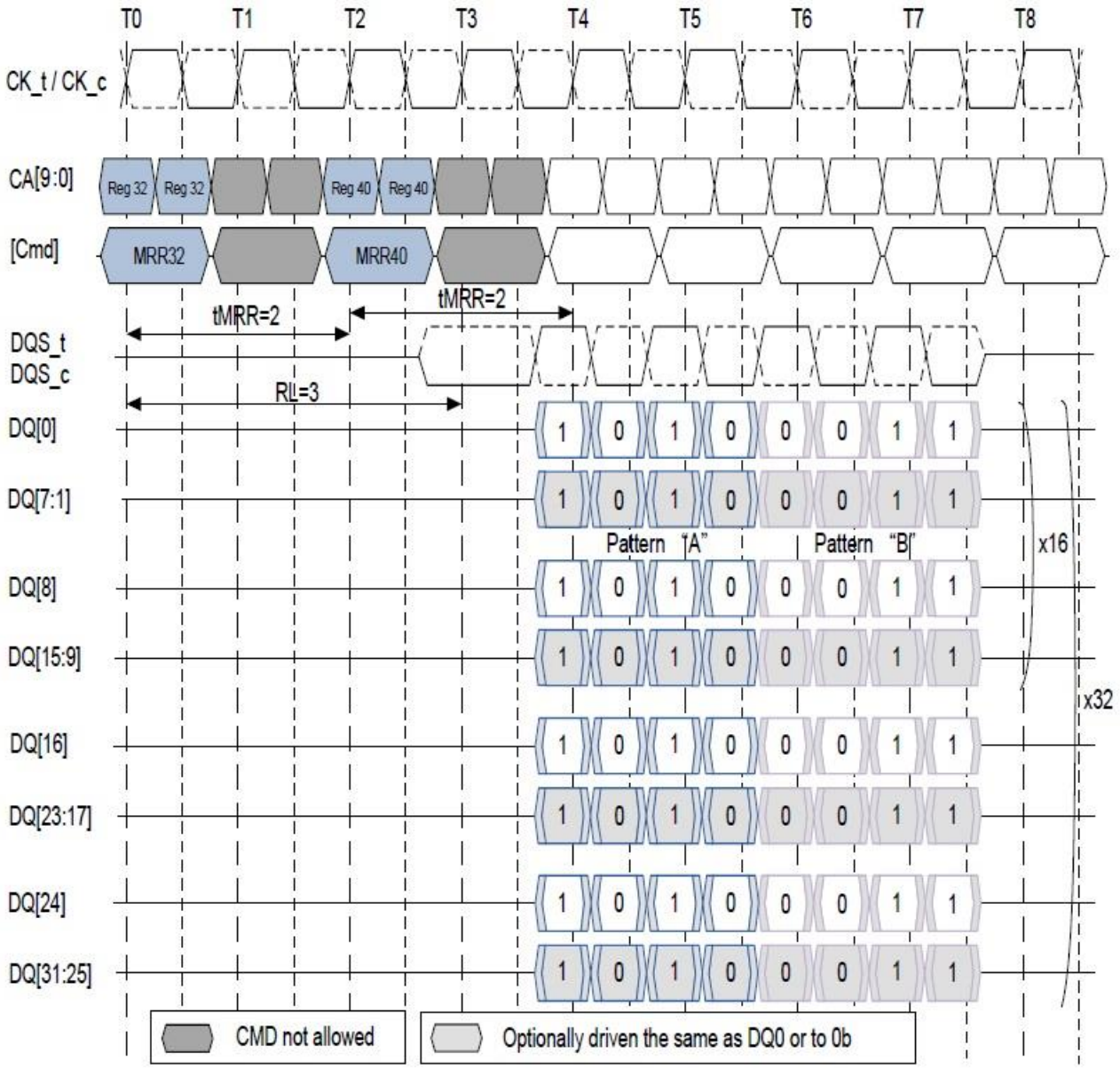
LPDDR2-S4 device features a DQ Calibration function that outputs one of two predefined system timing calibration patterns. A Mode Register Read to MR32 (Pattern “A”) or MR40 (Pattern “B”) will return the specified pattern on DQ0, DQ8, DQ16 and DQ24.

DQ[7:1], DQ[15:9], DQ[23:17] and DQ[31:25] drive the same information as DQ0 during the MRR burst.
MRR DQ Calibration commands can only occur in the Idle state.

Table of Data Calibration Pattern Description

Pattern	MR#	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3	Description
Pattern A	MR32	1	0	1	0	Read to MR32 return DQ calibration pattern A
Pattern B	MR40	0	0	1	1	Read to MR40 return DQ calibration pattern B

Figure of MR32 and MR40 DQ Calibration timing example: RL = 3, t_{MRR} = 2



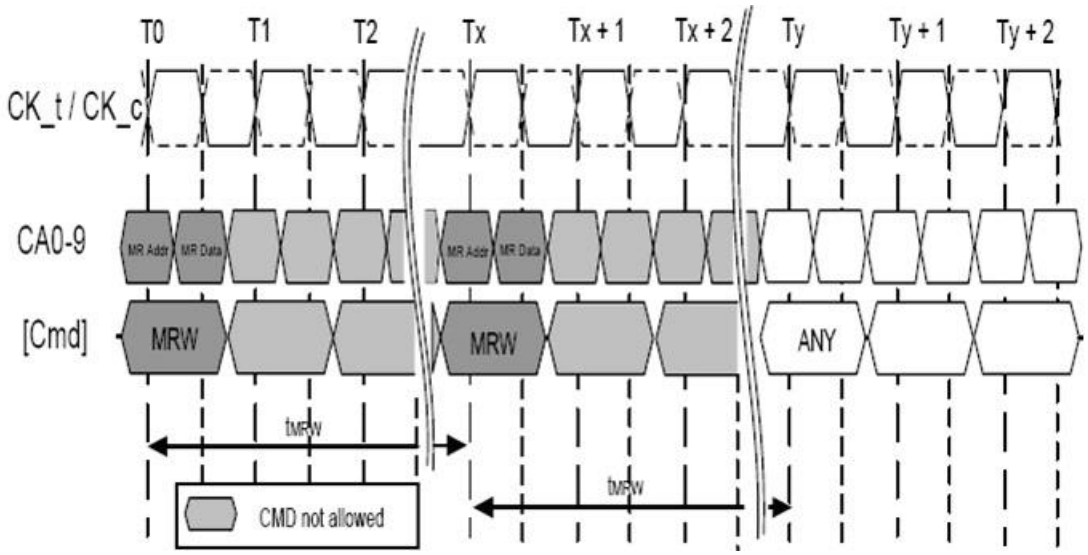
Note:
1. Mode Register Read has a burst length of four.
2. Mode Register Read operation must not be interrupted.
3. The Mode Register Command period is t_{MRR}. No command (other than Nop) is allowed during this period.

Mode Register Write Command

The Mode Register Write command is used to write configuration data to mode registers. The Mode Register Write (MRW) command is initiated by having CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 LOW at the rising edge of the clock. The mode register is selected by {CA1f-CA0f, CA9r-CA4r}. The data to be written to the mode register is contained in CA9f-CA2f. The MRW command period is defined by t_{MRW}. Mode Register Writes to read-only registers have no impact on the functionality of the device.

The MRW can only be issued when all banks are in the idle precharge state. One method of ensuring that the banks are in the idle precharge state is to issue a Precharge-All command.

Figure of Mode Register Write timing example: RL = 3, t_{MRW} = 5



Notes:

1. The Mode Register Write Command period is t_{MRW}. No command (other than Nop) is allowed during this period.
2. At time Ty, the device is in the idle state.

Table of Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW)

Current State	Command	Intermediate State	Next State
All Banks Idle	MRR	Mode Register Reading (All Banks Idle)	All Banks Idle
	MRW	Mode Register Writing (All Banks Idle)	All Banks Idle
	MRW (RESET)	Resetting (Device Auto Initialization)	All Banks Idle
Bank(s) Active	MRR	Mode Register Reading (Bank(s) Active)	Bank(s) Active
	MRW	Not Allowed	Not Allowed
	MRW (RESET)	Not Allowed	Not Allowed

Mode Register Write Reset (MRW RESET)

The MRW RESET command brings the device to the Device Auto Initialization (Resetting) state in the power on Initialization sequence (See "Reset command" of Power Ramp and Device Initialization). The MRW RESET command can be issued from the idle state. This command resets all Mode Registers to their default values. No commands other than NOP can be issued to the device during the MRW RESET period (t_{INIT4}). After MRW Reset, boot timings must be observed until the device initialization sequence is complete and the device is in the idle state. Array data is undefined after the MRW RESET command. For the timing diagram related to MRW Reset, refer to the Figure of "Power Ramp and Initialization Sequence".

Mode Register Write ZQ Calibration Command

The MRW command is also used to initiate the ZQ Calibration command. The ZQ Calibration command is used to calibrate the output drivers (R_{ON}) over process, temperature, and voltage. LPDDR2-S4 devices support ZQ Calibration.

There are four ZQ Calibration commands and related timings times: t_{ZQINIT}, $t_{ZQRESET}$, t_{ZQCL}, and t_{ZQCS}. t_{ZQINIT} corresponds to the initialization calibration; $t_{ZQRESET}$ is for resetting ZQ setting to default impedance; t_{ZQCL} is for long calibration; and t_{ZQCS} is for short calibration.

The Initialization ZQ Calibration (ZQINIT) must be performed for LPDDR2 devices. This Initialization Calibration achieves a R_{ON} accuracy of +/-15%. After initialization, the ZQ Long Calibration can be used to re-calibrate the system to a R_{ON} accuracy of +/-15%. A ZQ Short Calibration can be used periodically to compensate for temperature and voltage drift in the system.

The ZQRESET Command resets the R_{ON} calibration to a default accuracy of +/-30% across process, voltage, and temperature. This command is used to ensure R_{ON} accuracy to +/-30% when ZQCS and ZQCL are not used.

One ZQCS command can effectively correct a minimum of 1.5% (ZQ correction) of R_{ON} impedance error within t_{ZQCS} for all speed bins, assuming the maximum sensitivities specified in "Output Driver Temperature and Voltage Sensitivity" section. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.

One method for calculating the interval between ZQCS commands, given the temperature ($T_{driftrate}$) and voltage ($V_{driftrate}$) drift rates that the LPDDR2 is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{ZQ\ correction}{(T_{sens} \times T_{driftrate}) + (V_{sens} \times V_{driftrate})}$$

Where T_{sens} = max ($dR_{ON}dT$) and V_{sens} = max ($dR_{ON}dV$) define the temperature and voltage sensitivities.

For example, if T_{sens} = 0.75% / ℃, V_{sens} = 0.20% / mV, $T_{driftrate}$ = 1 ℃ / sec and $V_{driftrate}$ = 15 mV / sec, then the interval between ZQCS commands is calculated as:

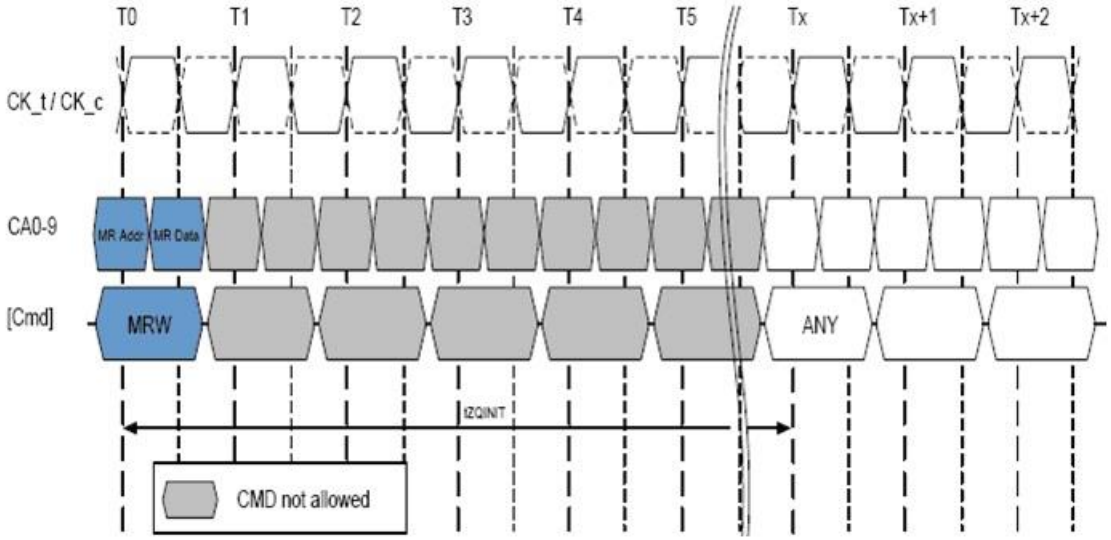
$$\frac{1.5}{(0.75 \times 1) + (0.20 \times 15)} = 0.4\ s$$

A ZQ Calibration command can only be issued when the device is in Idle state with all banks precharged.

No other activities can be performed on the data bus during the calibration period (t_{ZQINIT}, t_{ZQCL}, t_{ZQCS}). The quiet time on the data bus helps to accurately calibrate R_{ON}. There is no required quiet time after the ZQ RESET command. If multiple devices share a single ZQ resistor, only one device can be calibrating at any given time. After calibration is achieved, the device shall disable the ZQ ball's current consumption path to reduce power.

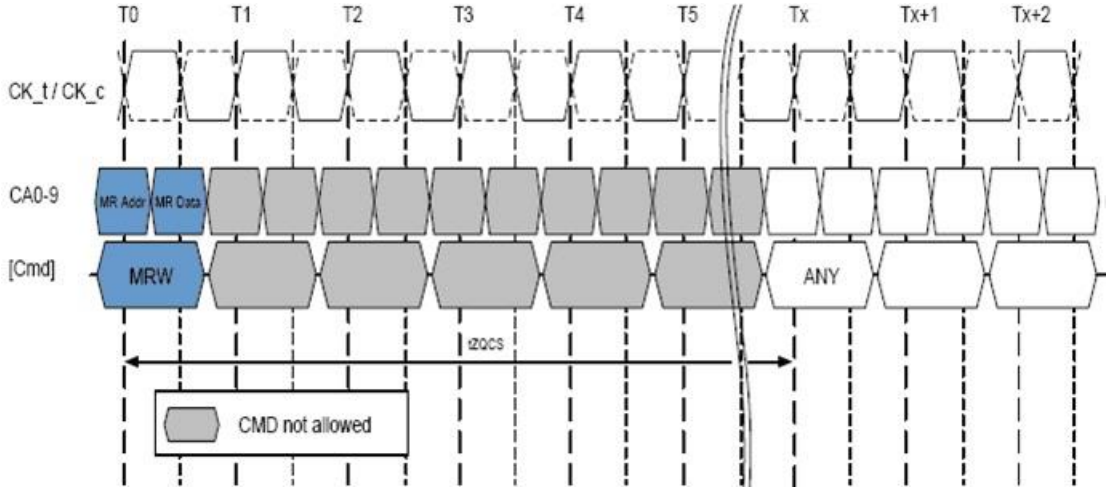
In systems that share the ZQ resistor between devices, the controller must not allow overlap of t_{ZQINIT}, t_{ZQCS}, or t_{ZQCL} between the devices. ZQ RESET overlap is allowed. If the ZQ resistor is absent from the system, ZQ must be connected to V_{DDCA}. In this case, the device must ignore ZQ calibration commands and the device will use the default calibration settings.

Figure of ZQ Calibration Initialization timing example



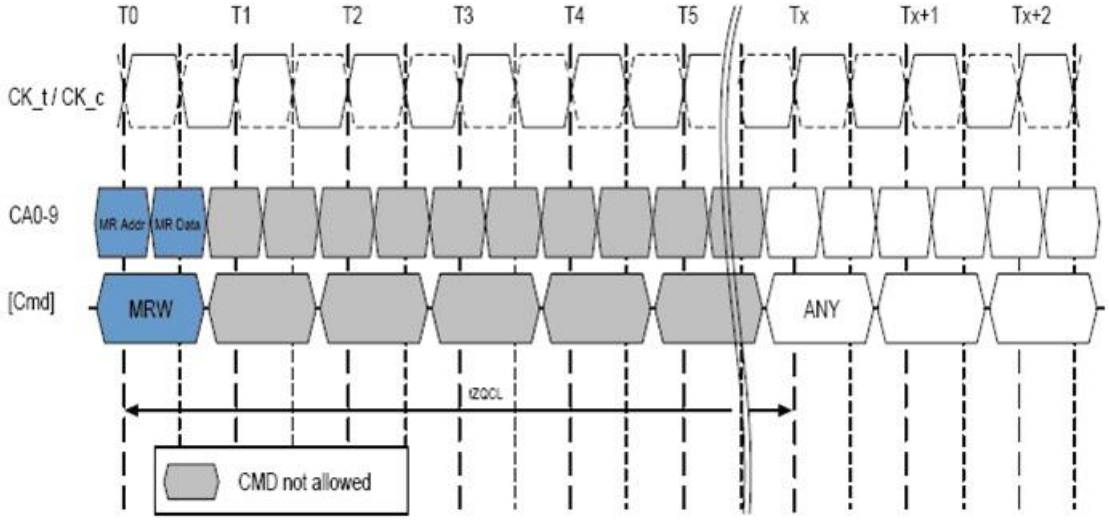
Notes:
1. The ZQ Calibration Initialization period is t_{ZQINIT}. No command (other than Nop) is allowed during this period.
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be high impedance during the calibration process.

Figure of ZQ Calibration Short timing example



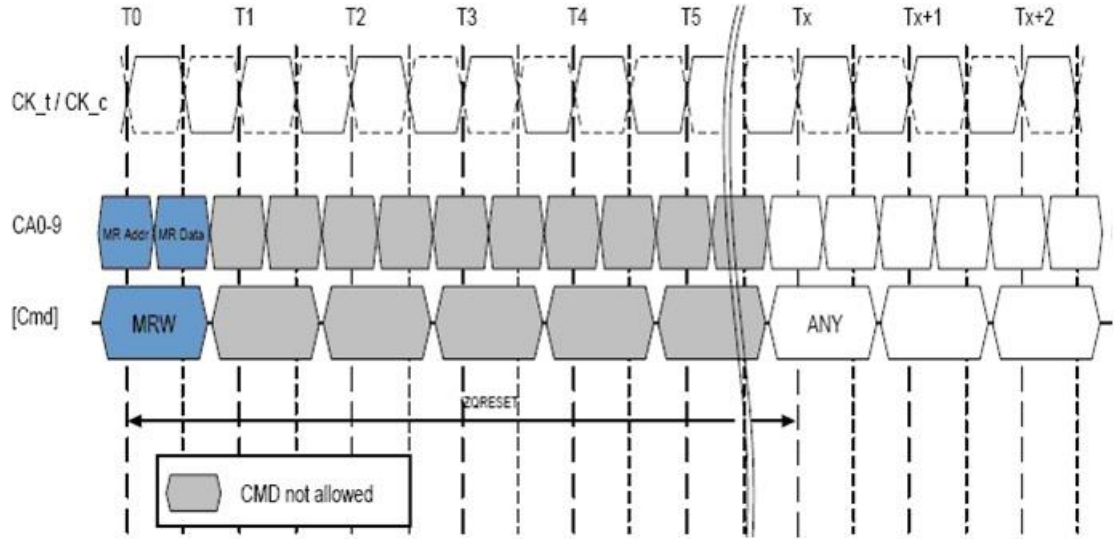
Notes:
1. The ZQ Calibration Short period is t_{ZQCS}. No command (other than Nop) is allowed during this period.
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be high impedance during the calibration process.

Figure of ZQ Calibration Long timing example



Notes:
1. The ZQ Calibration Long period is t_{ZQCL}. No command (other than Nop) is allowed during this period.
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be high impedance during the calibration process.

Figure of ZQ Calibration Reset timing example



Notes:
1. The ZQ Calibration Reset period is $t_{ZQRESET}$. No command (other than Nop) is allowed during this period.
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be high impedance during the calibration process.

ZQ External Resistor Value, Tolerance, and Capacitive Loading

To use the ZQ Calibration function, a 240 Ohm +/- 1% tolerance external resistor must be connected between the ZQ pin and ground. A single resistor can be used for each device or one resistor can be shared between multiple devices if the ZQ calibration timings for each device do not overlap. The total capacitive loading on the ZQ pin must be limited.

Power Down

Power down is synchronously entered when CKE is registered LOW and CS_n HIGH at the rising edge of clock. CKE must be registered HIGH in the previous clock cycle. A NOP command must be driven in the clock cycle following the power down command. CKE is not allowed to go LOW while mode register, read, or write operations are in progress. CKE is allowed to go LOW while any of other operations such as row activation, precharge, autoprecharge, or refresh is in progress, but power down I_{DD} spec will not be applied until finishing those operations.

If power down occurs when all banks are idle, this mode is referred to as idle power down; if power down occurs when there is a row active in any bank, this mode is referred to as active power down.

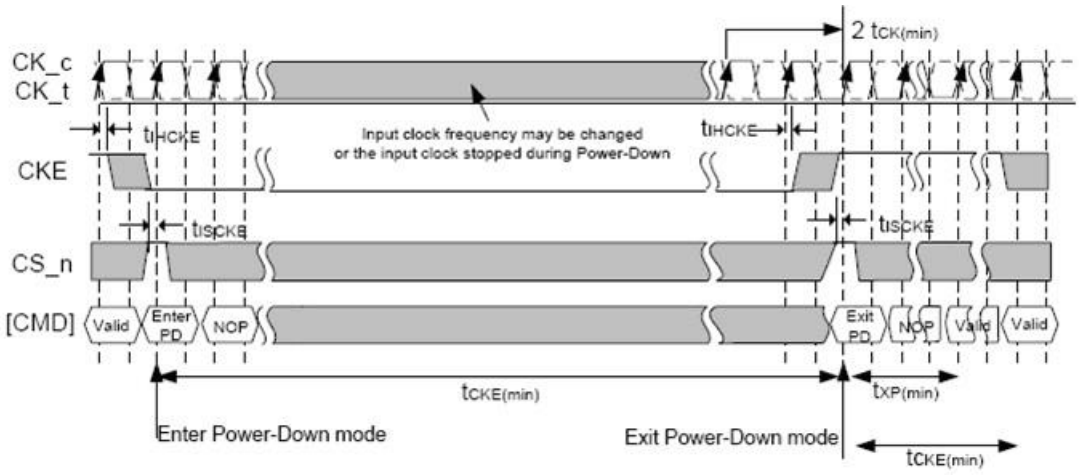
Entering power down deactivates the input and output buffers, excluding CK_t, CK_c, and CKE. In power down mode, CKE must be maintained LOW while all other input signals are "Don't Care". CKE LOW must be maintained until t_{CKE} has been satisfied. V_{REFCA} must be maintained at a valid level during power down.

V_{DDQ} may be turned off during power down. If V_{DDQ} is turned off, then V_{REFDQ} must also be turned off. Prior to exiting power down, both V_{DDQ} and V_{REFDQ} must be within their respective minimum/maximum operating ranges (see "AC and DC Operating Conditions" section).

The maximum duration in power down mode is only limited by the refresh requirements, as no refresh operations are performed in power down mode.

The power down state is exited when CKE is registered HIGH. The controller must drive CS_n HIGH in conjunction with CKE HIGH when exiting the power down state. CKE HIGH must be maintained until t_{CKE} has been satisfied. A valid, executable command can be applied with power down exit latency, t_{XP} after CKE goes HIGH. Power down exit latency is defined in the "AC Timing" section.

Figure of Basic Power Down Entry and Exit timing



Note: Input clock frequency can be changed or the input clock stopped during power down, provided that upon exiting power down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to power down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

Figure of CKE Intensive Environment

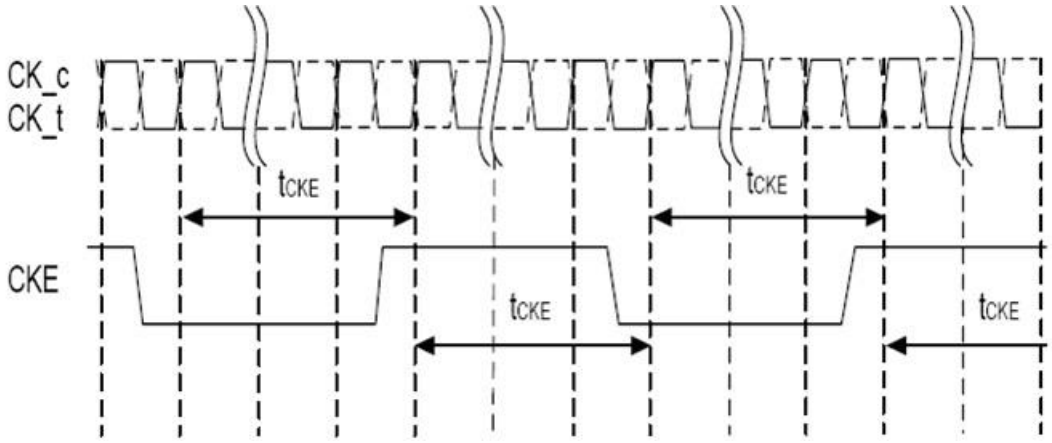
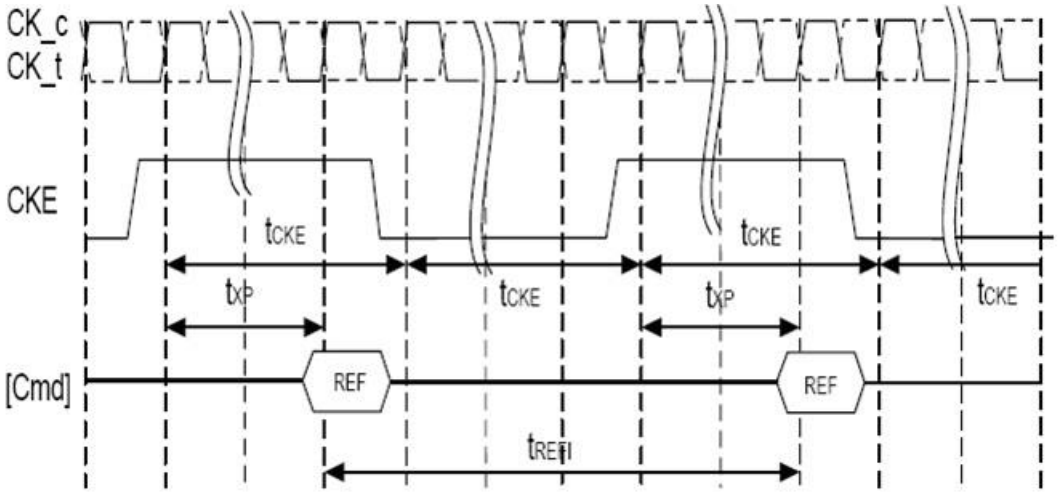
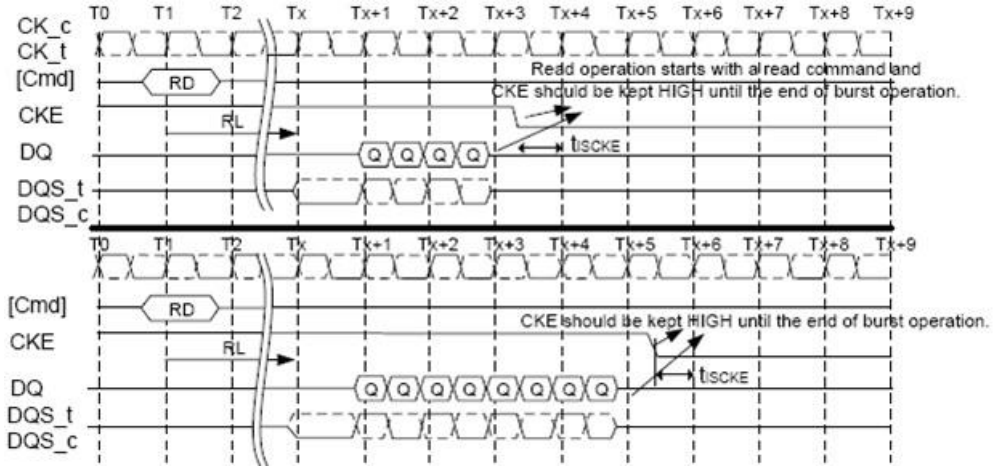


Figure of Refresh to Refresh timing with CKE Intensive Environment



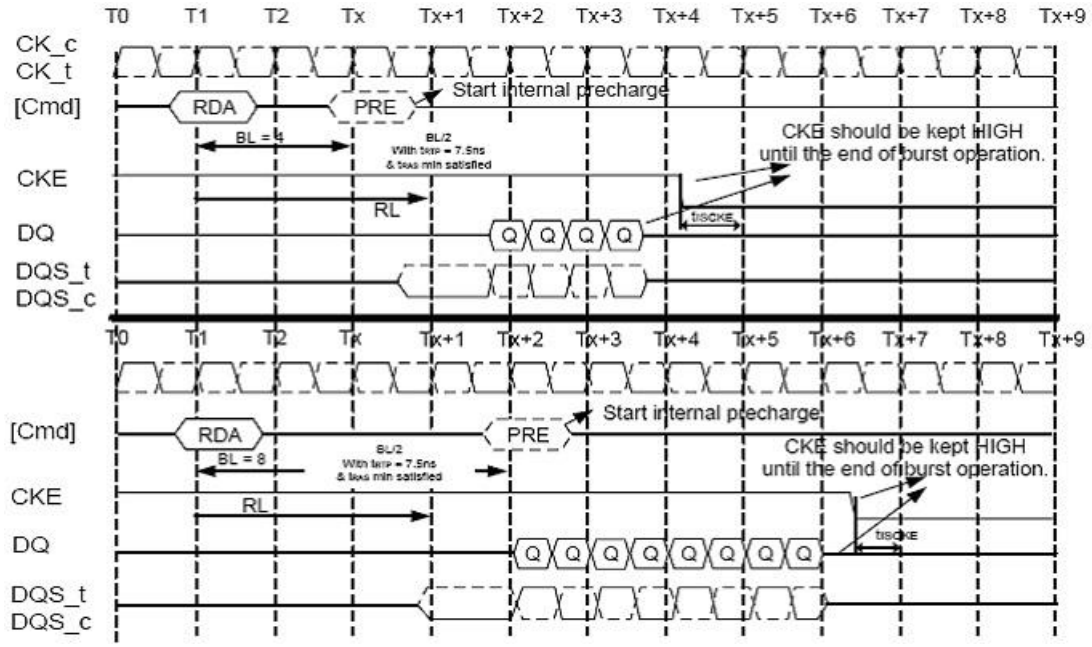
Note: The pattern shown above can repeat over a long period of time. With this pattern, all AC and DC timing & voltage specifications with temperature and voltage drift are ensured.

Figure of Read to Power Down Entry



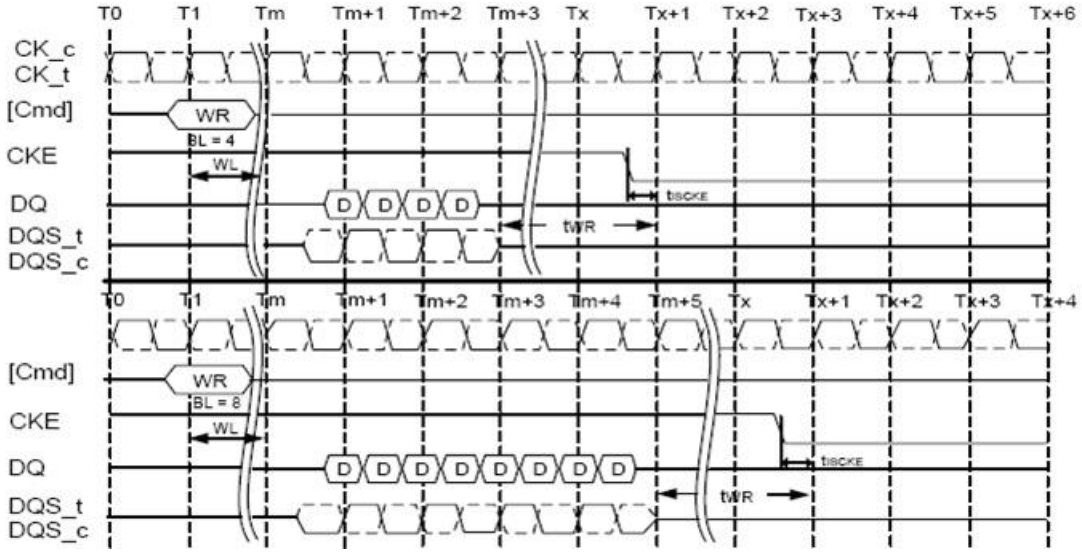
Note: CKE can be registered LOW at (RL + RU($t_{DQSCK\,(MAX)}$ / t_{CK}) + BL/2 + 1) clock cycles after the clock on which the Read command is registered.

Figure of Read with Auto Precharge to Power Down Entry



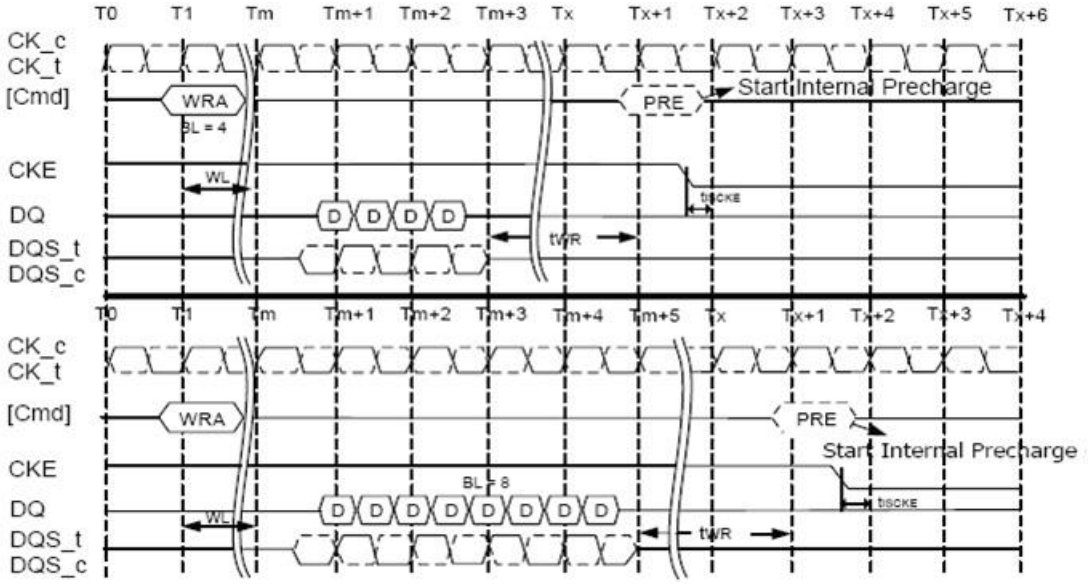
Note: CKE can be registered LOW at (RL + RU($t_{DQSCK\,(MAX)}$ / t_{CK}) + BL/2 + 1) clock cycles after the clock on which the Read command is registered.

Figure of Write to Power Down Entry



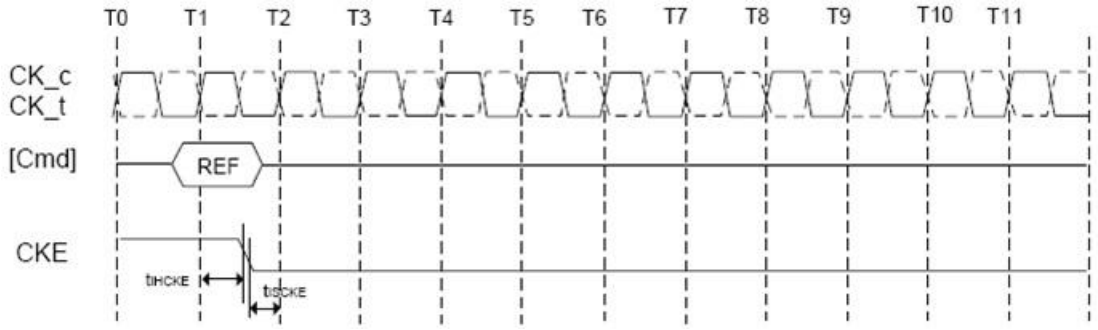
Note: CKE can be registered LOW at (WL + 1 + BL/2 + RU(t_{WR}/ t_{CK})) clock cycles after the clock on which the Write command is registered.

Figure of Write with Auto Precharge to Power Down Entry



Note: CKE can be registered LOW at (WL + 1 + BL/2 + RU(t_{WR} / t_{CK}) + 1) clock cycles after the Write command is registered.

Figure of Refresh command to Power Down Entry



Note: CKE can go LOW at t_{IHCKE} after the clock on which the Refresh command is registered.

Figure of Activate command to Power Down Entry



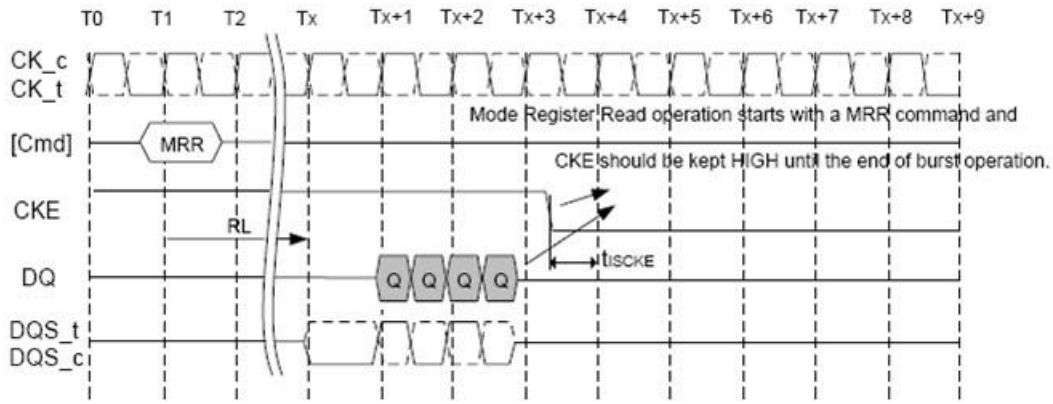
Note: CKE can go LOW at t_{IHCKE} after the clock on which the Activate command is registered.

Figure of Precharge/Precharge All command to Power Down Entry



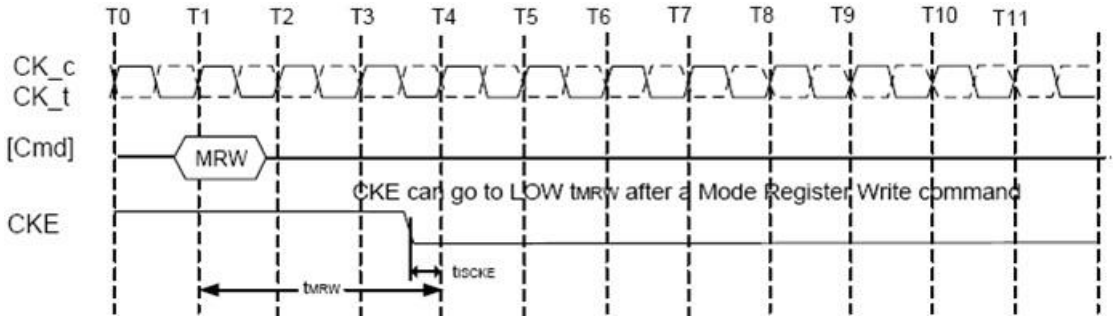
Note: CKE may go LOW at t_{IHCKE} after the clock on which the Precharge/Precharge All command is registered.

Figure of Mode Register Read to Power Down Entry



Note: CKE can be registered LOW at (RL + RU($t_{DQSCK\ (MAX)}$ / t_{CK})+ BL/2 + 1) clock cycles after the clock on which the Mode Register Read command is registered.

Figure of Mode Register Write to Power Down Entry



Note: CKE can be registered LOW at t_{MRW} after the clock on which the Mode Register Write command is registered

Deep Power Down

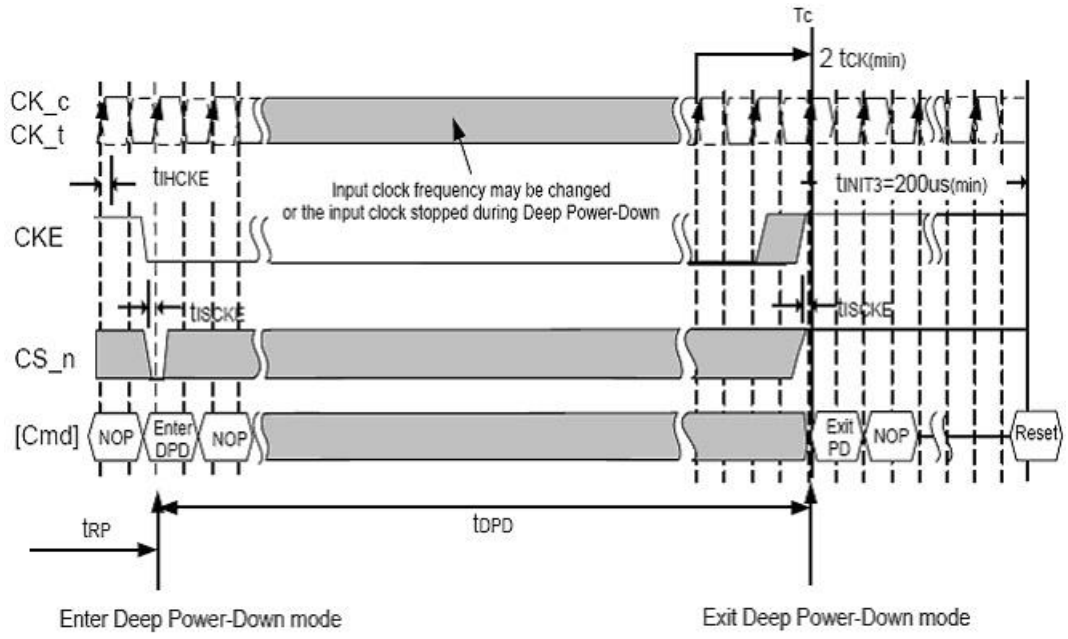
Deep Power Down (DPD) is entered when CKE is registered LOW with CS_n LOW, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of clock. A NOP command must be driven in the clock cycle following the power down command. CKE is not allowed to go LOW while MRR or MRW operations are in progress. All banks must be in idle state with no activity on the data bus prior to entering the Deep Power Down mode. During Deep Power Down, CKE must be held LOW.

In Deep Power Down mode, all input buffers except CKE, all output buffers, and the power supply to internal circuitry are disabled within the device. All power supplies must be within specified limits prior to exiting Deep Power Down. V_{REFDQ} and V_{REFCA} can be at any level within minimum and maximum levels. However prior to exiting Deep Power Down, V_{REF} must be within specified limits (See "AC & DC Operating Conditions" section).

The contents of the device may be lost upon entry into Deep Power Down mode.

The Deep Power Down state is exited when CKE is registered HIGH, while meeting t_{ISCKE} with a stable clock input. The device must be fully re-initialized by controller as described in the Power Up and Initialization sequence. The device is ready for normal operation after the initialization sequence.

Figure of Deep Power Down Entry and Exit timing



Notes:

1. Initialization sequence can start at any time after T_C.
2. t_{INIT3} and T_C refer to timings in the initialization sequence. For more detail, see “Power Up, Initialization, and Power Down”.
3. Input clock frequency can be changed or the input clock stopped during deep power down, provided that upon exiting deep power down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to deep power down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

Input clock stop and frequency change

LPDDR2 devices support input clock frequency change during CKE LOW under the following conditions:

- $t_{CK(abs),\ min}$ is met for each clock cycle;
- Refresh Requirements apply during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- Any Activate, Preactive or Precharge commands have executed to completion prior to changing the frequency;
- The related timing conditions (t_{RCD}, t_{RP}) have been met prior to changing the frequency;
- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of 2 clock cycles prior to CKE going HIGH.

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR2 devices support clock stop during CKE LOW under the following conditions:

- CK_t is held LOW and CK_c is held HIGH during clock stop;
- Refresh Requirements apply during clock stop;
- During clock stop, only REFab or REFpb commands may be executing;
- Any Activate, Preactive or Precharge commands have executed to completion prior to stopping the clock;
- The related timing conditions (t_{RCD}, t_{RP}) have been met prior to stopping the clock;
- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of 2 clock cycles prior to CKE going HIGH.

LPDDR2 devices support input clock frequency change during CKE HIGH under the following conditions:

- $t_{CK\ (abs),\ min}$ is met for each clock cycle;
- Refresh Requirements apply during clock frequency change;
- Any Activate, Read, Write, Preactive, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to changing the frequency;
- The related timing conditions (t_{RCD}, t_{WR}, t_{WRA}, t_{RP}, t_{MRW}, t_{MRR}, etc.) have been met prior to changing the frequency;
- CS_n shall be held HIGH during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- The LPDDR2 device is ready for normal operation after the clock satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of $2t_{CK} + t_{XP}$.

After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR2 devices support clock stop during CKE HIGH under the following conditions:

- CK_t is held LOW and CK_c is held HIGH during clock stop;
- CS_n shall be held HIGH during clock clock stop;
- Refresh Requirements apply during clock stop;
- During clock stop, only REFab or REFpb commands may be executing;
- Any Activate, Read, Write, Preactive, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to stopping the clock;
- The related timing conditions (t_{RCD}, t_{WR}, t_{WRA}, t_{RP}, t_{MRW}, t_{MRR}, etc.) have been met prior to stopping the clock;
- The LPDDR2 device is ready for normal operation after the clock is restarted and satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of $2t_{CK} + t_{XP}$.

No Operation command

The purpose of the No Operation command (NOP) is to prevent the device from registering any unwanted command between operations. Only when the CKE level is constant for clock cycle N-1 and clock cycle N, a NOP command can be issued at clock cycle N. A NOP command has two possible encodings:

1. CS_n HIGH at the clock rising edge N.
2. CS_n LOW and CA0, CA1, CA2 HIGH at the clock rising edge N.

The No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

Truth tables

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

Table of Command Truth Table [1~12]

Command	Command Pins			CA Pins										CK_t Edge
	CKE		CS_n	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
	CK_t (n-1)	CK_t (n)												
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	↑
	H	H	X	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	↓
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	↑
	H	H	X	MA6	MA7	X								↓
Refresh (per bank)[11]	H	H	L	L	L	H	L	X						↑
	H	H	X	X										↓
Refresh (all bank)	H	H	L	L	L	H	H	X						↑
	H	H	X	X										↓
Enter Self Refresh	H	L	L	L	L	H	X							↑
	X	L	X	X										↓
Activate (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	↑
	H	H	X	R0	R1	R2	R3	R4	R5	R6	R7	R13	R14	↓
Write (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
	H	H	X	AP[3,4]	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
Read (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
	H	H	X	AP[3,4]	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
Precharge (per bank, all bank)	H	H	L	H	H	L	H	AB	X	X	BA0	BA1	BA2	↑
	H	H	X	X										↓
BST	H	H	L	H	H	L	L	X						↑
	H	H	X	X										↓
Enter Deep Power Down	H	L	L	H	H	L	X							↑
	X	L	X	X										↓
NOP	H	H	L	H	H	H	X							↑
	H	H	X	X										↓
Maintain PD, SREF, DPD (NOP)	L	L	L	H	H	H	X							↑
	L	L	X	X										↓
NOP	H	H	H	X										↑
	H	H	X	X										↓
Maintain PD, SREF, DPD (NOP)	L	L	H	X										↑
	L	L	X	X										↓
Enter Power Down	H	L	H	X										↑
	X	L	X	X										↓
Exit PD, SREF, DPD	L	H	H	X										↑
	X	H	X	X										↓

Notes:

1. All commands are defined by the current states of CS_n, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.
2. Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon.
3. AP “HIGH” during a READ or WRITE command indicates that an auto precharge will occur to the bank associated with the READ or WRITE command.
4. “X” means “H or L (but a defined logic level)”.
5. Self refresh exit and Deep Power Down exit are asynchronous.
6. V_{REF} must be between 0 and V_{DDQ} during Self Refresh and Deep Power Down operation.
7. CAxr refers to command/address bit “x” on the rising edge of clock.
8. CAxf refers to command/address bit “x” on the falling edge of clock.
9. CS_n and CKE are sampled at the rising edge of clock.
10. Per Bank Refresh is only allowed in devices with 8 banks.
11. The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.
12. AB “HIGH” during Precharge command indicates that all bank Precharge will occur. In this case, Bank Address is do-not-care.

Table of CKE Truth Table [1~5,11]

Current State	CKE n-1	CKE n	CS_n	Command n	Operation n	Next State	Notes
Active Power Down	L	L	X	X	Maintain Active Power Down	Active Power Down	
	L	H	H	NOP	Exit Active Power Down	Active	6,9
Idle Power Down	L	L	X	X	Maintain Idle Power Down	Idle Power Down	
	L	H	H	NOP	Exit Idle Power Down	Idle	6,9
Resetting Idle Power Down	L	L	X	X	Maintain Resetting Power Down	Resetting Power Down	
	L	H	H	NOP	Exit Resetting Power Down	Idle or Resetting	6,9,12
Deep Power Down	L	L	X	X	Maintain Deep Power Down	Deep Power Down	
	L	H	H	NOP	Exit Deep Power Down	Power On	8
Self Refresh	L	L	X	X	Maintain Self Refresh	Self Refresh	
	L	H	H	NOP	Exit Self Refresh	Idle	7,10
Bank(s) Active	H	L	H	NOP	Enter Active Power Down	Active Power Down	
All Banks Idle	H	L	H	NOP	Enter Idle Power Down	Idle Power Down	
	H	L	L	Enter Self Refresh	Enter Self Refresh	Self Refresh	
	H	L	L	Deep Power Down	Enter Deep Power Down	Deep Power Down	
Resetting	H	L	H	NOP	Enter Resetting Power Down	Resetting Power Down	
Other states	H	H	Refer to the Command Truth Table				

Notes:

1. "CKE n" is the logic state of CKE at clock rising edge n; "CKE n-1" was the state of CKE at the previous clock edge.
2. "CS_n" is the logic state of CS_n at the clock rising edge n;
3. "Current state" is the state of the device immediately prior to clock rising edge n.
4. "Command n" is the command registered at clock edge N, and "Operation n" is a result of "Command n".
5. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
6. Power Down exit time (t_{XP}) should elapse before a command other than NOP is issued.
7. Self Refresh exit time (t_{XSR}) should elapse before a command other than NOP is issued.
8. The Deep Power Down exit procedure must be followed as discussed in the Deep Power Down section.
9. The clock must toggle at least twice during the t_{XP} period.
10. The clock must toggle at least twice during the t_{XSR} time.
11. 'X' means "Don't care".
12. Upon exiting Resetting Power Down, the device will return to the idle state if t_{INIT5} has expired.

Table of Current State Bank n - Command to Bank n [1~5]

Current State	Command	Operation	Next State	Notes
Any	NOP	Continue previous operation	Current State	
Idle	ACTIVATE	Select and activate row	Active	
	Refresh (Per Bank)	Begin to refresh	Refreshing (Per Bank)	6
	Refresh (All Bank)	Begin to refresh	Refreshing (All Bank)	7
	MRW	Load value to Mode Register	MR Writing	7
	MRR	Read value from Mode Register	Idle, MR Reading	
	Reset	Begin Device Auto-Initialization	Resetting	7,8
	Precharge	Deactivate row in bank or banks	Precharging	9,15
Row Active	Read	Select column, and start read burst	Reading	
	Write	Select column, and start write burst	Writing	
	MRR	Read value from Mode Register	Active MR Reading	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading	Read	Select column, and start new read burst	Reading	10,11
	Write	Select column, and start write burst	Writing	10,11,12
	BST	Read burst terminate	Active	13
Writing	Write	Select column, and start new write burst	Writing	10,11
	Read	Select column, and start read burst	Reading	10,11,14
	BST	Write burst terminate	Active	13
Power On	Reset	Begin Device Auto-Initialization	Resetting	7,9
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Notes:

1. The table applies when both CKEn-1 and CKEn are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Power Down.
2. All states and sequences not shown are illegal or reserved.
3. Current State Definitions:
   Idle: The bank or banks have been precharged, and t_{RP} has been met.
   Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts / accesses and no register accesses are in progress.
   Reading: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Writing: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. NOP commands or allowable commands to the other bank must be issued on any clock edge occurring during these states. Allowable commands to the other banks are determined by its current state, and according to Table of Current State Bank n - Command to Bank m.
   Precharging: starts with the registration of a Precharge command and ends when t_{RP} is met. Once t_{RP} is met, the bank will be in the idle state.
   Row Activating: starts with registration of an Activate command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank will be in the 'Active' state.
   Read with AP Enabled: starts with the registration of the Read command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} has been met, the bank will be in the idle state.
   Write with AP Enabled: starts with registration of a Write command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.
5. The following states must not be interrupted by any executable command; NOP commands must be applied to each positive clock edge during these states.
   Refreshing (Per Bank): starts with registration of a Refresh (Per Bank) command and ends when t_{RFCpb} is met. Once t_{RFCpb} is met, the bank will be in the idle state.
   Refreshing (All Bank): starts with registration of a Refresh (All Bank) command and ends when t_{RFCab} is met. Once t_{RFCab} is met, the device will be in the all banks idle state.
   Idle MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the idle state.
   Resetting MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the resetting state.
   Active MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the active state.

MR Writing: starts with the registration of a MRW command and ends when t_{MRW} has been met. Once t_{MRW} has been met, the bank will be in the idle state.

Precharging All: starts with the registration of a Precharge All command and ends when t_{RP} is met. Once t_{RP} is met, the bank will be in the idle state.

6. Bank-specific; requires that the bank is idle and no bursts are in progress.
7. Not bank-specific; requires that all banks are idle and no bursts are in progress.
8. Not bank-specific; reset command is achieved through Mode Register Write command.
9. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
10. A command other than NOP should not be issued to the same bank while a Read or Write burst with Auto Precharge is enabled.
11. The new Read or Write command could be Auto Precharge enabled or Auto Precharge disabled.
12. A Write command can be applied after the completion of the Read burst; otherwise, a BST must be used to end the Read prior to asserting a Write command.
13. Not bank-specific. Burst Terminate (BST) command affects the most recent read/write burst started by the most recent Read/Write command, regardless of bank.
14. A Read command may be applied after the completion of the Write burst; otherwise, a BST must be used to end the Write prior to asserting a Read command.
15. If a Precharge command is issued to a bank in the idle state, t_{RP} shall still apply.

Table of Current State Bank n - Command to Bank m [1~6]

Current State of Bank n	Command for Bank m	Operation	Next State for Bank m	Notes
Any	NOP	Continue previous operation	Current State of Bank m	
Idle	Any	Any command allowed to Bank m	-	18
Row Activating, Active, or Precharging	Activate	Select and activate row in Bank m	Active	7
	Read	Select column, and start read burst from Bank m	Reading	8
	Write	Select column, and start write burst to Bank m	Writing	8
	Precharge	Deactivate row in bank or banks	Precharging	9
	MRR	Read value from Mode Register	Idle MR Reading or Active MR Reading	10,11,13
	BST	Read or Write burst terminate an ongoing Read/Write from/to Bank m	Active	18
Reading (Auto precharge disabled)	Read	Select column, and start read burst from Bank m	Reading	8
	Write	Select column, and start write burst to Bank m	Writing	8,14
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Writing (Auto precharge disabled)	Read	Select column, and start read burst from Bank m	Reading	8,16
	Write	Select column, and start write burst to Bank m	Writing	8
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading with Auto precharge	Read	Select column, and start read burst from Bank m	Reading	8,15
	Write	Select column, and start write burst to Bank m	Writing	8,14,15
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Writing with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	8,15,16
	Write	Select column, and start write burst to Bank m	Writing	8,15
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Power On	Reset	Begin Device Auto-Initialization	Resetting	12,17
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Notes:

1. The table applies when both CKEn-1 and CKEn are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Self Refresh or Power Down.
2. All states and sequences not shown are illegal or reserved.
3. Current State Definitions:
   Idle: the bank has been precharged, and t_{RP} has been met.
   Active: a row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
   Reading: a Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Writing: a Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
4. Refresh, Self Refresh, and Mode Register Write commands can only be issued when all bank are idle.
5. A Burst Terminate (BST) command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. The following states must not be interrupted by any executable command; NOP commands must be applied during each clock cycle while in these states:
   Idle MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the idle state.

Resetting MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the resetting state.
Active MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the active state.
MR Writing: starts with the registration of a MRW command and ends when t_{MRW} has been met. Once t_{MRW} has been met, the bank will be in the idle state.

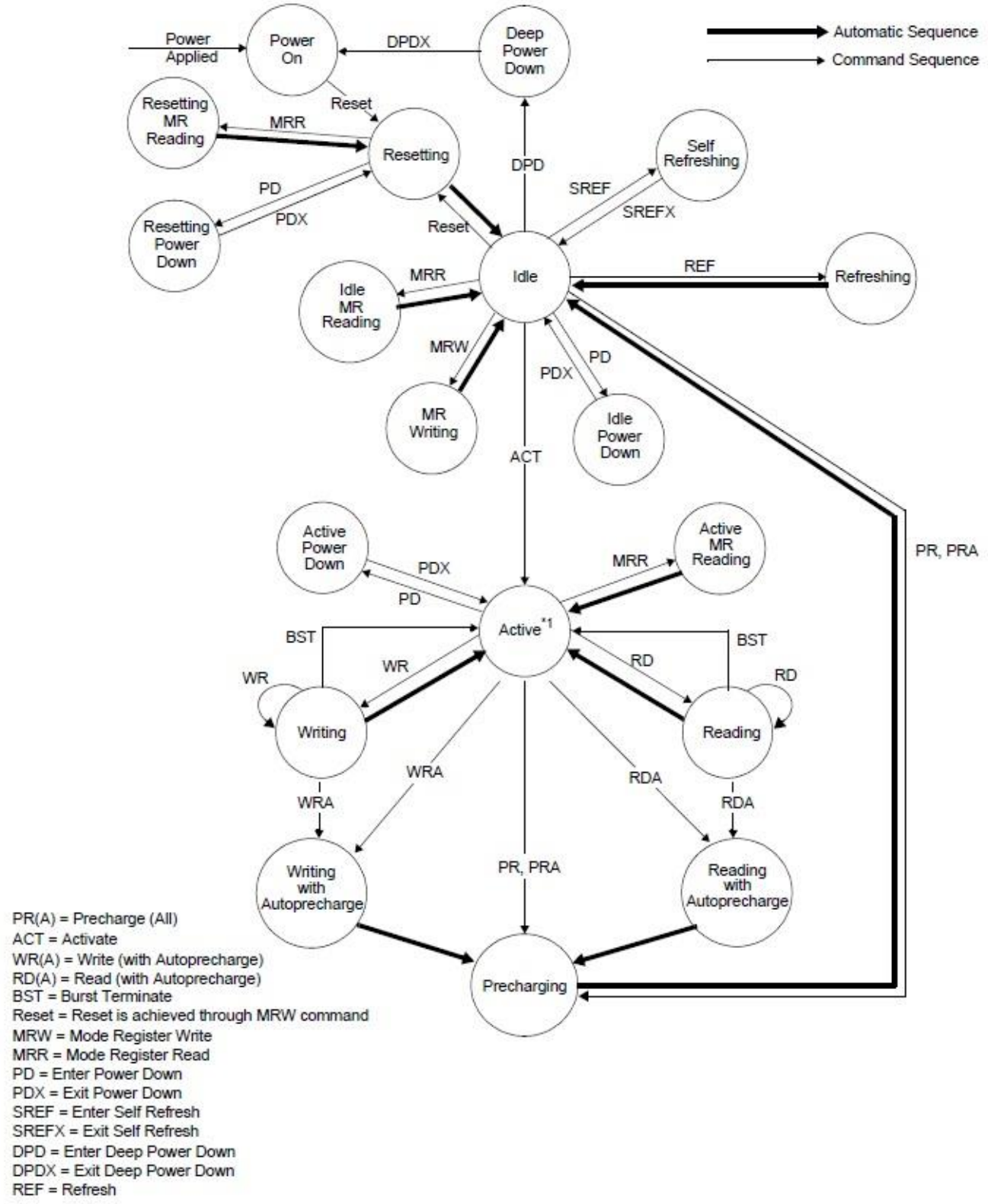
7. t_{RRD} must be met between Activate command to Bank n and a subsequent Activate command to Bank m.
8. Reads or Writes listed in the Command column include Reads and Writes with Auto Precharge enabled and Reads and Writes with Auto Precharge disabled.
9. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
10. MRR is allowed during the Row Activating state (Row Activating starts with registration of an Activate command and ends when t_{RCD} is met.)
11. MRR is allowed during the Precharging state. (Precharging starts with registration of a Precharge command and ends when t_{RP} is met.
12. Not bank-specific; requires that all banks are idle and no bursts are in progress.
13. The next state for Bank m depends on the current state of Bank m (Idle, Row Activating, Precharging, or Active). The reader shall note that the state may be in transition when a MRR is issued. Therefore, if Bank m is in the Row Activating state and Precharging, the next state may be Active and Precharge dependent upon t_{RCD} and t_{RP} respectively.
14. A Write command may be applied after the completion of the Read burst; otherwise a BST must be issued to end the Read prior to asserting a Write command.
15. Read with auto precharge enabled or a Write with auto precharge enabled may be followed by any valid command to other banks provided that the timing restrictions of auto precharge are followed.
16. A Read command may be applied after the completion of the Write burst; otherwise, a BST must be issued to end the Write prior to asserting a Read command.
17. Reset command is achieved through Mode Register Write command.
18. BST is allowed only if a Read or Write burst is ongoing.

Table of Data Mask Truth Table

Name (Functional)	DM	DQs	Note
Write enable	L	Valid	1
Write inhibit	H	X	1

Note: Used to mask write data, provided coincident with the corresponding data.

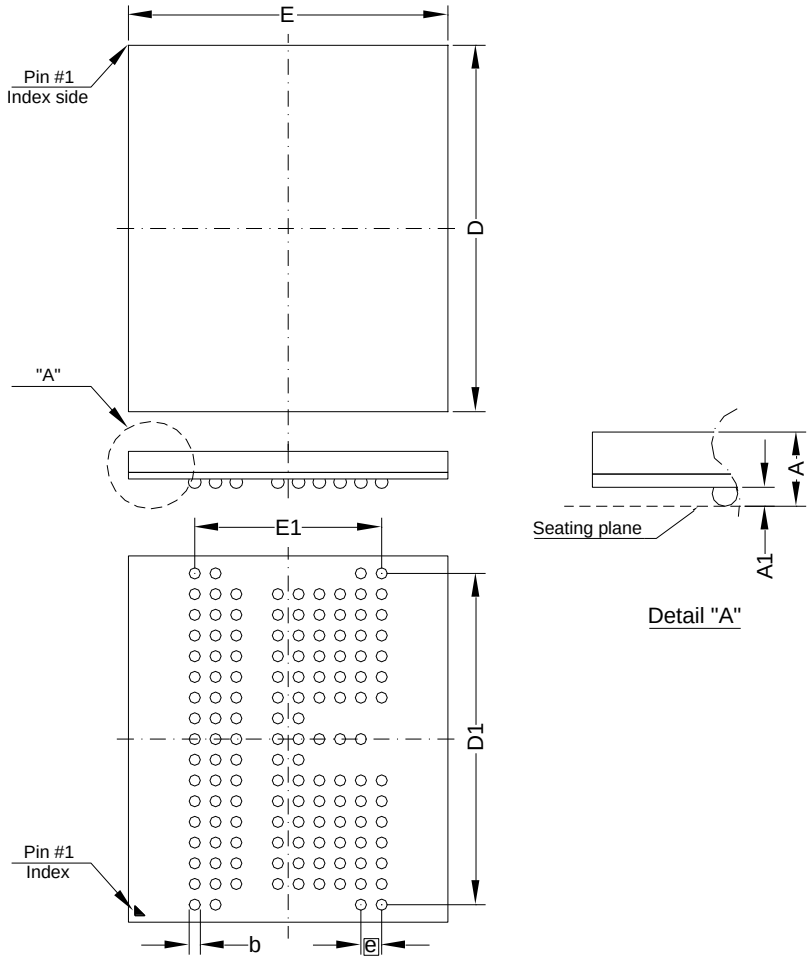
Simplified Bus Interface State Diagram



Note: All banks are precharged in the idle state.

PACKING DIMENSIONS

134-BALL (10x11.5 mm)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	-	-	1.00	-	-	0.039
A_1	0.25	0.32	0.37	0.010	0.013	0.015
b	0.35	0.41	0.46	0.014	0.016	0.018
D	11.40	11.50	11.60	0.449	0.453	0.457
E	9.90	10.00	10.10	0.390	0.394	0.398
D_1	10.40 BSC			0.409 BSC		
E_1	5.85 BSC			0.230 BSC		
e	0.65 BSC			0.026 BSC		

Controlling dimension : Millimeter.
(Revision date : Jul 11. 2025)

Revision History

Revision	Date	Description
1.0	2025.07.23	Original
1.1	2025.09.05	Modify: Product ID
1.2	2026.10.27	Modify: IDD4RQ

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