VLSI SINCE 1983
2026 VLSI International Symposium on Technology, Systems and Applications
April 13-17, 2026, Hsinchu, Taiwan

aiPIM - Processing in Memory DRAM

ESMT (Elite Semiconductor Microelectronics Technology Inc.)

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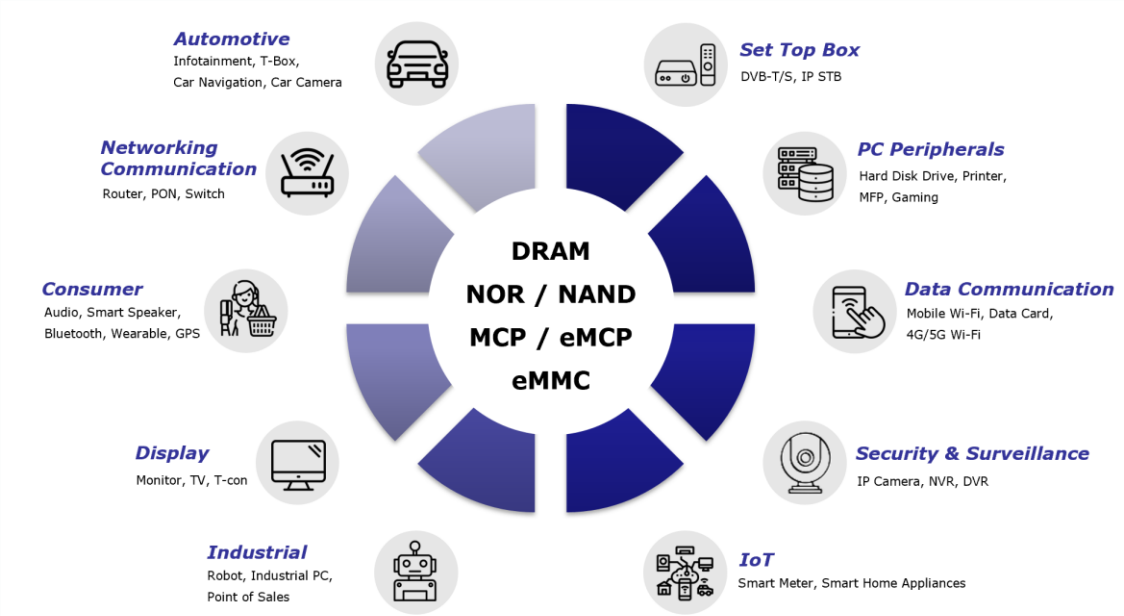
Who we are?

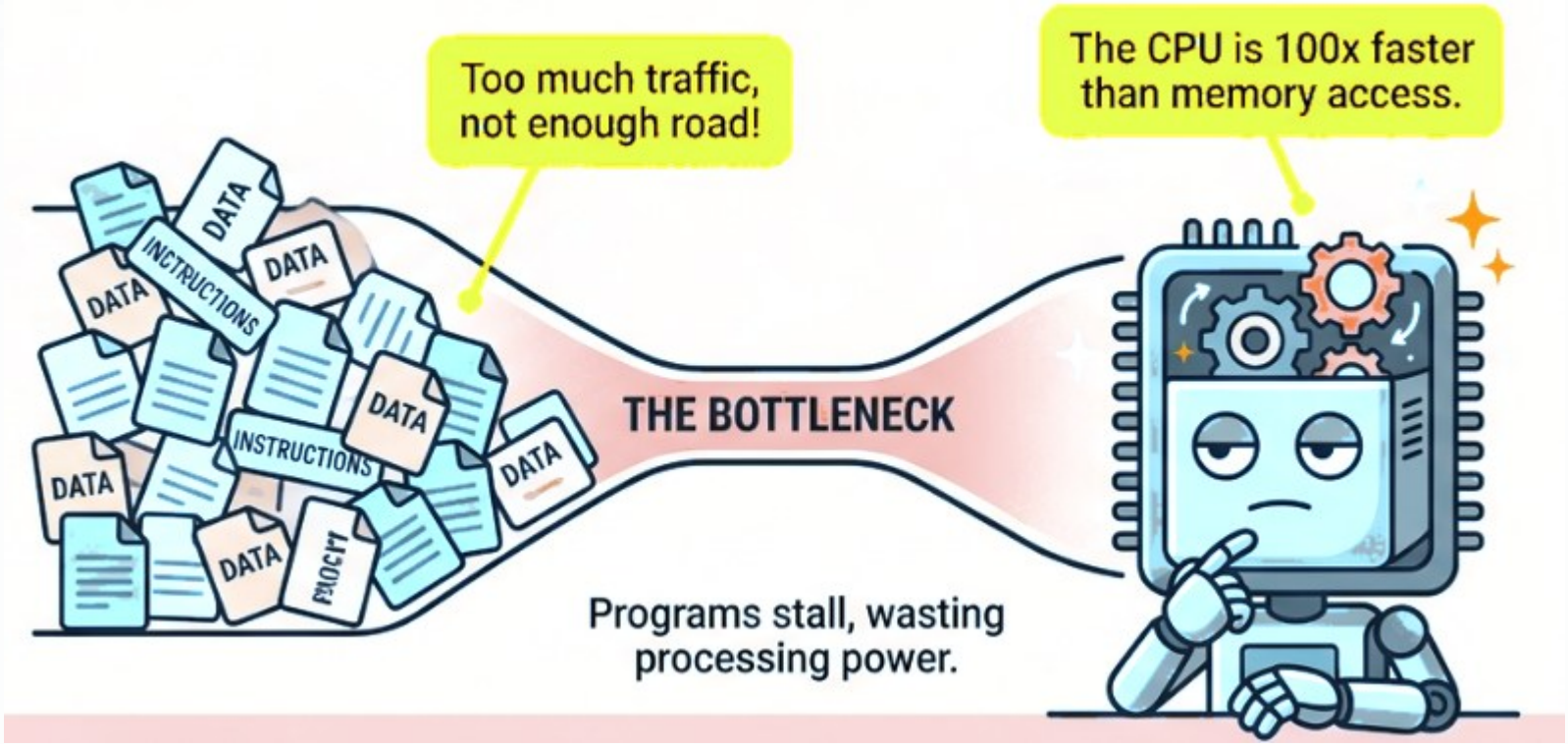
- ESMT is a fabless specialty memory supplier for niche market in various applications



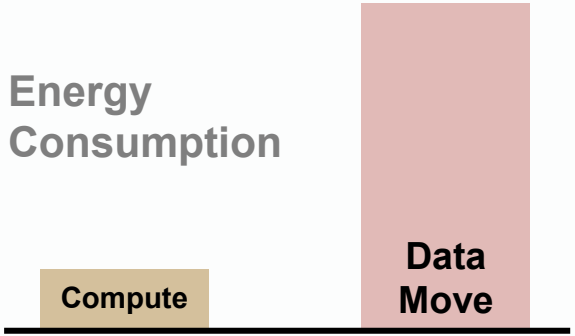
Outline

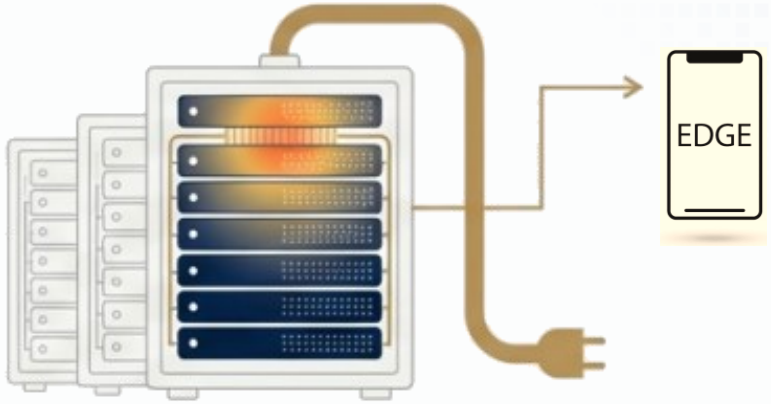
- The von Neumann Bottleneck
- Moving Data with Memory
- ESMT aiPIM Design Concept
- Product Prototypes
- Conclusion and Future Outlook

The von Neumann Bottleneck



Critical Energy Consumption



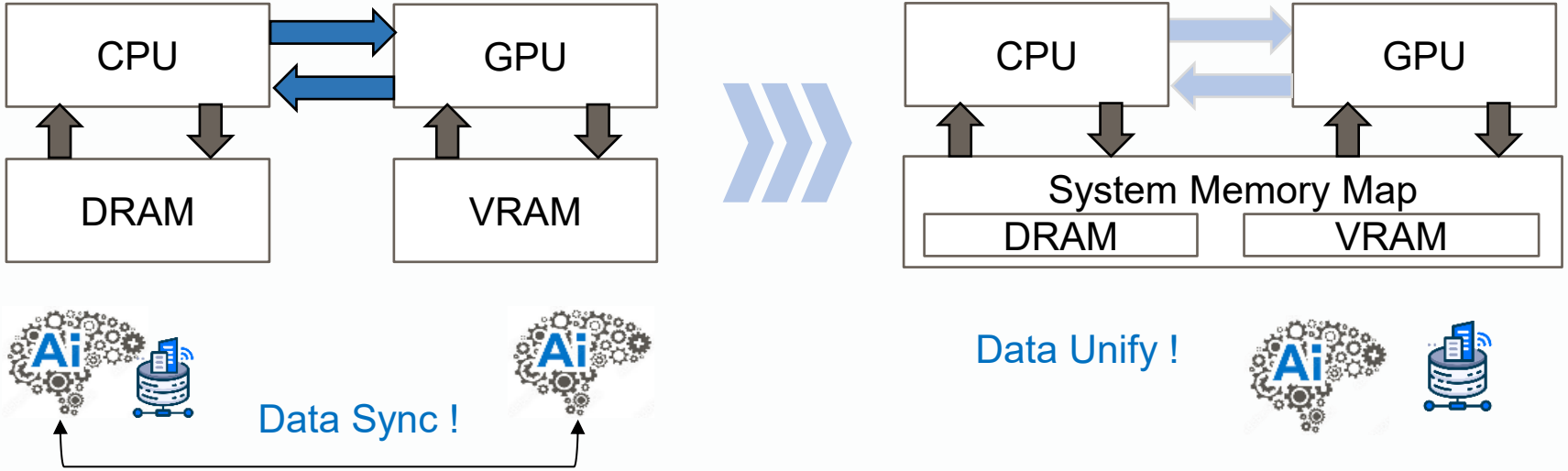


Energy to move data from DRAM to processor is **more than 1,000X** that to compute them.

Power consumption impacts from **AI server** ability toward personal **edge AI** battery life.

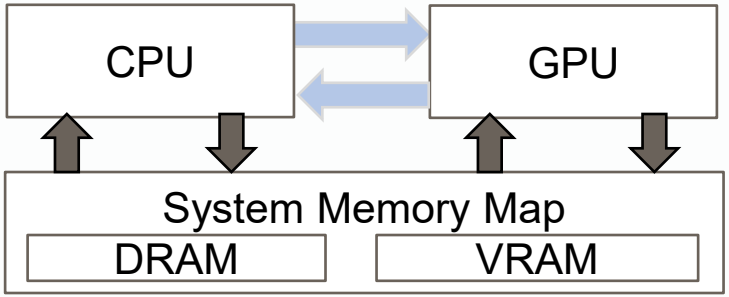
Unified Memory Access Requirement

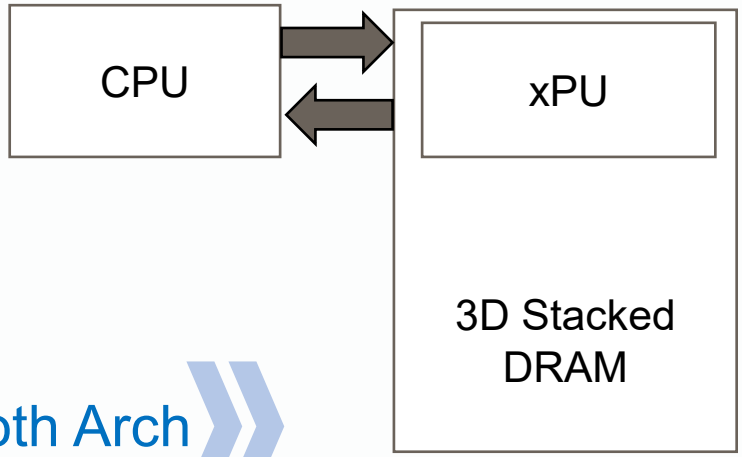
- Heterogeneous computing facilitates complex AI job offloading.
- Unified memory is the key, but challenging in advanced protocols.



aiPIM is Naturally Data Unify

- aiPIM use relatively simple interface, the memory interfaces

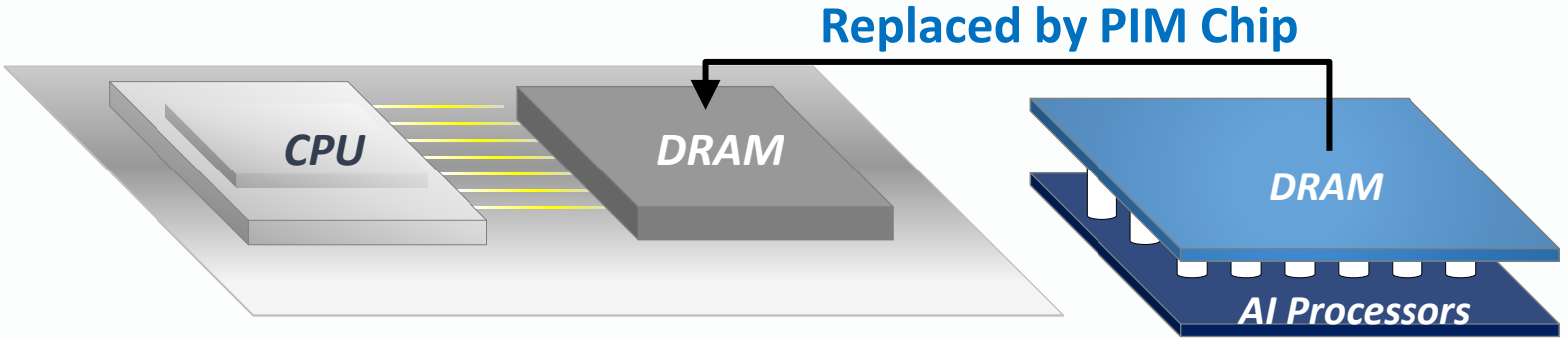




Data Unify in Both Arch

ESMT aiPIM: Drop and Play Concept

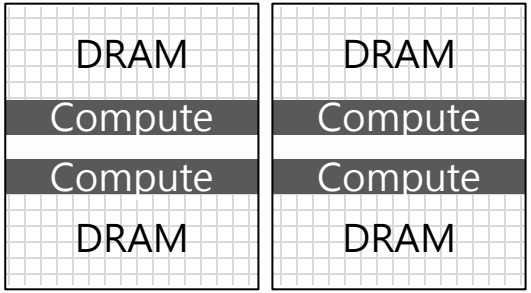
- Pin-to-pin replacement the DRAM with aiPIM.
- Friendly to legacy systems, upgrade immediately.
- Ultra-fast and energy-saving local AI data processing.

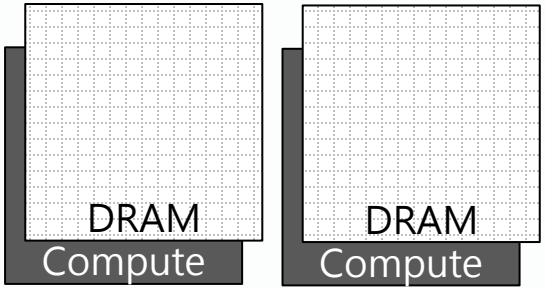


Processing in/near Memory Trend

	UPMEM (Qualcomm) DDR4 DPU	SKHynix AiM	Samsung LPDDR PIM	**ESMT aiPIM**
Interface	DDR4	GDDR6	LPDDR5/6	LPDDR4/5 xSPI
Feature	INT based DDR4 NPU	FP based Assist GPU	INT based Main memory	INT + FP Main Memory
Status	Commercial	Published	Published	Progressing

PIM Chip Decisions: 2D vs 3D





Type	**2D LPDDR PIM**	**3D LPDDR PIM**
Technology	DRAM Process	DRAM Process ， Logic Process
PIM performance	Limited, 2D bandwidth	Flexible, 3D bandwidth
Cost	A little higher	Much higher, p thermal, package
Similarity	GDDR6-AiM	HBM-PIM, aiPIM

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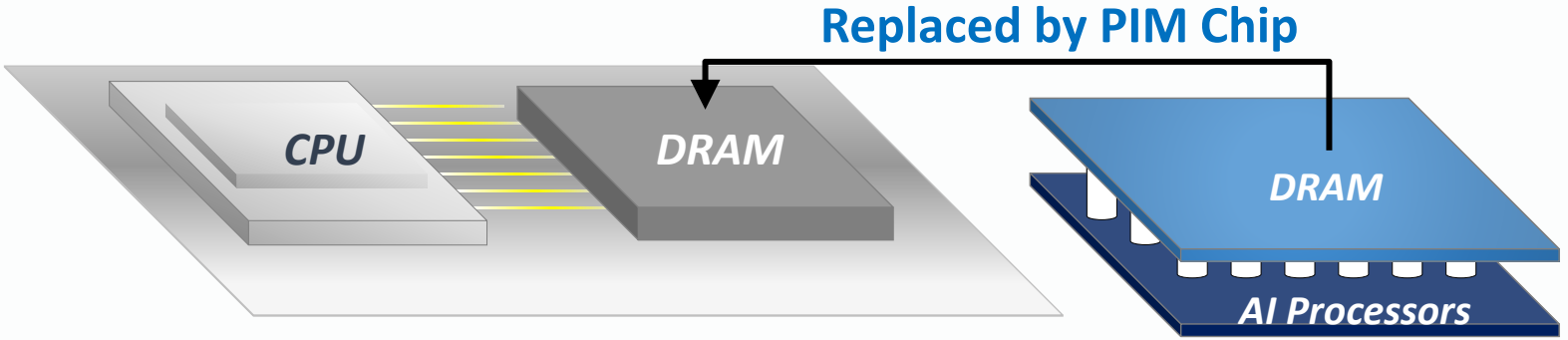
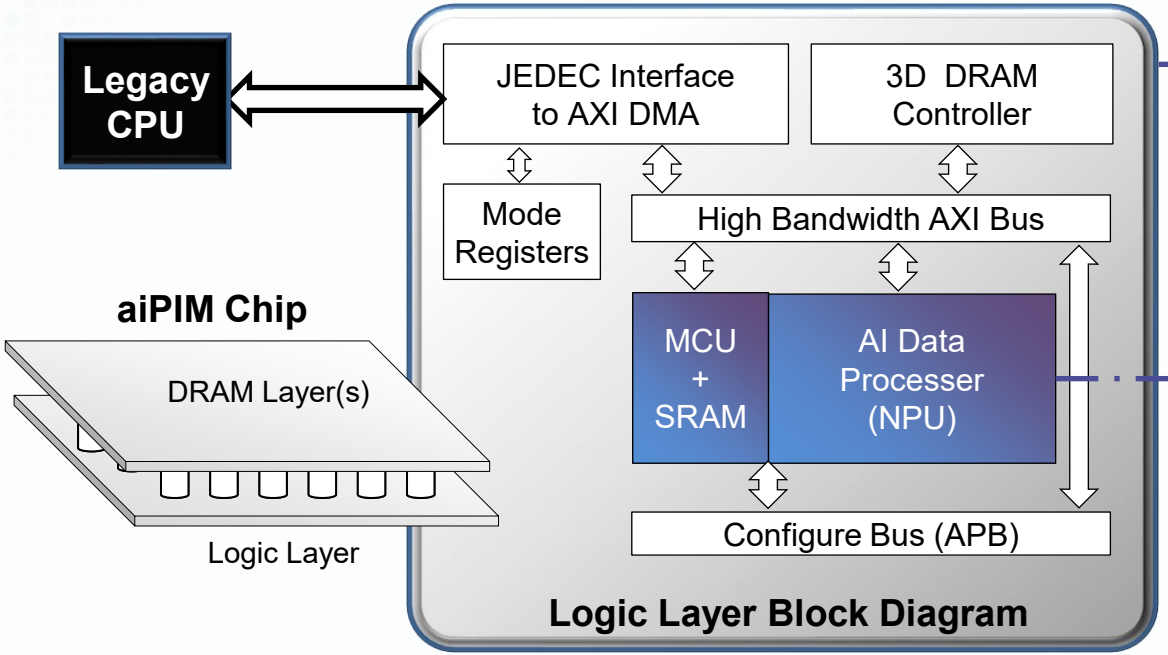


aiPIM Acts Both a Product & a Platform



ESMT provide the 3D PIM Platform.

SoC partners can use their own NPU system inside.

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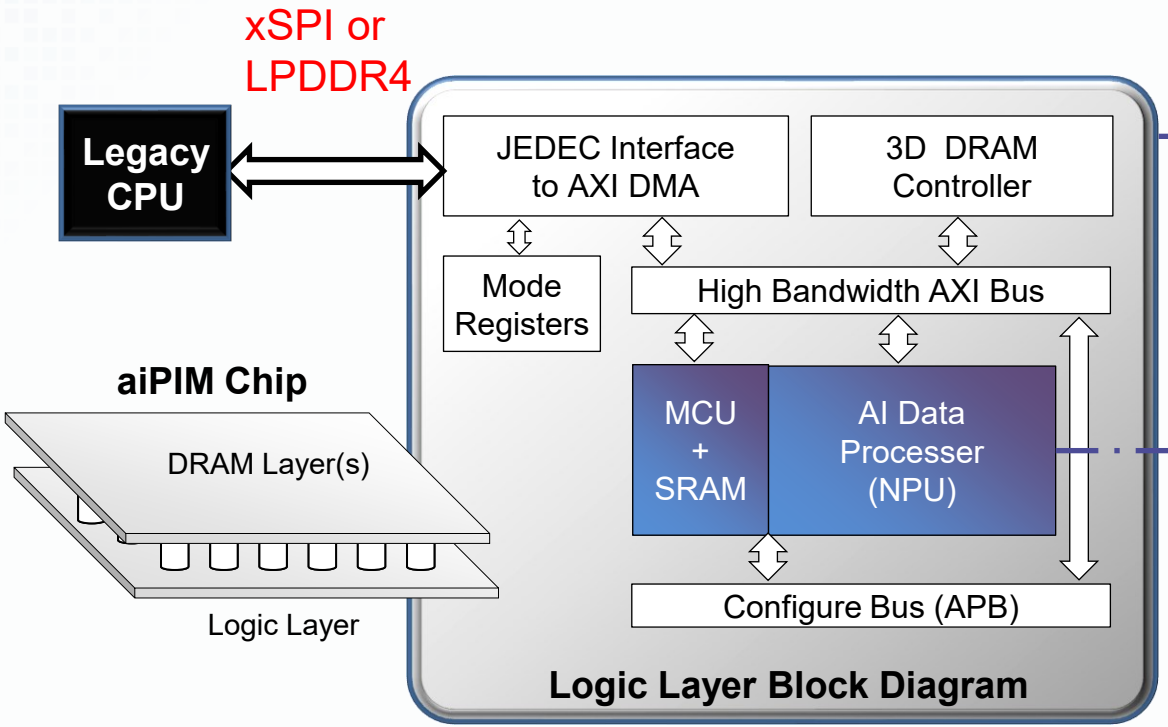

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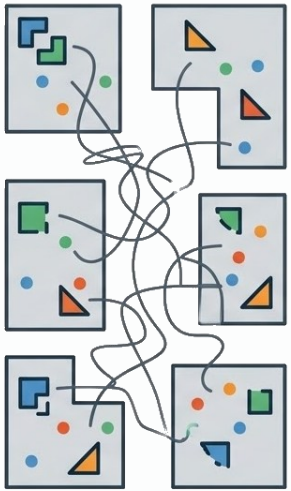
PIM Eco System Challenges

Data Islands (Fragmentation)



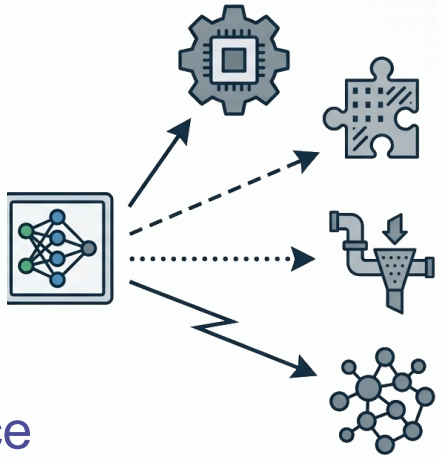
Limits in

- Capacity
- Coherence
- Scalability

Standardization Issue

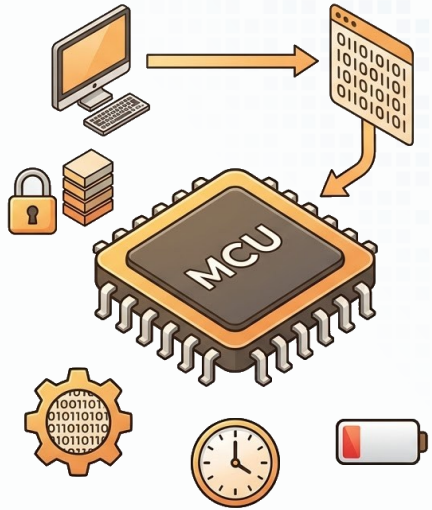
Lack of

- Standard
- Instruction set
- Program interface



aiPIM SDK Approaches

- AIoT MCU Environment
  - ✓Cross-compiled PIM task package
  - ✓SDK with static memory allocation



- Embedded CPU Environment
  - ✓PIM-LIB add-on edge frameworks
  - ✓TF-Lite, ORT-EP, TVM-BYOC, GGML

How aiPIM Overcome Challenges

- Drop and play replacement

  (Legacy LPDDR, xSPI compatible)

- AI Task based, instead of instruction-based

  (not to affect CPU tool chains)

- Constrained, selected edge AI tasks (without diversity)

- Open source PIM library (to promote when ready)

Conclusion :

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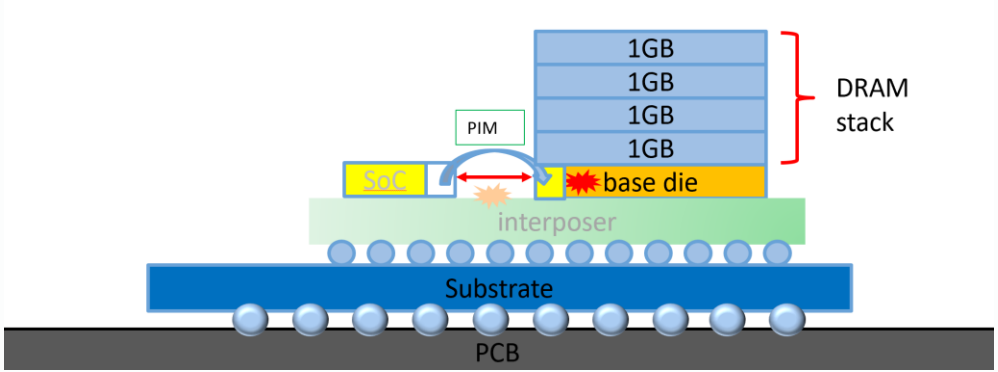
aiPIM lowers the PIM barrier,
by trading extreme flexibility
for market-ready standardization

- A new platform for the 3D processing in memory
- Drop-and-play upgrade for legacy edge systems

Development Schedule

- Phase1 one layer DRAM + Logic (2026)
- Phase2 multi-layers of DRAM + Logic (2027)



Thank you