# High Speed 10M bit/s Photocoupler

## Product Description

The EMD2A611 is an optically coupled gate that combines a light emitting diode and an integrated high gain photo detector. The output of the detector IC is an open collector Schottky clamped transistor.
The internal shield provides a guaranteed common mode transient immunity specification of 10,000 V/μs for the EMD2A611.

This unique design provides maximum AC and DC circuit isolation while achieving TTL compatibility. The optocoupler AC and DC operational parameters are guaranteed from –40°C to +110°C, allowing trouble-free system performance.

The EMD2A611 is suitable for high-speed logic interfacing, input/output buffering, as line receivers in environments that conventional line receivers cannot tolerate and are recommended for use in extremely high ground or induced noise environments.

## Features

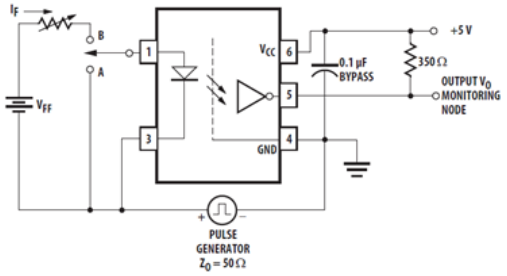
- 10 kV/μs minimum Common Mode Rejection (CMR) at VCM = 1000V
- High speed: 10M bit/s typical
- VCC range: 4.5~5.5V
- LSTTL/TTL compatible
- Inverter logic type
- Low input current capability: 5 mA
- Guaranteed ac and dc performance over -40°C ~ +110°C.

## Applications

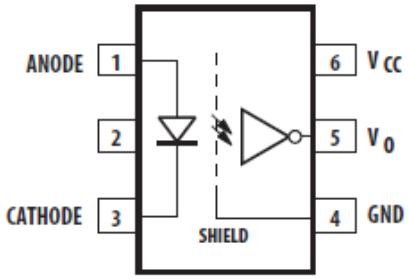
- Isolated line receiver
- Computer-peripheral interfaces
- Microprocessor system interfaces
- Digital isolation for A/D, D/A conversion
- Switching power supply
- Instrument input/output isolation
- Ground loop elimination
- Pulse transformer replacement
- Power transistor isolation in motor drives
- Isolation of high speed logic systems

## Safety approved

- UL1577 recognized with 3750 Vrms for 1 minute for EMD2A611-SK and 5000 Vrms for 1 minute for EMD2A611-SL
  Certificate No. E529603
- IEC/EN/DIN EN 60747-5-5 Approved
  $V_{IORM}$ = 891 Vpeak for EMD2A611-SK
  $V_{IORM}$ = 1140 Vpeak for EMD2A611-SL
  Certificate No. 40055846
- CQC approved: GB4943.1-2011
  Certificate No. CQC22001358589

| SCHEMATIC | PIN DEFINITION | PACKAGE |
|---|---|---|
|  | 1.Anode<br>2.NC<br>3.Cathode<br>4.GND<br>5.VO<br>6.$V_{CC}$ |  |

## Connection Diagram




## Order Information

EMD2A611-00S###%FR1

| | |
|---|---|
| 00 | Internal control Code |
| S### | SK06: LSOP-6 Package 7mm clearance |
| | SL06: LSOP-6 Package 8mm clearance |
| % | E: RoHS & Halogen free package with VDE |
| | N: RoHS & Halogen free package |
| F | -40 to 110°C temperature rating |
| R1 | Packing in Tape & Reel |

## Order, Mark & Packing Information

| Package | Product ID | Mark | | Packing |
|---|---|---|---|---|
| LSOP-6 | EMD2A611-00SK06EFR1<br>EMD2A611-00SL06EFR1 | EYYWW<br>611<br>HV | E : ESMT<br>YY : Date code (Year)<br>WW : Date code (Week)<br>611 : Part Number<br>H : Internal Tracking Code<br>V : VDE Option | Tape & Reel 3Kpcs |
| | EMD2A611-00SK06NFR1<br>EMD2A611-00SL06NFR1 | EYYWW<br>611<br>H | | |

## Absolute Maximum Ratings (Ta = 25°C unless otherwise specified)

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Storage Temperature | Tstg | -55 | 125 | °C |
| Operating Temperature | Topr | -40 | 110 | °C |
| Average Forward Input Current(Note 1) | IF | - | 20 | mA |
| Reverse Input Voltage | VR | - | 5 | V |
| Input Power Dissipation | PI | - | 45 | mW |
| Supply Voltage | VCC | - | 7 | V |
| Output Collector Current | IO | | 50 | mA |
| Output Collector Voltage | VO | | 7 | V |
| Output Collector Power Dissipation | PI | - | 85 | mW |
| Lead Solder Temperature | Tsol | - | 260 | °C |

Note 1: Peaking circuits may produce transient input currents up to 50 mA, 50-ns maximum pulse width, provided average current does not exceed 20 mA

## Recommended Operation Condition

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Operating Temperature | TA | -40 | 110 | °C |
| Supply Voltage | VCC | 4.5 | 5.5 | V |
| Input Current High Level | IFLH | 5 | 15 | mA |
| Input Voltage Low Level | VFHL | -3.0 | 0.8 | V |
| Fan Out (at RL = 1 KΩ) | N | | 5 | TTL Loads |
| Output Pull-up Resistor | RL | 330 | 4K | Ω |

## IEC/EN/DIN EN 60747-5-5 Insulation Characteristics

| Description | Symbol | EMD2A611-SK | EMD2A611-SL | Unit |
|---|---|---|---|---|
| Climatic Classification | -- | 55/100/21 | 55/100/21 | -- |
| Pollution Degree (DIN VDE 0110/1.89) | -- | 2 | 2 | -- |
| Maximum Working Insulation Voltage | $V_{IORM}$ | 891 | 1140 | $V_{peak}$ |
| Input to Output Test Voltage, Method b (Note 2)<br>$V_{IORM}$ x 1.875=$V_{PR}$, 100% Production Test<br>With $t_m$=1sec, Partial discharge < 5pC | $V_{PR}$ | 1671 | 2137 | $V_{peak}$ |
| Input to Output Test Voltage, Method a (Note 2)<br>$V_{IORM}$ x 1.6=$V_{PR}$, 100% Production Test<br>With $t_m$=10sec, Partial discharge < 5pC | $V_{PR}$ | 1426 | 1824 | $V_{peak}$ |
| Highest Allowable Overvoltage<br>(Transient Overvoltage $t_{ini}$ = 60sec) | $V_{IOTM}$ | 6000 | 8000 | $V_{peak}$ |
| Safety-limiting values – maximum values allowed in the event of a failure | | | | |
| Case Temperature | Ts | 175 | 175 | ℃ |
| Input Current | Is, INPUT | 150 | 150 | mA |
| Output Power | Ps, OUTPUT | 600 | 600 | mW |
| Insulation Resistance at TS, $V_{IO}$ = 500 V | Rs | $>10^9$ | $>10^9$ | Ω |

Note 2 : Refer to the optocoupler section of th Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.
These optocouplers are suitable for "safe electrical isolation" only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits. Surface mount classification is Class A accordance with CECC 00802.

## Insulation and Safety-Related Specifications

| Parameter | Symbol | EMD2A | | Unit | Conditions |
|---|---|---|---|---|---|
| | | 611-SK | 611-SL | | |
| Minimum External Air Gap (External Clearance) | L(101) | 7.0 | 8.0 | mm | Measured from input terminals to output terminals, shortest distance through air. |
| Minimum External Tracking (External Creepage) | L(102) | 8.0 | 8.0 | mm | Measured from input terminals to output terminals, shortest distance path along body. |
| Tracking Resistance (Comparative Tracking Index) | CTI | >175 | >175 | V | DIN IEC 112/VDE 0303 Part 1. |

## Electrical Characteristics (DC)

All Typical values at $T_A$ = 25°C and $V_{CC}$ = 5 V, unless otherwise specified; all minimum and maximum specifications are at recommended operating condition.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Condition |
|---|---|---|---|---|---|---|
| High Level Output Current | IOH | - | 0.35 | 100 | µA | VCC = 5.5V, VO = 5.5V, VF = 0.8V |
| Input Threshold Current | ITH | - | 1.0 | 5.0 | mA | VCC = 5.5V, VO = 0.6V, IOL > 13 mA |
| Low Level Output Voltage | VOL | - | 0.25 | 0.6 | V | VCC = 5.5V, IF = 5 mA, IOL(Sinking) = 13 mA |
| High Level Supply Current | ICCH | - | 5.6 | 7.5 | mA | VCC = 5.5V, IF = 0 mA, |
| Low Level Supply Current | ICCL | - | 5.2 | 10.5 | mA | VCC = 5.5V, IF = 10 mA |
| Input Forward Voltage | VF | 1.6 | 2.0 | 2.4 | V | IF = 10 mA |
| Input Reverse Breakdown Voltage | BVR | 5 | - | - | V | IR = 10 µA |
| Input Capacitance | CIN | - | 60 | - | pF | f = 1 MHz, VF = 0V |

## Switching Specification (AC)

All Typical values at TA = 25°C and $V_{CC}$ = 5 V, IF = 7.5mA, unless otherwise specified; all minimum and maximum specifications are at recommended operating condition.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Condition |
|---|---|---|---|---|---|---|
| Propagation Delay Time to High Output Level | tPLH | - | 60 | 75 | ns | VCC = 5V, IF = 7.5 mA, RL = 350Ω, CL = 15 pF |
| Propagation Delay Time to Low Output Level | tPHL | - | 35 | 75 | | |
| Pulse Width Distortion | \| tPHL-tPLH \| | - | 25 | 40 | | |
| Propagation Delay Skew | tPSK | - | - | 50 | | |
| Output Rise Time (10 to 90%) | tr | - | 30 | - | | |
| Output Fall Time (90 to 10%) | tf | - | 3 | - | | |
| Common mode transient immunity at high level output (Note 3) | \| CMH \| | 10 | 15 | - | kV/µs | VCC = 5V, IF = 0 mA, VO(MIN) = 2V,RL = 350Ω, VCM = 1000V |
| Common mode transient immunity at low level output (Note 4) | \| CML \| | 10 | 15 | - | kV/µs | VCC = 5V, IF = 7.5 mA, VO(MAX) = 0.8V,RL = 350Ω, VCM = 1000V |

Note 3 : CMH is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (that is, VOUT > 2.0V).
Note 4 : CML is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (that is, VOUT > 0.8V).

## Isolation characteristic

All Typical values at $T_A$ = 25°C and $V_{CC}$ = 5 V, unless otherwise specified; all minimum and maximum specifications are at recommended operating condition.

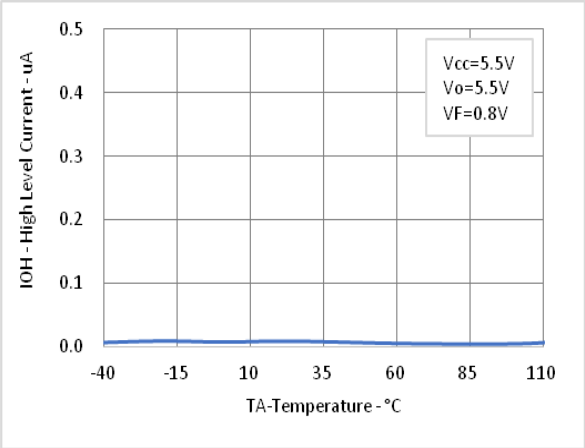
| Parameter | Symbo | Device | Min. | Typ. | Max. | Unit | Test Condition |
|---|---|---|---|---|---|---|---|
| Withstand Insulation Test Voltage (Note 5, 6) | $V_{ISO}$ | EMD2A611-SK | 5000 | - | - | V | RH ≤ 40%-60%, t = 1min, $T_A$ = 25 °C |
| | | EMD2A611-SL | | | | | |
| Input-Output Resistance (Note 5) | $R_{I-O}$ | - | - | $10^{12}$ | - | Ω | $V_{I-O}$ = 500V DC |

Note 5: Device is considered a two terminal device: pins 1, 2, 3 are shorted together and pins 4, 5, 6 are shorted together.

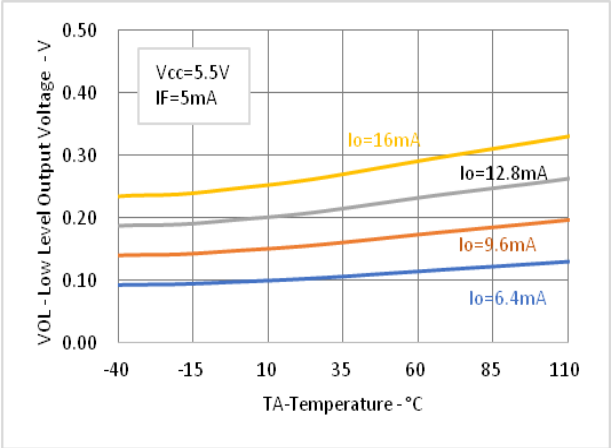
Note 6: According to UL1577, each photo coupler is tested by applying an insulation test voltage 6000VRMS for one second (leakage current less than 10uA). This test is performed before the 100% production test for partial discharge.

## Typical Performance Curves & Test Circuits

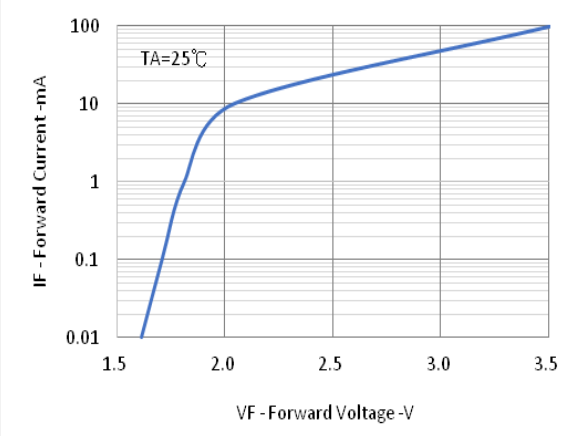
### Fig.1 High Level Output Current vs. Temp




### Fig.2 Low Level Output Voltage vs. Temp




### Fig.3 Input Diode Forward Characteristic




### Fig.4 Output Voltage vs. Input Current

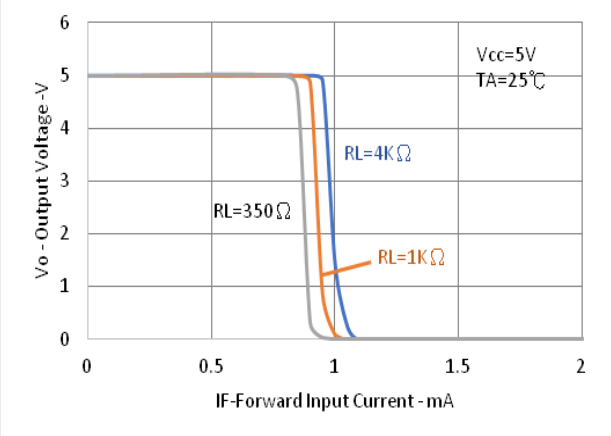


**Fig.5 Low Level Output Current vs. Temp**

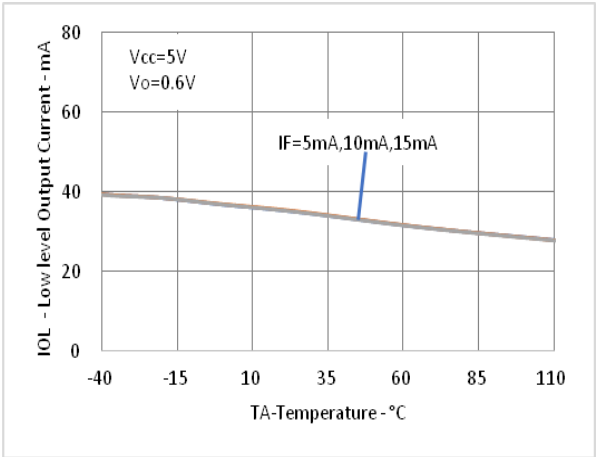



**Fig.6 Propagation Delay vs. Temperature**

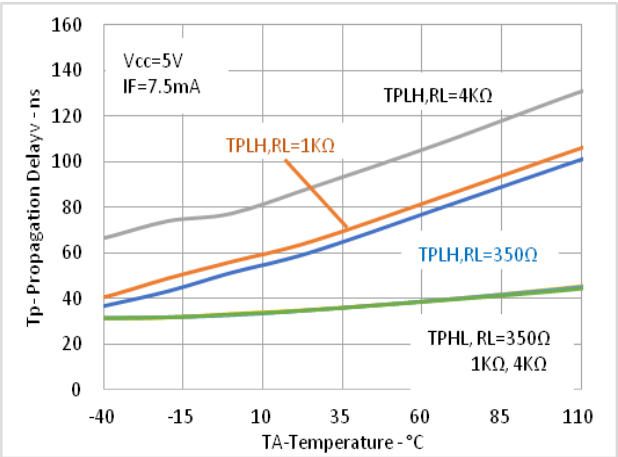



**Fig.7 Propagation Delay vs. Input Current**

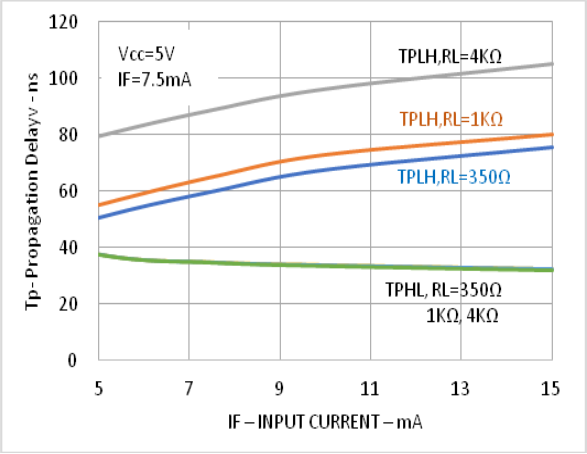



**Fig.8 Pulse Width Distortion vs. Temperature**

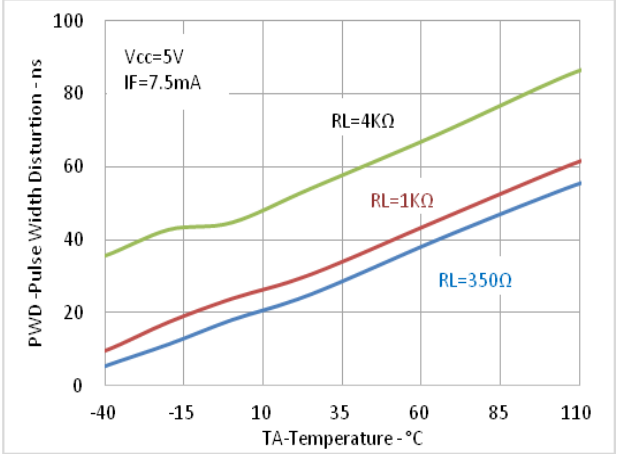



**Fig.9 Rise and Fall Time vs. Temperature**

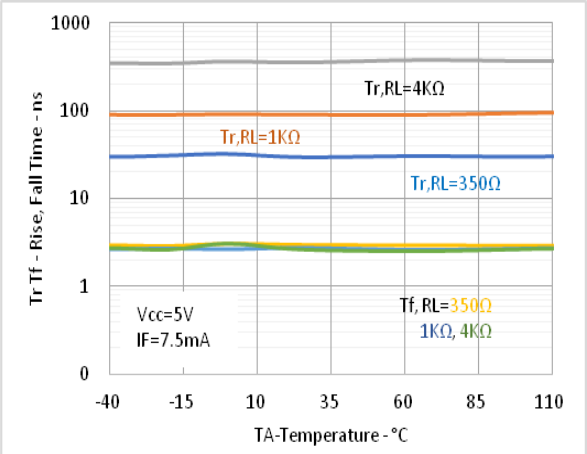
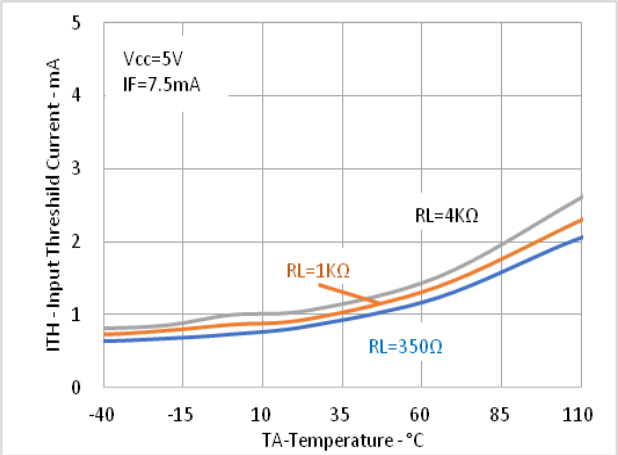
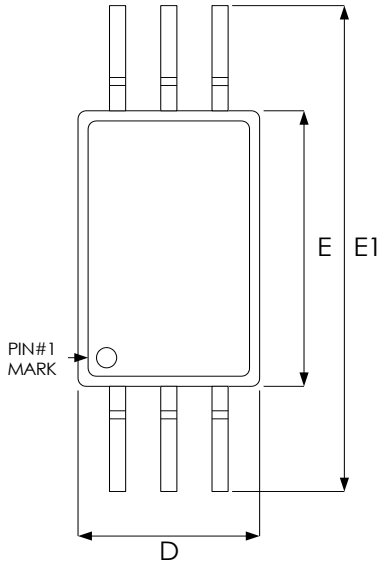


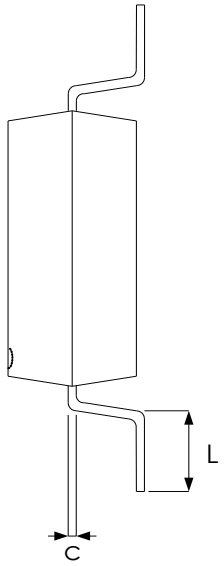

**Fig.10 Input Threshold Current vs. Temp**



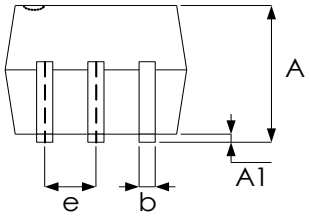
**Package Outline Drawing**
**L-SOP 6L (277mil, 7mm clearance)**




**TOP VIEW**



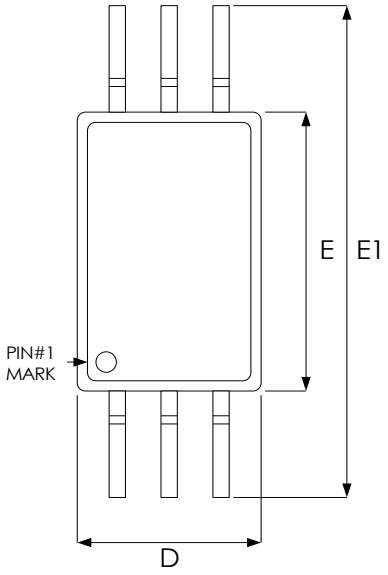

**SIDE VIEW**



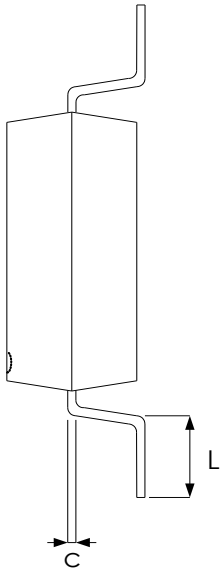

**BOTTOM VIEW**

| Symbol | Dimension in mm | |
|---|---|---|
| | Min. | Max. |
| A | 1.70 | 2.30 |
| A1 | 0.10 | 0.30 |
| b | 0.30 | 0.50 |
| c | 0.20 | 0.30 |
| D | 4.20 | 4.80 |
| E | 6.50 | 7.10 |
| E1 | 9.40 | 10.00 |
| e | 1.27 BSC | |
| L | 0.70 | 1.20 |

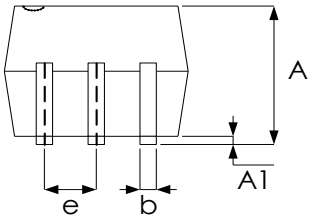
**Package Outline Drawing**
**L-SOP 6L (277mil, 8mm clearance)**




**TOP VIEW**




**SIDE VIEW**




**BOTTOM VIEW**

| Symbol | Dimension in mm | |
|---|---|---|
| | Min. | Max. |
| A | 1.70 | 2.30 |
| A1 | 0.10 | 0.30 |
| b | 0.30 | 0.50 |
| c | 0.20 | 0.30 |
| D | 4.20 | 4.80 |
| E | 6.51 | 7.11 |
| E1 | 11.20 | 11.80 |
| e | 1.27 BSC | |
| L | 0.50 | 1.00 |

## Revision History

| Revision | Date | Description |
|---|---|---|
| 0.1 | 2023.02.03 | Preliminary version |
| 0.2 | 2023.06.01 | Update: 1. High Speed Information (page1)<br>2. Insulation Characteristics (page4) |

Important Notice



The contents contained in this document are believed to be accurate at the time of publication. ESMT assumes no responsibility for any error in this document, and reserves the right to change the products or specification in this document without notice.

The information contained herein is presented only as a guide or examples for the application of our products. No responsibility is assumed by ESMT for any infringement of patents, copyrights, or other intellectual property rights of third parties which may result from its use. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of ESMT or others.

Any semiconductor devices may have inherently a certain rate of failure. To minimize risks associated with customer's application, adequate design and operating safeguards against injury, damage, or loss from such failure, should be provided by the customer when making application designs.

ESMT's products are not authorized for use in critical applications such as, but not limited to, life support devices or system, where failure or abnormal operation may directly affect human lives or cause physical injury or property damage. If products described here are to be used for such kinds of application, purchaser must do its own quality assurance testing appropriate to such applications.