eMMC Flash

3.3V 64 Gbyte eMMC Flash Memory

Features

- Compatible to JEDEC Embedded Multi Media Card (eMMC) Electrical Standard (5.1)
- Data bus width: 1bit(Default), 4bit and 8bit
- Not support large sector size (4KB)
- Interface power: V_{CCQ} (1.70V~1.95V or 2.7V~3.6V), Memory power: V_{CC} (2.7V~3.6V)
- Temperature: Operation (-25°C~85°C), storage (-40°C~85°C)
- User Density:

Density	LBA (Hex)	LBA (Dec)	Capacity (Bytes)
64 GB	0x747C000	122,142,720	62,537,072,640

System Performance

Table 1. Read/Write Performance

Product ID	Read Sequential (MB/S)	Write Sequential (MB/S)
FC51J64SJTS1A-2.5BWGE2C	290	195

Note:
1. Values given for an 8-bit bus width, running HS400 mode from ESMT proprietary tool
2. Performance numbers might be subject to changes without notice.

Table 2. Capacity according to partition

Capactity	Boot Partition 1	Boot Partition 2	RPMB
64 GB	4096 KB	4096 KB	4096 KB

Table 3. Ordering Information

Product ID	Speed	Package	Comments
FC51J64SJTS1A-2.5BWGE2C	200 MHz	153 ball BGA	Pb-free

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Figure 1. Ball Configuration (Top View)

(BGA 153 Ball, 11.5 mmx13 mmx1.0 mm Body, 0.5 mm Ball Pitch)

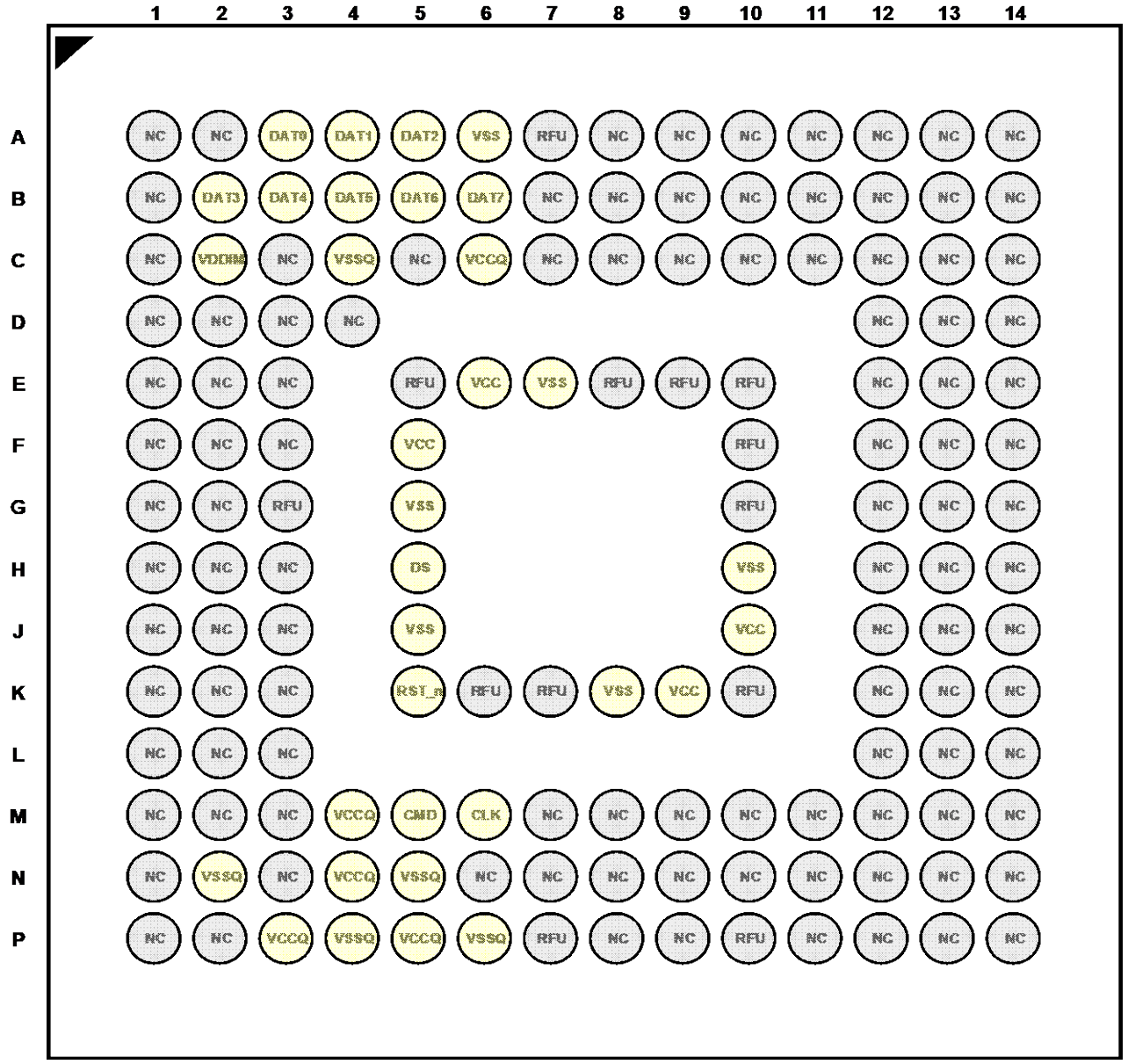


Table 4. Ball Descriptions

Ball Name	Type*1	Function
DAT0~DAT7	I/O/PP	Data Input/Output
DS	O/PP	Data Strobe
CLK	I	Clock
CMD	I/O/PP/OD	Command
VCC	S	Power Supply for Flash
VCCQ	S	Power Supply for Controller
VDDIM	-	Internal voltage node
VSS	S	Ground for Controller Flash
VSSQ	S	I/O Ground
RST_n	I	Reset
NC	NC	No Connection
RFU	-	Reserved For Future Use

Note:

1. I: input; O: Output; PP: push-pull; OD: open-drain; NC: Not connected (or logical high); S: power supply.

eMMC Register Value

Table 5. OCR Register

OCR bit	Voltage window	Register Value
[6:0]	Reserved	000 0000b
[7]	1.70 – 1.95	1b
[14:8]	2.0-2.6	000 0000b
[23:15]	2.7-3.6	1 1111 1111b
[28:24]	Reserved	000 0000b
[30:29]	Access Mode	00b (byte mode), 10b (sector mode)
[31]	Card power up status bit (busy)*	

Note*： This bit is set to LOW if the e•MMC has not finished the power up routine. The supported voltage range is coded as shown in table.

Table 6. CID Register

Name	Field	Width	CID-slice	CID Value
Manufacture ID	MID	8	[127:120]	ECh
Reserved	-	6	[119:114]	0h
Card/BGA	CBX	2	[113:112]	1h
OEM/Application ID	OID	8	[111:104]	0h
Product name	PNM	48	[103:56]	534A54314330h
Product revision	PRV	8	[55:48]	10h
Product serial number	PSN	32	[47:16]	set at test
Manufacture date	MDT	8	[15:8]	set at test
CRC7 checksum	CRC	7	[7:1]	set at test
not used, always ‘1’	-	1	[0:0]	1h

Table 7. CSD Register

Name	Field	Width	Cell Type	CSD-slice	CSD Value
CSD Structure	CSD-STRUCTURE	2	R	[127:126]	3h
System specification version	SPEC_VERS	4	R	[125:122]	4h
Reserved	-	2	R	[121:120]	0h
Data read access-time 1	TAAC	8	R	[119:112]	2Fh
Data read access-time 2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	1h
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	2Ah
Device command classes	CCC	12	R	[95:84]	5F5h
Max. read data block length	READ_BL_LEN	4	R	[83:80]	9h
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0h
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0h
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0h
DSR implemented	DSR_IMP	1	R	[76:76]	0h
Reserved	-	2	R	[75:74]	0h
Device size	C_SIZE	12	R	[73:62]	FFFh
Max. read current@VDD min	VDD_R_CURR_MIN	3	R	[61:59]	6h
Max. read current@VDD max	VDD_R_CURR_MAX	3	R	[58:56]	6h
Max. write current@VDD min	VDD_W_CURR_MIN	3	R	[55:53]	6h
Max. write current@VDD max	VDD_W_CURR_MAX	3	R	[52:50]	6h
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	7h
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	1Fh
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	1Fh
Write Protect group size	WP_GRP_SIZE	5	R	[36:32]	1Fh
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	1h
Manufacture default ECC	DEFAULT_ECC	2	R	[30:29]	0h
Write speed factor	R2W_FACTOR	3	R	[28:26]	1h
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	9h
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0h
Reserved	-	4	R	[20:17]	0h
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0h
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0h
Copy flag(OTP)	COPY	1	R/W	[14:14]	0h
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0h
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0h
File Format	FILE_FORMAT	2	R/W	[11:10]	0h
ECC code	ECC	2	R/W/E	[9:8]	0h
CRC	CRC	7	R/W/E	[7:1]	Dh
Not used, always ‘1’	-	1	-	[0:0]	1h

Table 8. Extended CSD Register

Name	Field	Size	Cell Type	CSD- slice	CSD Value
Reserved	-	6	TBD	[511:506]	0h
Extended Security Commands Error	EXT_SECURITY_ERR	1	R	[505]	0h
Supported Command Sets	S_CMD_SET	1	R	[504]	1h
HPI features	HPI_FEATURES	1	R	[503]	3h
Background operations support	BKOPS_SUPPORT	1	R	[502]	1h
Max packed read commands	MAX_PACKED_READS	1	R	[501]	3Fh
Max packed write commands	MAX_PACKED_WRITES	1	R	[500]	3Fh
Data Tag Support	DATA_TAG_SUPPORT	1	R	[499]	1h
Tag Unit Size	TAG_UNIT_SIZE	1	R	[498]	1h
Tag Resources Size	TAG_RES_SIZE	1	R	[497]	0h
Context management capabilities	CONTEXT_CAPABILITIES	1	R	[496]	5h
Large Unit size	LARGE_UNIT_SIZE_M1	1	R	[495]	0h
Extended partitions attribute support	EXT_SUPPORT	1	R	[494]	3h
Supported modes	SUPPORTED_MODES	1	R	[493]	1h
FFU features	FFU_FEATURES	1	R	[492]	1h
Operation codes timeout	OPERATION_CODE_TIMEOUT	1	R	[491]	17h
FFU Argument	FFU_ARG	4	R	[490:487]	0h
Barrier support	BARRIER_SUPPORT	1	R	[486]	0h
Reserved	-	177	TBD	[485:309]	0h
CMD Queuing Support	CMDQ_SUPPORT	1	R	[308]	1h
CMD Queuing Depth	CMDQ_DEPTH	1	R	[307]	3h
Reserved	-	1	TBD	[306]	0h
Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	4	R	[305:302]	0h
Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT	32	R	[301:270]	0h
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	R	[269]	1h
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	R	[268]	1h
Pre EOL information	PRE_EOL_INFO	1	R	[267]	1h
Optimal read size	OPTIMAL_READ_SIZE	1	R	[266]	8h
Optimal write size	OPTIMAL_WRITE_SIZE	1	R	[265]	8h
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	8h
Device version	DEVICE_VERSION	2	R	[263:262]	0h
Firmware version	FIRMWARE_VERSION	8	R	[261:254]	FW Version

Table 8. Extended CSD Register - Continued

Name	Field	Size	Cell Type	CSD- slice	CSD Value
Power class for 200MHz, DDR at VCC= 3.6V	PWR_CL_DDR_200_360	1	R	[253]	0h
Cache size	CACHE_SIZE	4	R	[252:249]	100h
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	32h
Power off notification(long) timeout	POWER_OFF_LONG_TIME	1	R	[247]	3Ch
Background operations status	BKOPS_STATUS	1	R	[246]	0h
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0h
1st initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	1Eh
Cache Flushing Policy	CACHE_FLUSH_POLICY	1	R	[240]	0h
Power class for 52MHz, DDR at V_{CC} = 3.6V	PWR_CL_DDR_52_360	1	R	[239]	0h
Power class for 52MHz, DDR at V_{CC} = 1.95V	PWR_CL_DDR_52_195	1	R	[238]	0h
Power class for 200MHz at V_{CCQ} =1.95V, V_{CC} = 3.6V	PWR_CL_200_195	1	R	[237]	0h
Power class for 200MHz at V_{CCQ} =1.3V, V_{CC} = 3.6V	PWR_CL_200_130	1	R	[236]	0h
Minimum Write Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	0h
Minimum Read Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	0h
Reserved	-	1	TBD	[233]	0h
TRIM Multiplier	TRIM_MULT	1	R	[232]	2h
Secure Feature support	SEC_FEATURE_SUPPORT	1	R	[231]	55h
Secure Erase Multiplier	SEC_ERASE_MULT	1	R	[230]	1Bh
Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	[229]	11h
Boot information	BOOT_INFO	1	R	[228]	7h
Reserved	-	1	TBD	[227]	0h
Boot partition size	BOOT_SIZE_MULTI	1	R	[226]	20h
Access size	ACC_SIZE	1	R	[225]	6h
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	[224]	1h
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	1h
Reliable write sector count	REL_WR_SEC_C	1	R	[222]	1h
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	20h
Sleep current (VCC)	S_C_VCC	1	R	[220]	7h
Sleep current (VCCQ)	S_C_VCCQ	1	R	[219]	7h
Production state awareness timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT	1	R	[218]	17h
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	17h
Sleep Notification Timout[1]	SLEEP_NOTIFICATION_TIME	1	R	[216]	11h

Table 8. Extended CSD Register - Continued

Name	Field	Size	Cell Type	CSD- slice	CSD Value
Sector Count	SEC_COUNT	4	R	[215:212]	747C000h
Secure Write Protect Information	SECURE_WP_INFO	1	R	[211]	0h
Minimum Write Performance for 8bit at 52MHz	MIN_PERF_W_8_52	1	R	[210]	0h
Minimum Read Performance for 8bit at 52MHz	MIN_PERF_R_8_52	1	R	[209]	0h
Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0h
Minimum Read Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0h
Minimum Write Performance for 4bit at 26MHz	MIN_PERF_W_4_26	1	R	[206]	0h
Minimum Read Performance for 4bit at 26MHz	MIN_PERF_R_4_26	1	R	[205]	0h
Reserved	-	1	TBD	[204]	0h
Power class for 26MHz at 3.6V 1 R	PWR_CL_26_360	1	R	[203]	0h
Power class for 52MHz at 3.6V 1 R	PWR_CL_52_360	1	R	[202]	0h
Power class for 26MHz at 1.95V 1 R	PWR_CL_26_195	1	R	[201]	0h
Power class for 52MHz at 1.95V 1 R	PWR_CL_52_195	1	R	[200]	0h
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	5h
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	19h
I/O Driver Strength	DRIVER_STRENGTH	1	R	[197]	1Fh
Device type	DEVICE_TYPE	1	R	[196]	57h
Reserved	-	1	TBD	[195]	0h
CSD STRUCTURE	CSD_STRUCTURE	1	R	[194]	2h
Reserved	-	1	TBD	[193]	0h
Extended CSD revision	EXT_CSD_REV	1	R	[192]	8h
Modes Segment					
Command set	CMD_SET	1	R/W/E_P	[191]	0h
Reserved	-	1	TBD	[190]	0h
Command set revision	CMD_SET_REV		R	[189]	0h
Reserved	-	1	TBD	[188]	0h
Power class	POWER_CLASS		R/W/E_P	[187]	0h
Reserved	-	1	TBD	[186]	0h
High-speed interface timing	HS_TIMING	1	R/W/E_P	[185]	0h
Strobe Support	STROBE_SUPPORT	1	R	[184]	1h
Bus width mode	BUS_WIDTH	1	W/E_P	[183]	0h
Reserved	-	1	TBD	[182]	0h
Erased memory content	ERASED_MEM_CONT	1	R	[181]	0h
Reserved	-	1	TBD	[180]	0h

Table 8. Extended CSD Register - Continued

Name	Field	Size	Cell Type	CSD- slice	CSD Value
Partition configuration	PARTITION_CONFIG	1	R/W/E & R/W/E_P	[179]	0h
Boot config protection	BOOT_CONFIG_PROT	1	R/W & R/W/C_P	[178]	0h
Boot bus Conditions	BOOT_BUS_CONDITIONS	1	R/W/E	[177]	0h
Reserved	-	1	TBD	[176]	0h
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	[175]	0h
Boot write protection status registers	BOOT_WP_STATUS	1	R	[174]	0h
Boot area write protection register	BOOT_WP	1	R/W & R/W/C_P	[173]	0h
Reserved	-	1	TBD	[172]	0h
User area write protection register	USER_WP	1	R/W, R/W/C_P & R/W/E_P	[171]	0h
Reserved	-	1	TBD	[170]	0h
FW configuration	FW_CONFIG	1	R/W	[169]	0h
RPMB Size	RPMB_SIZE_MULT	1	R	[168]	20h
Write reliability setting register	WR_REL_SET	1	R/W	[167]	0h
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	14h
Start Sanitize operation	SANITIZE_START	1	W/E_P	[165]	0h
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0h
Enable background operations handshake	BKOPS_EN	1	R/W	[163]	0h
H/W reset function	RST_n_FUNCTION	1	R/W	[162]	0h
HPI management	HPI_MGMT	1	R/W/E_P	[161]	0h
Partitioning Support	PARTITIONING_SUPPORT	1	R	[160]	7h
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	4C9h
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0h
Partitioning Setting	PARTITION_SETTING_ COMPLETED	1	R/W	[155]	0h
General Purpose Partition Size	GP_SIZE_MULT	12	R/W	[154:143]	0h
Enhanced User Data Area Size	ENH_SIZE_MULT	3	R/W	[142:140]	0h
Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	[139:136]	0h
Reserved	-	1	TBD	[135]	0h
Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	0h
Production state awareness	PRODUCTION_STATE_AWAR ENESS	1	R/W/E	[133]	0h
Package Case Temperature is controlled	TCASE_SUPPORT	1	W/E_P	[132]	0h

Table 8. Extended CSD Register - Continued

Name	Field	Size	Cell Type	CSD- slice	CSD Value
Periodic Wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	0h
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	1	R	[130]	1h
Reserved	-	2	TBD	[129:128]	0h
Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	64	vendor specific	[127:64]	0h
Native sector size	NATIVE_SECTOR_SIZE	1	R	[63]	0h
Sector size emulation	USE_NATIVE_SECTOR	1	R/W	[62]	0h
Sector size	DATA_SECTOR_SIZE	1	R	[61]	0h
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	[60]	0h
Class 6 commands control	CLASS_6_CTRL	1	R/W/E_P	[59]	0h
Number of addressed group to be Released	DYNCAP_NEEDED	1	R	[58]	0h
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	0h
Exception events status	EXCEPTION_EVENTS_STATUS	2	R	[55:54]	0h
Extended Partitions Attribute	EXT_PARTITIONS_ATTRIBUTE	2	R/W	[53:52]	0h
Context configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	0h
Packed command status	PACKED_COMMAND_STATUS	1	R	[36]	0h
Packed command failure index	PACKED_FAILURE_INDEX	1	R	[35]	0h
Power Off Notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	0h
Control to turn the Cache ON/OFF	CACHE_CTRL	1	R/W/E_P	[33]	0h
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	0h
Reserved	-	1	TBD	[31]	0h
Mode config	MODE_CONFIG	1	R/W/E_P	[30]	0h
Mode operation codes	MODE_OPERATION_CODES	1	W/E_P	[29]	0h
Reserved	-	2	TBD	[28:27]	0h
FFU status	FFU_STATUS	1	R	[26]	0h
Pre loading data size	PRE_LOADING_DATA_SIZE	4	R/W/E_P	[25:22]	0h
Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	4	R	[21:18]	2648000h
Product state awareness enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT	1	R/W/E & R	[17]	3h
Secure Removal Type	SECURE_REMOVAL_TYPE	1	R/W & R	[16]	9h
Command Queue Mode Enable	CMDQ_MODE_EN	1	R/W/E_P	[15]	0h
Reserved	-	15	TBD	[14:0]	0h

Note：Reserved bits should be read as “0”.

Bus Signal Levels

Figure 2. Bus Signal Levels

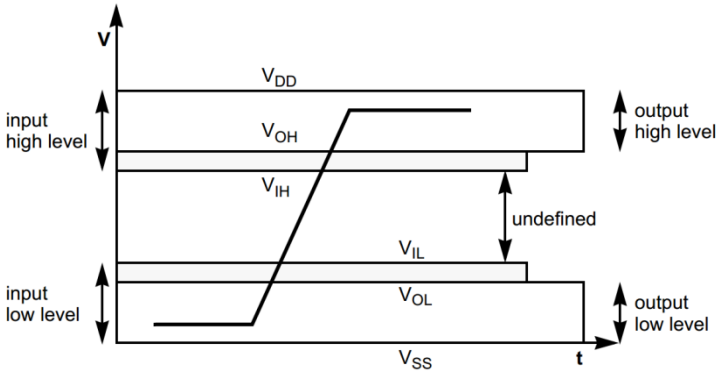


Table 9. Bus Signal Levels

Paramter	Symbol	Min	Max	Unit	Remark
Open-drain bus signal level					
Output HIGH voltage	V_{OH}	V_{CCQ} - 0.2	-	V	
Output LOW voltage	V_{OL}	-	0.3	V	I_{OL} = 2mA
Push-pull bus signal level (2.7V~3.6V V_{CCQ})					
Output HIGH voltage	V_{OH}	0.75 * V_{CCQ}	-	V	I_{OH} = -100uA @ V_{CCQ} min
Output LOW voltage	V_{OL}	-	0.125 * V_{CCQ}	V	I_{OL} = 100uA @ V_{CCQ} min
Input HIGH voltage	V_{IH}	0.625* V_{CCQ}	V_{CCQ} + 0.3	V	
Input LOW voltage	VI_L	V_{SS} - 0.3	0.25 * V_{CCQ}	V	
Push-pull bus signal level (1.70V~1.95V V_{CCQ})					
Output HIGH voltage	V_{OH}	V_{CCQ} - 0.45	-		I_{OH} = - 2mA
Output LOW voltage	V_{OL}	-	0.45		I_{OL} = 2mA
Input HIGH voltage	V_{IH}	0.65 * V_{CCQ}	V_{CCQ} + 0.3		
Input LOW voltage	VI_L	V_{SS} - 0.3	0.35*V_{CCQ}		

Bus Timing

Device Interface Timings

Figure 3. Bus Timing in Single Data Rate Mode

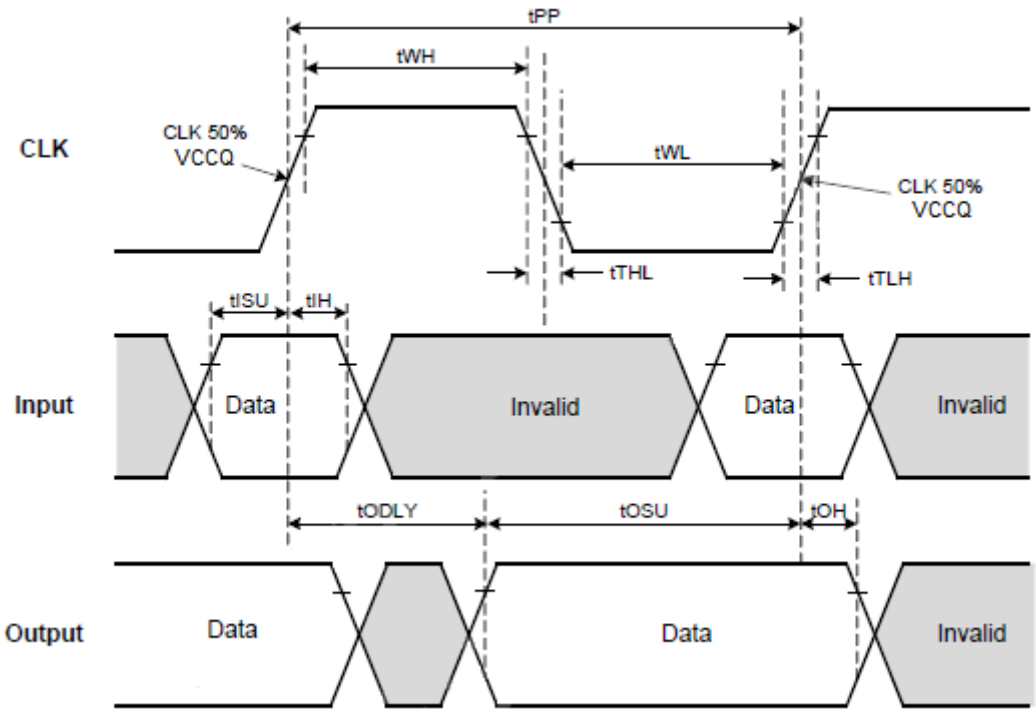


Table 10. High-Speed Device Interface Timing

Paramter	Symbol	Min	Max	Unit	Remark
Clock CLK[*1]					
Clock frequency data transfer mode (PP)[*2]	f_{PP}	0	52[*3]	MHz	CL ≤ 30pF Tolerance: +100kHz
Clock frequency identification mode (OD)	f_{OD}	0	400	kHz	Tolerance: +20kHz
Clock high time	t_{WH}	6.5	-	ns	CL ≤ 30pF
Clock low time	t_{WL}	6.5	-	ns	CL ≤ 30pF
Clock rise time[*4]	t_{TLH}	-	3	ns	CL ≤ 30pF
Clock fall time	t_{THL}	-	3	ns	CL ≤ 30pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3	-	ns	CL ≤ 30pF
Input hold time	t_{IH}	3	-	ns	CL ≤ 30pF
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer	t_{ODLY}	-	13.7	ns	CL ≤ 30pF
Output hold time	t_{OH}	2.5	-	ns	CL ≤ 30pF
Signal rise time[*5]	t_{RISE}	-	3	ns	CL ≤ 30pF
Signal fall time	t_{FALL}	-	3	ns	CL ≤ 30pF

Note:

1. CLK timing is measured at 50% of V_{CCQ}.
2. A e•MMC shall support the full frequency range from 0 Mhz - 26 Mhz, or 0 MHz - 52 MHz
3. Device can operate as high-speed Device interface timing at 26 MHz clock frequency.
4. CLK rise and fall times are measured by min (V_{IH}) and max (V_{IL}).
5. Inputs CMD, DAT rise and fall times are measured by min (V_{IH}) and max (V_{IL}), and outputs CMD, DAT rise and fall times are measured by min (V_{OH}) and max (V_{OL}).

Table 11. Backward Compatible Device Interface Timing

Paramter	Symbol	Min	Max	Unit	Remark[*1]
Clock CLK[*2]					
Clock frequency data transfer mode (PP)[*3]	f_{PP}	0	26	MHz	CL ≤ 30pF
Clock frequency identification mode (OD)	f_{OD}	0	400	kHz	-
Clock high time	t_{WH}	10	-	ns	CL ≤ 30pF
Clock low time	t_{WL}	10	-	ns	CL ≤ 30pF
Clock rise time[*4]	t_{TLH}	-	10	ns	CL ≤ 30pF
Clock fall time	t_{THL}	-	10	ns	CL ≤ 30pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3	-	ns	CL ≤ 30pF
Input hold time	t_{IH}	3	-	ns	CL ≤ 30pF
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer[*5]	t_{ODLY}	11.7	-	ns	CL ≤ 30pF
Output hold time[*5]	t_{OH}	8.3	-	ns	CL ≤ 30pF

Note:

1. The Device must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.
2. CLK timing is measured at 50% of V_{CCQ}.
3. For compatibility with Devices that support the v4.2 standard or earlier, host should not use > 26 MHz before switching to high-speed interface timing.
4. CLK rise and fall times are measured by min (V_{IH}) and max (V_{IL}).
5. t_{OSU} and t_{OH} are defined as values from clock rising edge. However, there may be Devices or devices which utilize clock falling edge to output data in backward compatibility mode. Therefore, it is recommended for hosts either to set t_{WL} value as long as possible within the range which will not go over t_{CK}-$t_{OH(min)}$ in the system or to use slow clock frequency, so that host could have data set up margin for those devices. In this case, each device which utilizes clock falling edge might show the correlation either between t_{WL} and t_{OSU} or between t_{CK} and t_{OSU} for the device in its own datasheet as a note or its' application notes.

Dual Data Rate Interface Timings

Figure 4. Bus Timing in Dual Data Rate Mode

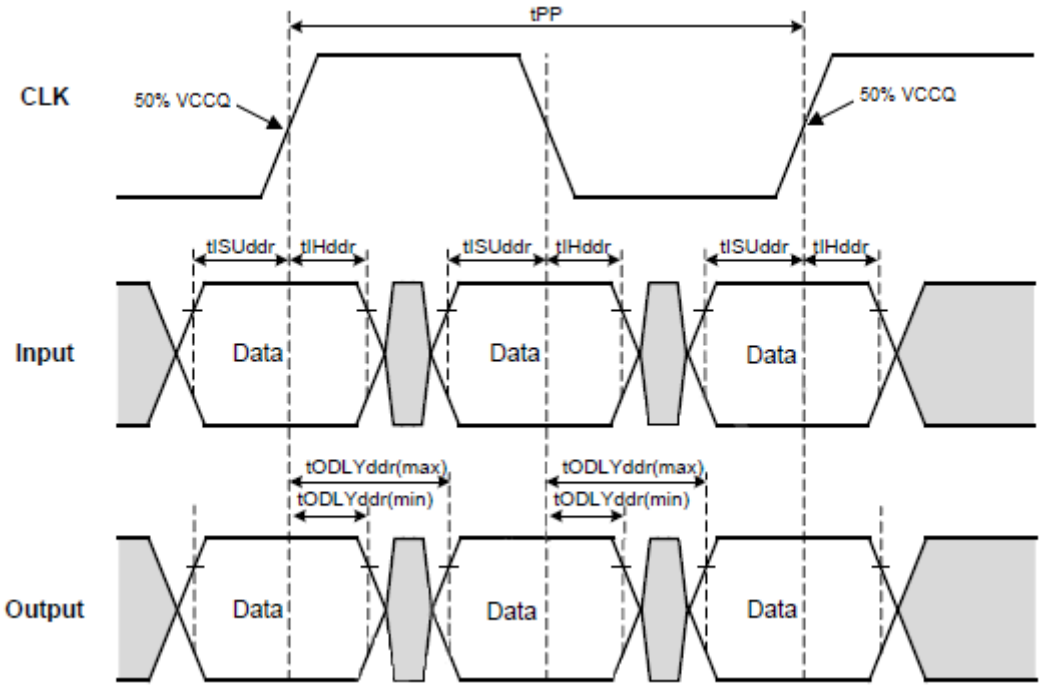


Table 12. High-speed Dual Data Rate Interface Timing

Paramter	Symbol	Min	Max	Unit	Remark
Input CLK[*1]					
Clock duty cycle	-	45	55	%	Includes jitter, phase noise
Clock rise time	t_{TLH}	-	3	ns	CL≤ 30pF
Clock fall time	t_{THL}	-	3	ns	CL≤ 30pF
Input CMD (referenced to CLK-SDR mode)					
Input set-up time	t_{ISUddr}	3	-	ns	CL≤ 20pF
Input hold time	t_{IHddr}	3	-	ns	CL≤ 20pF
Output CMD (referenced to CLK-SDR mode)					
Output delay time during data transfer	t_{ODLY}	-	13.7	ns	CL≤ 20pF
Output hold time	t_{OH}	2.5	-	ns	CL≤ 20pF
Signal rise time	t_{RISE}	-	3	ns	CL≤ 20pF
Signal fall time	t_{FALL}	-	3	ns	CL≤ 20pF
Input DAT (referenced to CLK-DDR mode)					
Input set-up time	t_{ISUddr}	2.5	-	ns	CL≤ 20pF
Input hold time	t_{IHddr}	2.5	-	ns	CL≤ 20pF
Output DAT (referenced to CLK-DDR mode)					
Output delay time during data transfer	$t_{ODLYddr}$	1.5	7	ns	CL≤ 20pF
Signal rise time (DAT0-7)[*2]	t_{RISE}	-	2	ns	CL≤ 20pF
Signal fall time (DAT0-7)	t_{FALL}	-	2	ns	CL≤ 20pF

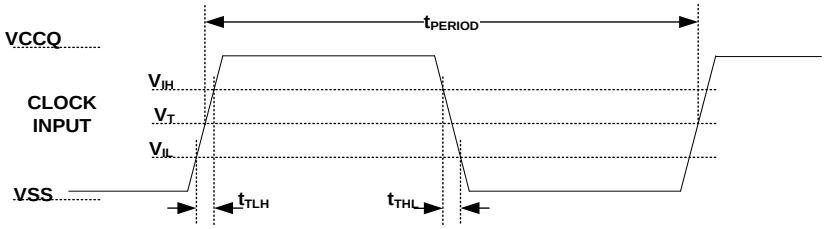
Notes:

1. CLK timing is measured at 50% of V_{CCQ}.
2. Inputs DAT rise and fall times are measured by min (V_{IH}) and max (V_{IL}), and outputs DAT rise and fall times are measured by min (V_{OH}) and max (V_{OL}).

Bus Timing Specification in HS200 mode

HS200 Device Clock Timing

Figure 5. HS200 Device Clock Timing



Note1: V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).

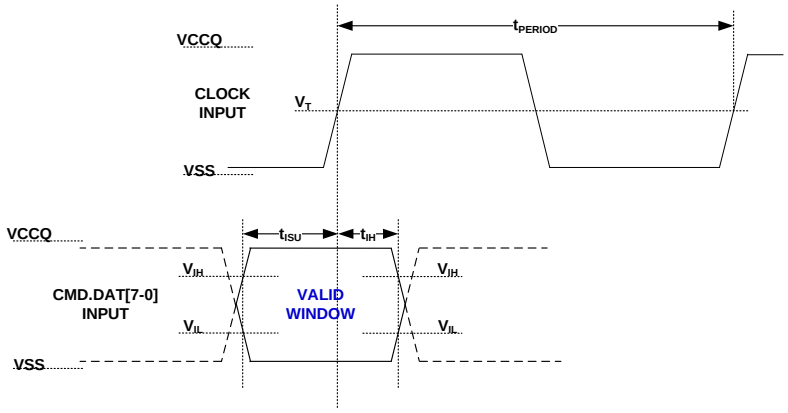
Note2: V_T=0.975V - Clock Threshold (V_{CCQ} = 1.8V) and V_T=0.65V - Clock Threshold (V_{CCQ} = 1.2V), indicates clock reference point for timing measurements.

Symbol	Min.	Max.	Unit	Remark
t_{PERIOD}	5	-	ns	200MHz (Max.), between rising edges
t_{TLH}, t_{THL}	-	0.2· t_{PERIOD}	ns	t_{TLH}, t_{THL} < 1ns (max.) at 200MHz, C_{DEVICE}=6pF, The absolute maximum value of t_{TLH}, t_{THL} is 10ns regardless of clock frequency.
Duty Cycle	30	70	%	

Table 13. HS200 Device Clock Timing

HS200 Device Input Timing

Figure 6. HS200 Device Input Timing



Note1: t_{ISU} and t_{IH} are measured at V_{IL}(max.) and V_{IH}(min.).

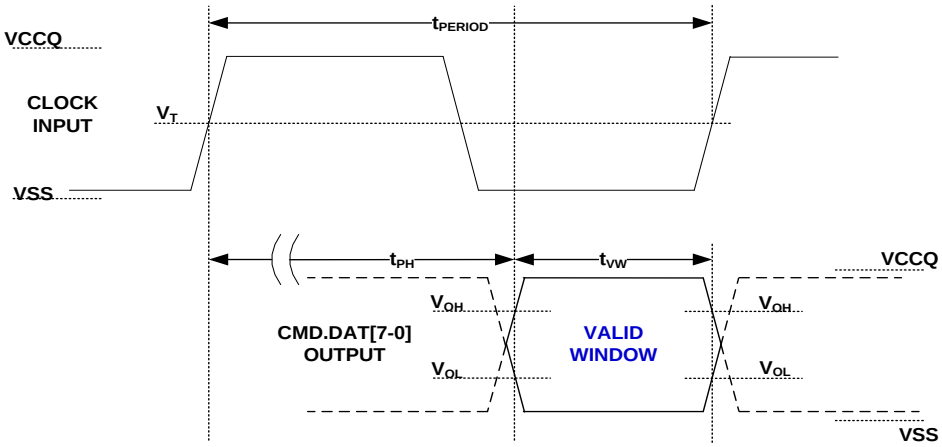
Note2: V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).

Table 14. HS200 Device Input Timing

Symbol	Min.	Max.	Unit	Remark
t_{ISU}	1.40	-	ns	C_{DEVICE} ≤6pF
t_{IH}	0.8	-	ns	C_{DEVICE} ≤6pF

HS200 Device Output Timing

Figure 7. HS200 Device Output Timing



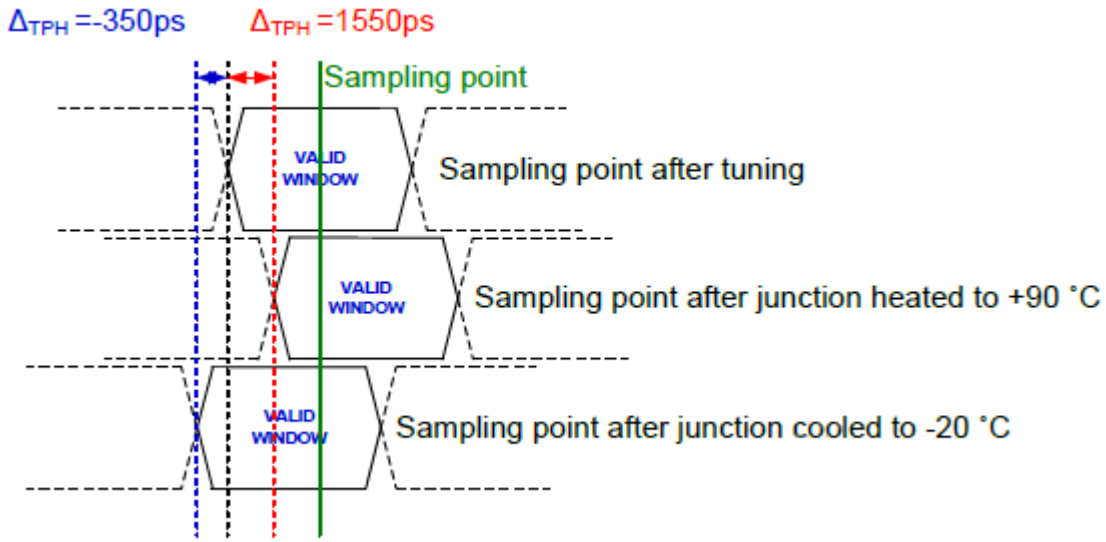
Note: V_{OH} denotes V_{OH}(min.) and V_{OL} denotes V_{OL}(max.).

Table 15. HS200 Device Output Timing

Symbol	Min.	Max.	Unit	Remark
t_{PH}	0	2	UI	Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift.
Δ_{TPH}	-350 (ΔT= -20 deg.C)	+1550 (ΔT=90 deg.C)	ps	Delay variation due to temperature change after tuning. Total allowable shift of output valid window (T_{VW}) from last system Tuning procedure Δ_{TPH} is 2600ps for ΔT from -25 deg.C to 125 deg.C during operation.
t_{VW}	0.575	-	UI	t_{VW}=2.88ns at 200MHz Using test circuit in Figure 6 including skew among CMD and DAT lines created by the Device. Host path may add Signal Integrity induced noise, skews, etc. Expected T_{VW} at Host input is larger than 0.475UI.

Note: Unit Interval (UI) is one bit nominal time. For example, UI=5ns at 200MHz.

Figure 8. t_{PH} Consideration

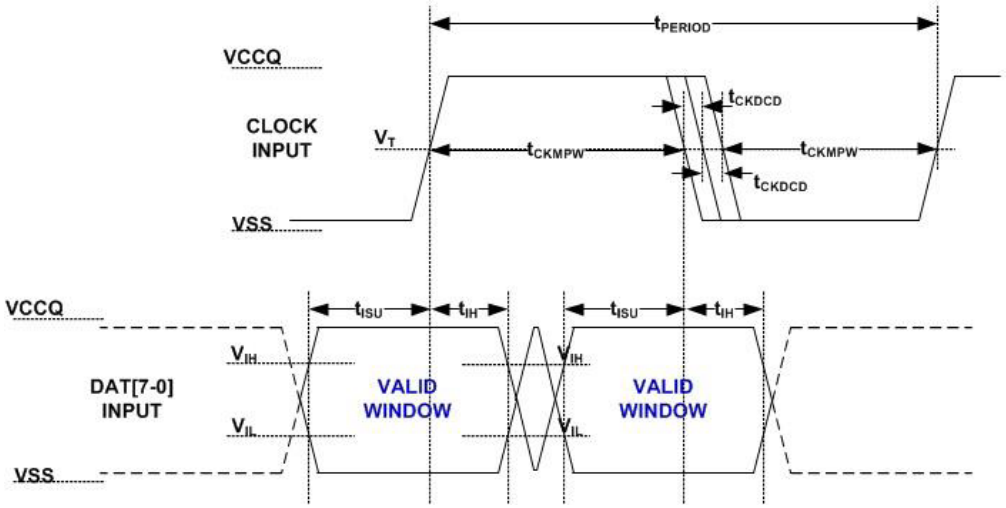


Bus Timing Specification in HS400 mode

HS400 Device Input Timing

The CMD input timing for HS400 mode is the same as CMD input timing for HS200 mode.

Figure 9. HS400 Device Input Timing



Note: V_T = 50% of V_{CCQ}, indicates clock reference point for timing measurements.

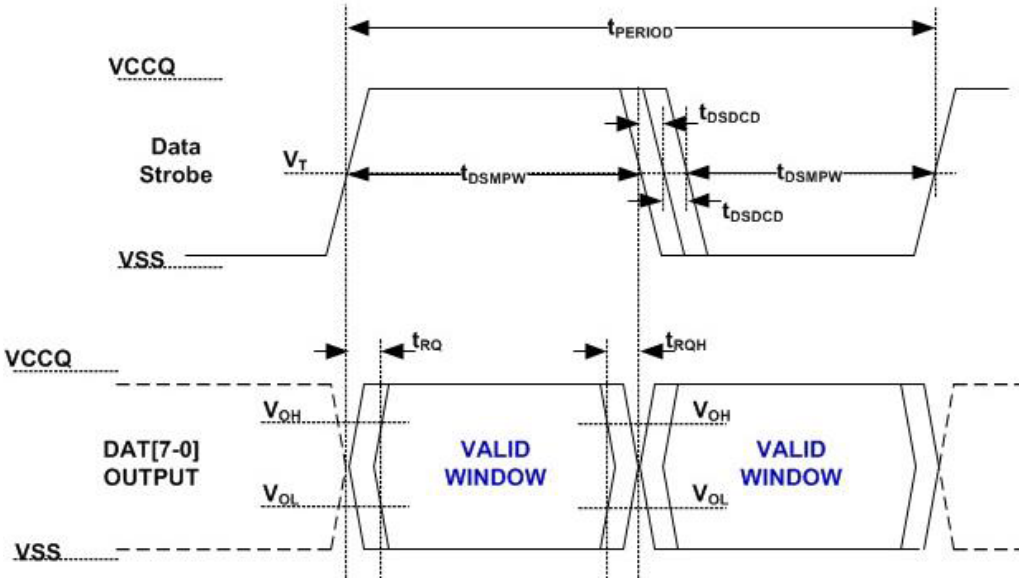
Table 16. HS400 Device Input Timing

Parameter	Symbol	Min	Max	Unit	Remark
Input CLK					
Cycle time data transfer mode	t_{PERIOD}	5	-	-	200MHz(Max), between rising edges With respect to V_T.
Slew rate	SR	1.125	-	V/ns	With respect to V_{IH}/V_{IL}.
Duty cycle distortion	t_{CKDCD}	0.0	0.3	ns	Allowable deviation from an ideal 50% duty cycle. With respect to V_T. Includes jitter, phase noise
Minimum pulse width	t_{CKMPW}	2.2	-	ns	With respect to V_T.
Input DAT (referenced to CLK)					
Input set-up time	t_{ISUddr}	0.4	-	ns	$C_{Device} \leq 6pF$ With respect to V_{IH}/V_{IL}.
Input hold time	t_{IHddr}	0.4	-	ns	$C_{Device} \leq 6pF$ With respect to V_{IH}/V_{IL}.
Slew rate	SR	1.125	-	V/ns	With respect to V_{IH}/V_{IL}.

HS400 Device Output Timing

The Data Strobe is used to read data in HS400 mode. The Data Strobe is toggled only during data read or CRC status response.

Figure 10. HS400 Device Output Timing



Note: V_T = 50% of V_{CCQ}, indicates clock reference point for timing measurements.

Table 17. HS400 Device Output Timing

Parameter	Symbol	Min	Max	Unit	Remark
Data Strobe					
Cycle time data transfer mode	t_{PERIOD}	5	-	-	200MHz(Max), between rising edges With respect to V_T.
Slew rate	SR	1.125	-	V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Duty cycle distortion	t_{DSDCD}	0.0	0.2	ns	Allowable deviation from the input CLK duty cycle distortion (t_{CKDCD}). With respect to V_T. Includes jitter, phase noise
Minimum pulse width	t_{DSMPW}	2.0	-	ns	With respect to V_T.
Read pre-amble	t_{RPRE}	0.4	-	t_{PERIOD}	Max value is specified by manufacturer. Value up to infinite is valid
Read post-amble	t_{RPST}	0.4	-	t_{PERIOD}	Max value is specified by manufacturer. Value up to infinite is valid
Output DAT (referenced to Data Strobe)					
Output skew	t_{RQ}	-	0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Output hold skew	t_{RQH}	-	0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Slew rate	SR	1.125	-	V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load

Table 18. Bus Signal Line Load

Paramter	Symbol	Min	Typ	Max	Unit	Remark
Pull-up resistence for CMD	R_{CMD}	4.7	-	100	KOhm	
Pull-up resistence for DAT0-DAT7	R_{DAT}	10	-	100	KOhm	
Internal pull up resistance DAT1-DAT7	R_{int}	10	-	150	KOhm	
Bus signal line capacitance	C_L	-	-	30	pF	
Single Device capacitance	C_{Device}	-	-	12	pF	
Maximum signal line inductance	-	-	-	16	nH	$f_{PP} \leq 52MHz$

Table 19. HS400 Capacitance and Resistors

Paramter	Symbol	Min	Typ	Max	Unit	Remark
Pull-down resistance for Data Strobe	R_{DS}	10	-	100	KOhm	
Single Device capacitance	C_{DEVICE}	-	-	6	pF	

Note: Recommended maximum value is 50 KOhm for 1.8V interface supply voltages.

eMMC DC Parameter

Table 20. Supply Voltage

Item	Min	Max	Unit
V_{CCQ}	1.70 (2.7)	1.95 (3.6)	V
V_{CC}	2.7	3.6	V
V_{SS}	-0.5	0.5	V

Table 21. Power Consumption

Power Consumption		NAND	Controller	Unit
V_{CC} = 3.3V, V_{CCQ} = 1.8V				
Active power consumption during operation (1, 2)	Read	TBD	TBD	mA
	Write	TBD	TBD	mA
Lower power mode(stand-by) (3)		TBD	TBD	uA
Lower power mode(sleep) (4)		TBD	TBD	uA

Note:

1. Test condition: Bus width x8, 200 MHz DDR, 512KB data transfer, measured on internal board, 25°C.
2. The measurement for max RMS current is the average RMS current consumption over a period of 100ms.
3. Power measurement conditions: Bus configuration = x8, No CLK.
4. Bus configuration = x8, No CLK. In sleep state, triggered by CMD5. Flash V_{CC} power supply is switched off.

For 2.7 V - 3.6 V V_{CCQ} range (compatible with JESD8C.01)

Table 22. Push-pull signal level - high-voltage

Paramter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	V_{OH}	0.75 * V_{CCQ}	-	V	I_{OH} = -100 µA @ V_{CCQ} min
Output LOW voltage	V_{OL}	-	0.125 * V_{CCQ}	V	I_{OL} = 100 µA @ V_{CCQ} min
Input HIGH voltage	V_{IH}	0.625 * V_{CCQ}	V_{CCQ} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.25 * V_{CCQ}	V	

For 1.70V - 1.95V V_{CCQ} range

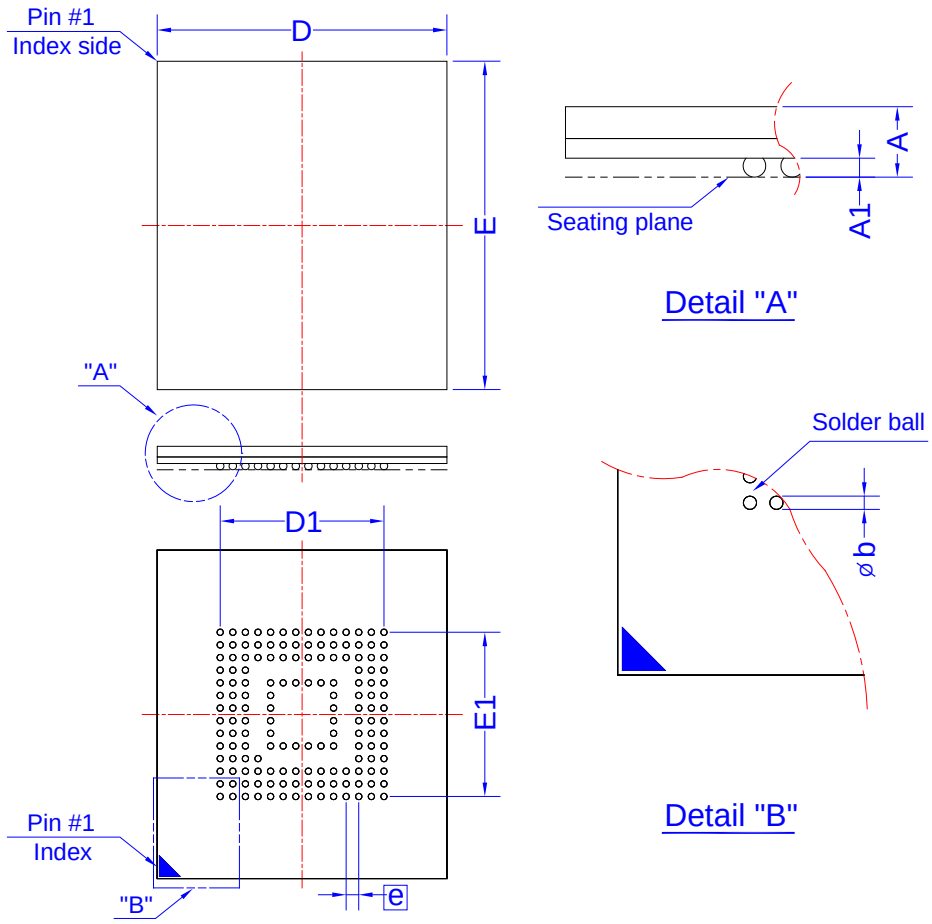
Table 23. Push-pull signal level - 1.70V-1.95V V_{CCQ} voltage range

Paramter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{CCQ} - 0.45	-	V	I_{OH} = -2mA
Output LOW voltage	V_{OL}	-	0.45	V	I_{OL} = 2mA
Input HIGH voltage	V_{IH}	0.65 * V_{CCQ}(1)	V_{CCQ} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.35 * V_{CCQ}(2)	V	

Note:
1. 0.7 * V_{DD} for MMC4.3 and older revisions.
2. 0.3 * V_{DD} for MMC4.3 and older revisions.

PACKING DIMENSIONS

Figure 11. 153-BALL (11.5x13 mm)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	0.90	1.00	1.10	0.035	0.039	0.043
A_1	0.17	0.22	0.27	0.007	0.009	0.011
Φ_b	0.25	0.30	0.35	0.010	0.012	0.014
D	11.40	11.50	11.60	0.449	0.453	0.457
E	12.90	13.00	13.10	0.508	0.512	0.516
D_1	6.50 BSC			0.256 BSC		
E_1	6.50 BSC			0.256 BSC		
e	0.50 BSC			0.020 BSC		

Controlling dimension: Millimeter.

(Revision date: Jan 13 2020)

Revision History

Revision	Date	Description
0.1	2023/02/21	Original
0.2	2023/05/18	Modify CSD and Extended CSD Register table
1.0	2023/08/02	Delete Preliminary

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